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Electronically Controllable Current-mode True RMS to DC Converter

Predrag B. Petrović

Faculty of Technical Sciences Čačak, SERBIA

Abstract: The paper presents a possible design of an electronically tuneable current-mode RMS-to-DC converter. The circuit consists of a single multiple-output current-controlled current differencing transconductance amplifier (MO-CCCDTA), two current-controlled conveyors (CCCII), and a grounded resistor and capacitor. The errors related to signal processing were investigated and presented in the paper. The PSpice simulation results are depicted, and they agree well with theoretical anticipation. The maximum power consumption of the converter is approximately 5.80 mW, at ±1.2 V supply voltages.

Keywords: RMS-to-DC converter; current-mode processing; CCCDTA; MOCCCII; simulation

Elektronsko nadzorovan RMS DC pretvornik v tokovnem načinu

Izvleček: Članek opisuje možno obliko elektronsko nastavljivega RMS-DC pretvornika v tokovnem načinu. Vezje je sestavljeno iz enega večizhodnega tokovno krmiljenega tokovno diferencialnega transkonduktančnega ojačevalnika (MO-CCCDTA), dveh tokovno krmičjenih ojačevalnikov (CCCII) in ozemljenega upora ter kondenzatorja. Raziskane in predstavljene so napake v zvezi signalom. Opravljena je bila PSpice analiza, ki se dobro ujema s teorijo. Največja poraba pretvornika je 5.80 mW pri napajalni napetosti ±1.2 V.

Ključne besede: RMS-DC pretvornik; CCCDTA, MOCCCII, simulacije

** Corresponding Author's e-mail: predrag.petrovic@ftn.kg.ac.rs*

1 Introduction

Magnitude-detection circuits, e.g. envelope detectors, peak detectors and RMS-to-DC converters produce an estimate of a signal's magnitude, and are important elements in communications transceivers, automatic gain control systems and analog spectrum analysers [1].

Mobile communication terminals or handsets have become ubiquitous in the modern society, creating insatiable market demand for and more efficient power supply solutions for the mobile terminal. Accurate monitoring of the transmitting power of the mobile terminal helps to optimise power consumption and performance of the wireless network [2]. Detectors intended for this purpose need to involve wide bandwidth, high input impedance, low loss, low noise, and are expected to be compact and robust in the presence of process-voltage-temperature (PVT) variations. High dynamic range and low power consumption are also desirable.

Different methods have been reported for the precision measuring of the RMS value of an AC voltage, such as sampling [2], Monte Carlo [3] and the wavelet transform [4, 5]. The implicit RMS converter described in [6–9] has been used for many years. Most of these devices similarly comprise two main parts: a full-wave rectifier (or absolute-value) circuit and a multiplier/divider circuit employing a log-antilog principle. High-frequency performances of these devices are limited to less than 5 MHz due to the band-width and the slow rate of the full-wave rectifier. Design technologies based on bipolar dynamic trans-linear circuits were proposed to implement true RMS-to-DC converters [10, 11]. Although these schemes require only NPN transistors, their circuits are operated in only one quadrant and employ full-wave rectifiers. The new design for RMS-to-DC converter relies on the dual trans-linear-based squarer circuit proposed in [12, 13], where the input current can be a two-quadrant current signal. Given that the full-wave rectifier is not required within this conversion scheme, the circuit exhibits a wide bandwidth, which,

due to the input interference, still appears limited compared to thermal-based or diode-based detectors [14].

Presently, there is a growing interest in synthesising the current-mode circuits because of a number of their potential advantages such as larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry and lower power consumption. The current differencing transconductance amplifier, CDTA [15], appears to be a versatile component in the realization of a class of analog signal-processing circuits. This device is quite suitable for the synthesis of current-mode circuits with electronically tunable properties. Moreover, the use of the CDTA as an active element provides the circuit implementations with a reduced number of passive elements, thereby leading to compact structures in some applications.

This paper presents the principles of operation, and the detailed circuit design of the new current-mode realisation of the bipolar RMS detector. The proposed detector uses an implicit computation to calculate the RMS value of an input signal, similarly to the translinear principle. The paper looks at a small-signal approach to the problem, i.e. voltage-to-current relations are regarded as linear, while in translinear circuits, the ability of exponential function to convert a sum of signals (voltages) into signal products (currents) is utilised. The fundamental building block is an analog multiplier/divider realised with one MO-CCCDTA, the anticipated exploitation of the proposed circuit being extended up to 10 MHz, with increased linearity and precision in determining the effective value. Unlike the detector described in [16, 17], which was realised using the CMOS technology, the one described in this paper involves simpler and more accurate control structure. Besides, the proposed circuit does not require a more precise bias voltages realization and complex transistor pairing, which was typical of the realisations described in [16, 17]. Additionally, it has fewer active building blocks and allows a faster access to the required feedback – the RMS of the input signal which is the subject of processing. In addition, the circuit comprises two grounded passive components (resistor and capacitor), rendering it very suitable for the IC implementation. The PSpice simulation results are also shown, and they are in agreement with theoretical analysis.

2 Proposed detector circuit

The proposed current-mode RMS detector using the MO-CCCDTA and MO-CCCIIs [18] is shown in Fig. 1. MO-CCCDTA properties are similar to the conventional CDTA, except that input voltages of MO-CCCDTA are not zero and the MO-CCCDTA has finite input resistances R_p and R_n at the *p* and *n* input terminals, respectively. These parasitic resistances are equal and can be controlled by the bias current I_p (Fig. 2).

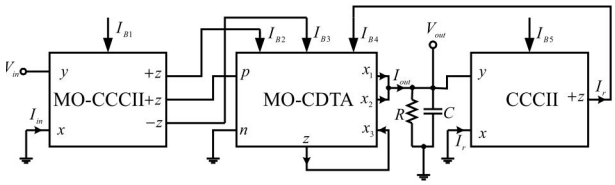


Figure 1: The proposed RMS circuit

Using the standard notation for the MO-CCCDTA, the circuit can be described by the following constitutive equations:

$$v_p = v_n = 0; i_z = i_p - i_n, and\ i_x = g_m v_z = g_m Z_z i_z \quad (1)$$

where *p* and *n* are input terminals, *z* and ± *x* are output terminals, g_m is the transconductance gain, and Z_z is external impedance connected at the terminal *z*. Based on the expressions above, the current flow out of the terminal *z* (i_z) is a difference between the input currents through the terminals *p* and *n* (i_p–i_n). The voltage drop at the terminal *z* is transferred to the current at the terminal *x* (i_x) by a transconductance gain (g_m) of the CDTA. These currents, copied to a general number of output current terminals *x*, are equal in magnitude.

While there are several technologies to realize the CDTA, one of the possible bipolar realizations is shown in Fig. 2.

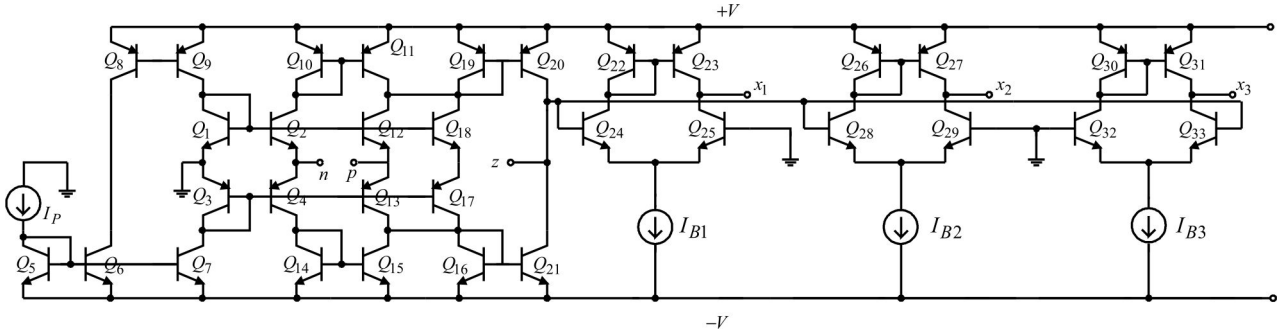


Figure 2: Bipolar realisation of MO-CCCDTA

It mainly comprises a current differencing circuit formed by two current followers, a basic current mirror and a multiple-output transconductance amplifier. Here, the transconductance gain g_m of the CDTA is directly proportional to the external bias current I_B (three bias currents I_{B2}, I_{B3} and I_{B4} in the case of proposed converter circuit, Fig. 1), which can be written by:

$$g_m = \frac{I_B}{2V_T} \tag{2}$$

where V_T= 26 mV at 27°C is the usual thermal voltage given by kT/q, k = Boltzmann's constant = 1.38×10^{-23} J/K, T = the absolute temperature (in Kelvins), and q = 1.6×10^{-19} C.

Generally, a MO-CCCII is a multiple-terminal active building block, as shown in Fig. 1. The port relations of the MO-CCCII can be presented by the following equation [1]:

$$i_y = 0; v_x = v_y + i_x R_x; i_{z+} = +i_x; i_{z-} = -i_x \tag{3}$$

The bipolar realisation of the MO-CCCII is proposed in [18]. In this case, the parasitic resistance R_x at the terminal x can be expressed by:

$$R_x = \frac{V_T}{2I_B} \tag{4}$$

where V_T is the thermal voltage and I_B (I_{B1} and I_{B5} in the proposed realisation, Fig. 1) is the bias current of the conveyor which remains tunable over several decades.

By the routine analysis of the proposed RMS circuit shown in Fig. 1 and using the properties of MO-CCCDTA and MO-CCCII, the output current at z terminal of MO-CCCDTA is obtained by:

$$I_z = I_{in} = I_{x3} \tag{5}$$

whereupon the output voltage at z terminal (V_z) of MO-CCCDTA equals:

$$V_z = \frac{I_{x3}}{g_{m3}} = \frac{2V_T I_{in}}{I_r} \tag{6}$$

Figure 1 infers that $I_{B2} = I_{in}$, $I_{B3} = -I_{in}$ and $I_{B4} = I_r$. Thus, the I_{x1} and I_{x2} can be obtained by:

$$I_{x1} = \begin{cases} g_{m1}V_z = \dfrac{I_{in}^2}{I_r} \; if \; I_{in} > 0 \\ 0 \; if \; I_{in} < 0 \end{cases}$$
$$I_{x2} = \begin{cases} 0 \; if \; I_{in} > 0 \\ g_{m2}V_z = \dfrac{I_{in}^2}{I_r} \; if \; I_{in} < 0 \end{cases} \tag{7}$$

The equation above suggests the output current I_{out} as:

$$I_{out} = I_{x1} + I_{x2} = \frac{I_{in}^2}{I_r} == \frac{R_{x2}}{R_{in}^2}\frac{V_{in}^2}{V_{out}} \tag{8}$$

Where $R_{in} = R_{x1}$. The current I_{out} is then converted to the output voltage, V_{out}, with an implied low-pass filtering function. We can recognise that the output current-to-voltage conversion (with second CCCII) establishes a differential equation relating the current, I_{out}, to the output voltage, V_{out}, i.e.:

$$\dot{V}_{out}(t) + \omega_0 V_{out}(t) = \frac{1}{C} I_{out}(t); \; \omega_0 = \frac{1}{RC} \tag{9}$$

A simple way to obtain this equation is to determine the transfer function relating I_{out} to V_{out}, and then take this back to the time domain. Equation (9) is the generic time-domain description of a low-pass filter, where the coefficient of the undifferentiated term on the LHS of the equation equals the filter cut-off frequency. Equation (8) can subsequently be combined with the above to obtain:

$$\dot{V}_{out}(t) + \omega_o V_{out}(t) = \frac{1}{R_1 C}\frac{V_{in}^2(t)}{V_{out}(t)}; \quad R_1 = \frac{R_{in}^2}{R_{x2}} \tag{10}$$

We may now multiply both sides of the equation by $2V_{out}$ and make a simple observation incorporated into the final result:

$$2V_{out}(t)\dot{V}_{out}(t) + 2\omega_o V_{out}^2(t) = \frac{2}{R_1 C}V_{in}^2(t) \Rightarrow$$
$$\frac{d}{dt}\left(V_{out}^2(t)\right) + 2\omega_o\left(V_{out}^2(t)\right) = \frac{2}{R_1 C}V_{in}^2(t) \tag{11}$$

Equation (11) is a first-order differential equation relating $(V_{out})^2$ and $(V_{in})^2$, having the same form as (9). Therefore, the square of the output is a low-pass filtered version of the square of the input. Based on (11), we can assume that:

$$V_{out}^2(t)=\frac{2}{R_1C}\int_0^t e^{-2\omega_0(t-\tau)}V_{in}^2(\tau)d\tau \quad (12)$$

The equation above (convolution integral) implies that if the square root of both sides is considered, the output is the root mean square of the input voltage, where the integral is assumed to compute mean value function. The implied filtering function is thus given by:

$$H(s)=\frac{R}{R_1}\frac{\omega_{3db}}{s+\omega_{3db}},\ where\ \omega_{3db}=\frac{2}{RC} \quad (13)$$

The low-pass filter performs averaging of the RMS function and needs to be of a lower corner frequency than the lowest frequency of interest. For line frequency measurements, this filter is simply too large to implement on-chip, but the proposed detector requires only one capacitor on the output to implement the low-pass filter. This capacitor can be selected by the user, depending on frequency range and settling time requirements. Low-pass filtering the square of the input sine functions with some a certain amplitude, frequency and phase shift ($V_{in}(t)=V\cos(\omega t+\phi)$), as suggested by (11), yields a time function $y(t)$ given by:

$$y(t)=\frac{V^2}{2}\left(1+\frac{1}{\sqrt{1+(2\omega/\omega_{3db})^2}}\cos(2\omega t)\right)=V_{out}^2(t) \quad (14)$$

The input phase shift, such as the net phase shift, after filtering of the second harmonic, yields zero phase, thereby simplifying the form of $y(t)$ without the loss of generality. R/R_1 was set to unity for simplicity reasons.

If we assume that the input signal frequency is considerably higher than the filter cut-off frequency, the approximate final output can be rather successfully estimated with just a few terms of a Taylor series. Accordingly, the DC component of the output voltage of the proposed circuit, i.e. the apparent output RMS value of the input and the associated second-harmonic component of the output voltage resulting from the rapidly decreasing magnitudes of higher harmonic terms, such as the ripple (peak-to-peak ripple of the output), is expressed as:

$$V_{RMS}\approx\left[1-\frac{1/16}{1+(2\omega/\omega_{3db})^2}\right]V_{true-RMS}$$
$$V_{ripple}\approx\frac{1/2}{\sqrt{1+(2\omega/\omega_{3db})^2}}V_{true-RMS} \quad (15)$$

The equation above infers the accuracy associated with the proposed circuit for measuring the effective value of the input sine voltage signal. In the case of the input signal described by the Fourier order, the estimation defined by (15) gains in complexity, whereas it also clearly implies that it is possible to filter and single out the effective value of the signal processed in the respective manner.

3 Non-ideal system analysis

The effects of MO-CDTA and MO-CCCII non-idealities on the RMS detector performance are to be considered in this section. By considering the non-ideal MO-CCCII characteristics, equation (3) can be rewritten as:

$$i_y=0;\ v_x=\alpha v_y+i_xR_x;\ i_{z+}=+\beta_p i_x;\ i_{z-}=-\beta_n i_x \quad (16)$$

where $\alpha=1-\varepsilon_v$ and ε_v ($|\varepsilon_v|<<1$) represents the voltage tracking error from y to x terminal, $\beta_p=1-\varepsilon_p$ and ε_p ($|\varepsilon_p|<<1$) denotes the current tracking error from x to $+z$ terminal, while $\beta_n=1-\varepsilon_n$ and ε_n ($|\varepsilon_n|<<1$) stands for the current tracking error from x to $-z$ terminal of the MO-CCCII, respectively. Given the non-idealities, currents generated from first and second CCCIIs (first and third circuits of the proposed realization in Fig. 1) can be defined as:

$$I_{in}=\frac{\alpha_1V_{in}}{R_{x1}};\ i_p=I_{B2}=\frac{\beta_{p1}\alpha_1V_{in}}{R_{x1}};$$
$$I_{B3}=\frac{\beta_{n1}\alpha_1V_{in}}{R_{x1}};\ I_r=\frac{\beta_{p2}\alpha_2V_{out}}{R_{x2}} \quad (17)$$

In practice, the deviation from the ideal performance of the proposed RMS circuits is mainly due to the non-ideal CDTA characteristics, which can be divided into two categories, i.e. parasitic gain effects and parasitic impedance effects. Fig. 3 illustrates the simplified equivalent circuit represented by the behavior of the non-ideal CDTA.

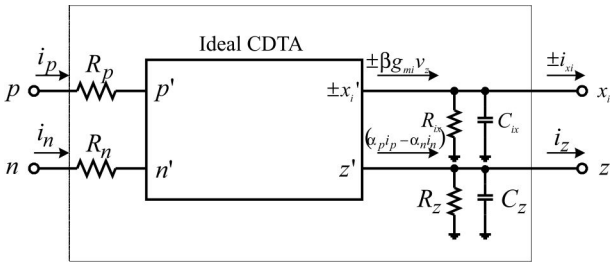


Figure 3: The equivalent circuit of the non-ideal CDTA

A practical CCCDTA device can be modelled as an ideal CCCDTA with finite parasitic resistances and capacitances, as well as non-ideal current transfer gains and a transconductance inaccuracy factor of the CCCDTA. Fig. 3 shows a more sophisticated circuit model to represent the non-ideal CCCDTA device, where R_p, R_n, R_x, and R_z are the terminal parasitic resistances. R_p and R_n are the current-controllable parasitic resistances, where R_x and R_z, as typical values of the parasitic resistances, connected to the terminals *x* and *z* respectively, are in the range of several mega-ohms. C_x and C_z are the terminal parasitic capacitances from terminals *x* and *z* to the ground (the shunt output impedances ($R_z//C_z$ and $R_x//C_x$) at terminals *z* and *x*, respectively). Typically, these parasitic capacitances are in the order of several pFs. In Fig. 3, α_p represents the non-ideal current transfer gain from the *p* terminal to the *z* terminal of the CCCDTA, α_n denotes the non-ideal current transfer gain from the *n* terminal to the *z* terminal of the CCCDTA, and β is the transconductance inaccuracy factor from the *z* terminal to the *x* terminal of the CCCDTA. The typical values of the non-ideal current transfer gains and the transconductance inaccuracy factor α_n, α_p, and β range from 0.9 to 1, with an ideal value of 1.

Based on the circuit representation in Fig. 3 and the proposed RMS detector, and given the non-ideal CDTA characteristics, after applying the non-ideal equivalent circuit mode of the CCCDTA to the proposed circuit, tedious derivations lead to the following modified characteristic equation):

$$i_p = I_{B2} = \frac{\alpha_1\beta_{p1}V_{in}}{R_{x1}};\ I_{B3} = \frac{\alpha_1\beta_{n1}V_{in}}{R_{x1}};$$
$$I_r = \frac{\alpha_2\beta_{p2}V_{out}}{R_{x2}} = I_{B4} \tag{18}$$

$$V_z = \frac{R_z}{1+sR_zC_z}\left(\alpha_p i_p - \beta g_{m3}V_z\right) \Rightarrow$$
$$V_z = \frac{\alpha_p R_z}{1+\beta g_{m3}R_z + sR_zC_z} i_p; \tag{19}$$
$$g_{m3} = \frac{I_r}{2V_T} = \frac{\alpha_2\beta_{p2}V_{out}}{2V_T R_{x2}}$$

The modified output current for the proposed RMS detector can be rewritten as:

$$I_{out} = \begin{cases} \beta g_{m1}V_z \dfrac{\frac{R_{1x}}{1+sC_{1x}R_{1x}}}{\frac{R_{1x}}{1+sC_{1x}R_{1x}} + \frac{R}{1+sCR}} = \beta g_{m1}V_z \dfrac{R_{1x}(1+sCR)}{R_{1x}(1+sCR)+R(1+sC_{1x}R_{1x})}; V_{in} > 0 \\ \beta g_{m2}V_z \dfrac{\frac{R_{2x}}{1+sC_{2x}R_{2x}}}{\frac{R_{2x}}{1+sC_{2x}R_{2x}} + \frac{R}{1+sCR}} = \beta g_{m2}V_z \dfrac{R_{2x}(1+sCR)}{R_{2x}(1+sCR)+R(1+sC_{2x}R_{2x})}; V_{in} < 0 \end{cases} \tag{20}$$
$$g_{m1} = \frac{I_{B2}}{2V_T};\ g_{m2} = \frac{I_{B3}}{2V_T}$$

It follows that:

$$I_{out} = \begin{cases} \beta \dfrac{\frac{\alpha_1\beta_{p1}V_{in}}{R_{x1}}}{2V_T} \dfrac{\alpha_p R_z}{1+\beta\frac{\alpha_2\beta_{p2}V_{out}}{2V_T R_{x2}}R_z + sR_zC_z} \dfrac{\alpha_1\beta_{p1}V_{in}}{R_{x1}} \dfrac{R_{1x}(1+sCR)}{R_{1x}(1+sCR)+R(1+sC_{1x}R_{1x})} \\ = \dfrac{\alpha_1^2\beta_{p1}^2\alpha_p R_z}{\left(2\frac{V_T}{V_{out}}R_{x2} + \beta\alpha_2\beta_{p2}R_z + 2\frac{V_T}{V_{out}}R_{x2}sR_zC_z\right)} \dfrac{R_{1x}(1+sCR)}{R_{1x}(1+sCR)+R(1+sC_{1x}R_{1x})} \dfrac{R_{x2}}{R_{x1}^2}\dfrac{V_{in}^2}{V_{out}}; & V_{in} > 0 \\ = k_1(s)\dfrac{R_{1x}(1+sCR)}{R_{1x}(1+sCR)+R(1+sC_{1x}R_{1x})}\dfrac{R_{x2}}{R_{x1}^2}\dfrac{V_{in}^2}{V_{out}} \\ \beta \dfrac{\frac{\alpha_1\beta_{n1}V_{in}}{R_{x1}}}{2V_T} \dfrac{\alpha_p R_z}{1+\beta\frac{\alpha_2\beta_{p2}V_{out}}{2V_T R_{x2}}R_z + sR_zC_z} \dfrac{\alpha_1\beta_{p1}V_{in}}{R_{x1}} \dfrac{R_{2x}(1+sCR)}{R_{2x}(1+sCR)+R(1+sC_{2x}R_{2x})} \\ = \dfrac{\alpha_1^2\beta_{n1}\beta_{p1}\alpha_p R_z}{\left(2\frac{V_T}{V_{out}}R_{x2} + \beta\alpha_2\beta_{p2}R_z + 2\frac{V_T}{V_{out}}R_{x2}sR_zC_z\right)} \dfrac{R_{2x}(1+sCR)}{R_{2x}(1+sCR)+R(1+sC_{2x}R_{2x})} \dfrac{R_{x2}}{R_{x1}^2}\dfrac{V_{in}^2}{V_{out}}; & V_{in} < 0 \\ = k_2(s)\dfrac{R_{2x}(1+sCR)}{R_{2x}(1+sCR)+R(1+sC_{2x}R_{2x})}\dfrac{R_{x2}}{R_{x1}^2}\dfrac{V_{in}^2}{V_{out}} \end{cases} \tag{21}$$

where:

$$k_1(s) = \frac{\alpha_1^2\beta_{p1}^2\alpha_p R_z}{\left(2\frac{V_T}{V_{out}}R_{x2} + \beta\alpha_2\beta_{p2}R_z + 2\frac{V_T}{V_{out}}R_{x2}sR_zC_z\right)}$$
$$k_2(s) = \frac{\alpha_1^2\beta_{n1}\beta_{p1}\alpha_p R_z}{\left(2\frac{V_T}{V_{out}}R_{x2} + \beta\alpha_2\beta_{p2}R_z + 2\frac{V_T}{V_{out}}R_{x2}sR_zC_z\right)} \tag{22}$$

The expressions above infer that the deviations in the transfer current gains are mainly the result of parasitic gains of the CDTAs. In order to improve the discrepancy to theoretical response, a high-performance CDTA with minor parasitic effects need to be employed. However, easy compensation for these deviations is possible by adjusting the values of I_{B1} and I_{B3}, respectively. The output voltage of the proposed RMS detector is defined as:

$$V_{out} = \beta g_{mi}V_z \frac{R'}{1+sC'R'};\ R' = \frac{RR_{ix}}{R+R_{ix}};$$
$$C' = C + C_{ix};\ i = 1,2. \tag{23}$$

Given the non-ideal characteristics of MO-CDTA and CCCIIs, the implied filtering function implies that:

$$H'(s) = k_i(s)\frac{R'}{R_1}\frac{\omega'_{3db}}{s+\omega'_{3db}},$$
$$where\ \omega'_{3db} = \frac{2}{R'C'};\ i = 1,2. \tag{24}$$

Equation (24) suggests that filtering function, represented by the integral operators (equation (12), poses different characteristics in comparison with the ideal situation (equation (13), especially in the operators' behavior at higher frequencies.

4 Simulation results

To confirm the given theoretical analysis, the proposed current-mode bipolar RMS circuit in Fig. 1 was simulated using the PSpice program. The CCCDTA and CCCIIs were realized by the schematic bipolar implementations given in Fig. 2 and [18], with the transistor model parameters of PR200N (PNP) and NP200N (NPN) of the bipolar arrays ALA400 from AT&T [19]. The supply voltages and the values of the bias currents were +V = –V = 1.2 V and $I_{B1} = I_{B5} = 100$ μA, $I_P = 300$ μA respectively, whereas the input voltage was within the range of 0 ÷ 500 mV.

Fig. 4 shows the wave form of the signal at the output of the circuit shown in Fig. 1 (voltage $V_{out}(t)$), whereby the total power dissipation was 5.80 mW. Small power consumption of the proposed circuits results from the application of low-voltage current mode and transconductance mode integrated circuits, with the use of bipolar transistor technology. Applying the current mode signal processing to solve the issues under consideration is a sensible approach to the problem. However, similar and sometimes lower power consumption can be achieved using CMOS technology instead of the bipolar one.

The output ripple is always considerably greater than the DC error; therefore, filtering out the ripple can substantially reduce the peak error without applying a long settling-time penalty by simply increasing the averaging capacitor. The rippling of the output voltage generated in this manner is lower than in detector [16, 20], followed by the shorter feedback as well. Linearity may seem like an odd property for a device that implements a function involving two very nonlinear processes: squaring and square rooting. However, an RMS-to-DC converter has a transfer function, RMS volts in to DC volts out, that should ideally have a 1:1 transfer function. To the extent that the input to output transfer function does not lie on a straight line, the part is nonlinear. Fig. 5 (a) shows the DC transfer function nearing zero in the proposed circuit. Given that the dynamic range has nonlinearity level lower than 1dB, the dynamic range of the circuit proposed in this paper is around 35 dB. The proposed detector circuit involves higher linearity compared to the ones described in [16, 20, 21].

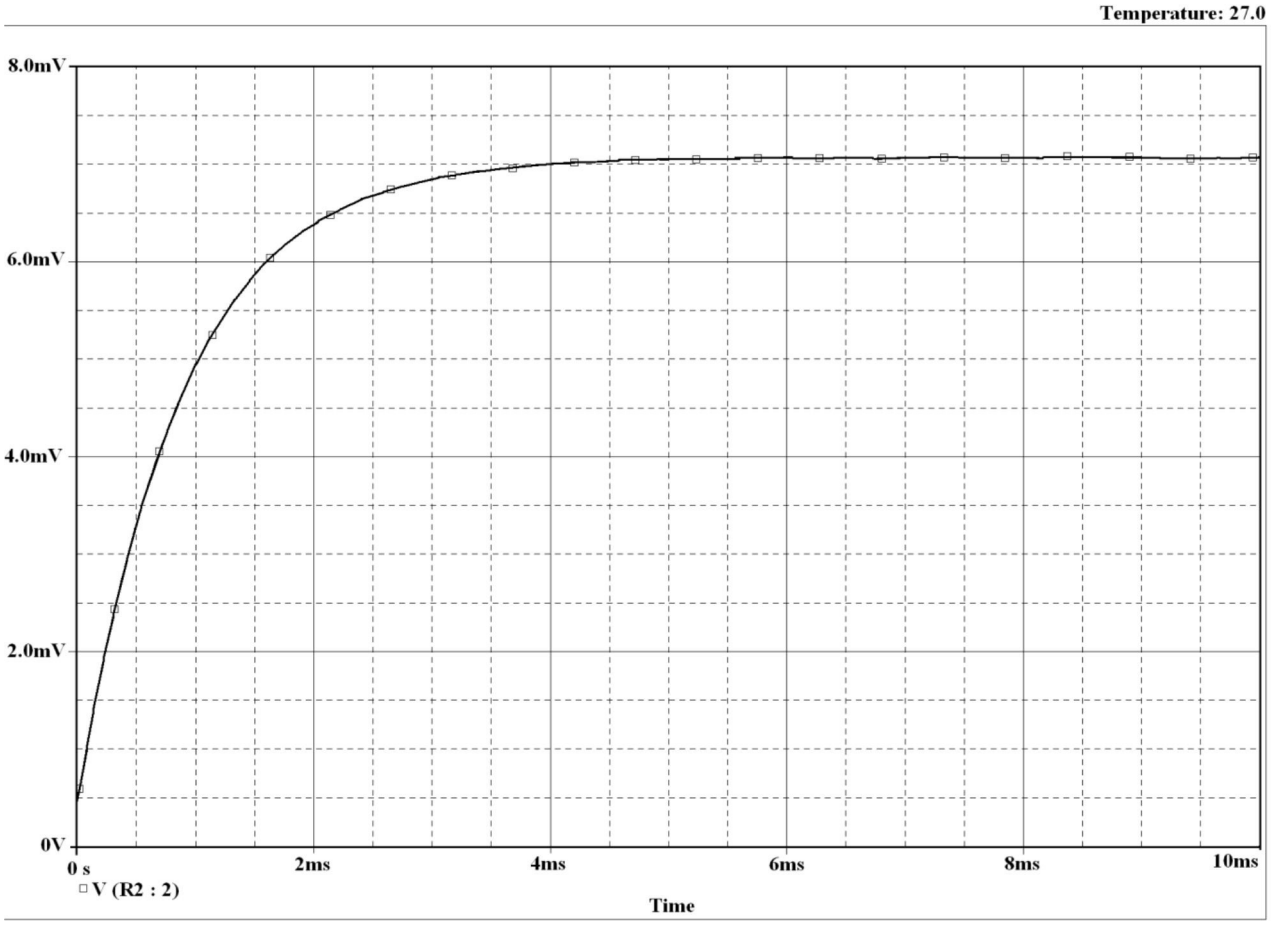
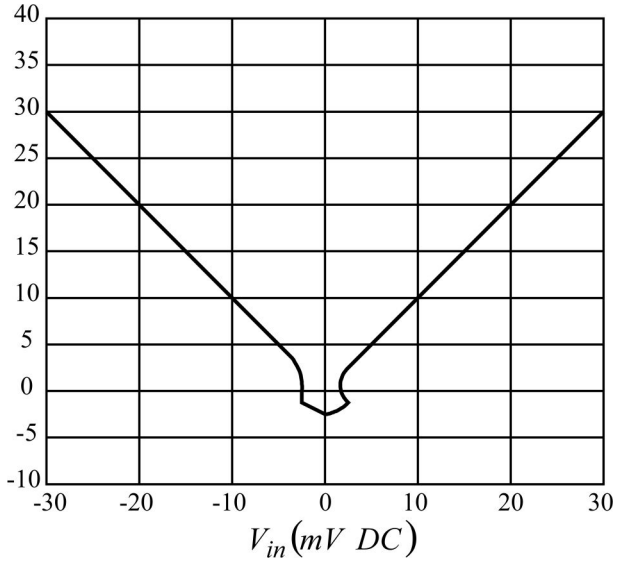
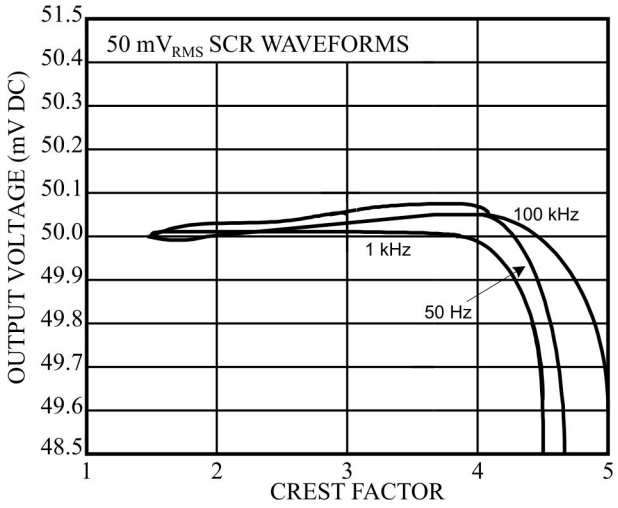


Figure 4: Time-domain response of the proposed RMS circuit for the sine input signal ($V_{in}(t) = 10\sin(2\pi ft)[\mathrm{mV}]$, $f = 100$ kHz, $R = 180$ Ω, $C = 5$ μF)



a)



b)

Figure 5: a) DC transfer function near zero; b) Performance vs Crest Factor

Crest Factor represents a common method of describing dynamic signal wave shapes. It is the ratio of the peak value relative to the RMS value of a waveform. For example, a signal with a crest factor 4 has a peak four times its RMS value. The proposed circuit performs very well with crest factor 4 or less, and responds with a reduced accuracy to signals with higher crest factors (Fig. 5 (b)). On the Fig. 5 (b) the "SCR waveforms" refers to the ideally chopped sine wave. High performance with crest factors lower than 4 can be directly attributed to the high linearity throughout the proposed solution.

Fig. 4 shows the result for pure sinusoid signal. However, as an RMS detector, the circuit should have consistent response in signals with equal powers but various waveform shapes. Thus, the circuit was simulated using various input waveforms to verify the RMS power detection function. The simulated detector responded to the single-tone sinusoid, two-tone signals (with frequencies of 1 MHz and 3 MHz, and amplitudes of 100 mV and 50 mV), square-waves (duty cycle = 50%) and triangle waves given in Fig. 6. All the used signals were at 1MHz. The relative errors were lower than 0.04 % for $P_{in} \leqq$ -20 dBm. Given that the dynamic range has nonlinearity level lower than 1dB, the dynamic range of the circuit proposed in this paper is around 36 dB.

The frequency responses, dynamic range of this bipolar detector, were all comparable and even superior to most diode detectors. The error in computing the effective value of the processed input voltage signal was lower than in [16, 22-26], whereby the circuit of the proposed detector, which includes a wider dynamic range, facilitates the realization more favourably than those described in [21, 23, 26, 27]. Similarly, it does not require a specific compensation procedure.

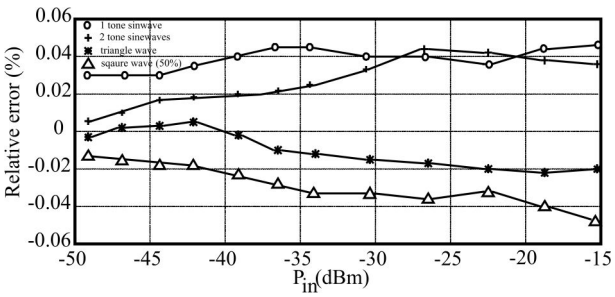


Figure 6: The simulated response of a single detector to various waveforms.

5 Conclusion

This paper reports on a new electronically controllable bipolar translinear RMS-to-DC converter. The proposed circuit employs two CCCIIs, one CDTA and two grounded passive elements, which is advantageous for integration point of view. The proposed circuit ensures high precision, wide bandwidth and high accuracy. The PSPICE simulation results were depicted, and they agree well with the theoretical anticipation.

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