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Design, Fabrication and Measurement of LDNMOS-SCR Devices with Appropriate ESD Protection Window for 18V HV CDMOS Process

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Abstract: Lateral Double Diffused MOSFET (LDMOS) embedded Silicon Controlled Rectifier (SCR) is a normal way to improve the Electro-Static Discharge (ESD) robustness for smart power technologies, but it doesn't always have the proper ESD window for a given application. In this paper, LDNMOS-SCR of four variants structures have been investigated based on a high-voltage (HV) 0.5μm 18V HV CDMOS process with 2D device simulation and silicon verification. Transmission Line Pulse (TLP) testing results demonstrated that those devices successfully elevate the second breakdown current I_{t2} from original 1.146A to above 3A; source isolated device has a lower trigger voltage V_{t1} (45.79V) than source non-isolated devices; the holding voltage V_h of the four devices is related to their structure, and their holding current I_h are all above 800mA, which is big enough to ensure the latch-up immunity under ESD stresses in HV applications. The device with its source isolated from PSUB is the suitable ESD protection device for HV 18V CDMOS technology owning to its strong ESD robustness, low V_{t1}, small on-resistance Ron and sufficiently big I_h.

Keywords: ESD window; LDMOS embedded SCR; TCAD device simulation; TLP

Načrtovanje, izdelava in merjenje naprav LDNMOS-SCR z ustreznim zaščitnim oknom ESD za 18V HV proces CDMOSI

Izvleček: Vgrajeni silicijev usmernik z dvojno lateralno difundiranim MOSFET (LDMOS) je običajen način za izboljšanje odpornosti proti elektrostatičnim razelektritvam (ESD) pri pametnih energetskih tehnologijah, vendar nima vedno ustreznega okna ESD za določeno aplikacijo. V tem članku so bile raziskane štiri različice struktur LDNMOS-SCR na osnovi visokonapetostnega (HV) 0,5μm 18V HV CDMOS procesa z 2D simulacijo naprave. Rezultati testiranja TLP (Transmission Line Pulse) so pokazali, da te naprave uspešno povečajo drugi prebojni tok I_{t2} s prvotnih 1,146A na več kot 3A; izvorno izolirana naprava ima nižjo prožilno napetost V_{t1} (45,79V) kot izvorno neizolirane naprave; držalna napetost V_h vseh štirih naprav je povezana z njihovo strukturo, njihov držalni tok I_h pa je nad 800 mA, kar je dovolj veliko za zagotovitev odpornosti na zaklepanje pri obremenitvah ESD v HV aplikacijah. Naprava z izvorom, izoliranim od PSUB, je primerna naprava za zaščito pred ESD za HV 18V tehnologijo CDMOS zaradi svoje močne odpornosti proti ESD, nizke V_{t1}, majhne upornosti Ron in dovolj velikega I_h.

Ključne besede: Okno ESD; vgrajeni SCR LDMOS; simulacija naprave TCAD; TLP

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1 Introduction

LDMOS power transistors have been commonly used as output driver and ESD protection device simultaneously in the smart power technologies [1-3]. However, the HV LDMOS doesn't have high ESD robustness after entering its snapback breakdown region. Such device exhibits random and unconstrained failures during the snapback breakdown before reaching its intrinsic limitation [4-7]. LDMOS embedded SCR is a normal way to improve the ESD robustness in high voltage technology. Several works have been done to kinds of LDMOS-SCR for smart power application. Wang discussed ESD charateristics about LDMOS-SCR device including its working mechanism, latchup immunity simulation, and response time analyses, etc [8]. Chang proposed the impact of technology layers and layout parameters on the LDMOS-SCR devices robustness [9]. Ker put forward a modified LDMOS-SCR achieving high holding voltage with the aid of RC detection circuit [10]. Lee found that a P+ strip inserted into drain region can improve the ESD failure threshold of embedded SCR LDMOS device [11]. Some other novel structures and their performance were studied for different application purposes in [12-16].

The purpose of this paper is to design a robust ESD protection device with an appropriate ESD window for 18V HV CDMOS technology with respect to traditional gate-grounded LDNMOS (GG-LDNMOS). Four types LDNMOS-SCR are considered in this paper, and the testing devices are fabricated in a 0.5μm 18V HV CDMOS technology. Their ESD characteristics are evaluated by two dimensional (2D) device simulation and transmission line pulse (TLP) measurement.

2 LDNMOS-SCR Devices and working mechanism

The cross-sectional view of conventional GG-LDNMOS is shown in Figure 1. Four types LDNMOS embedded SCR are designed based on the LDNMOS. As shown in Figure 2(a) is the structure for type I device, a P+ diffusion in conjunction with N+ diffusion is added in the deep N well (NWD) to serve as anode of the embedded SCR. The N+ region used as original drain electrode of LDNMOS shrinks its lateral dimension and is let alone with no voltage applying to it. Thus, there will be two discharge ways in the modified structure. One path for ESD current discharging is LDNMOS, it should pass through the NWD resistor named R_{drain} between the floating drain and anode. The other way is through the embedded SCR, the way is composed by P+ diffusion in the anode region, NWD, PW, N+ diffusion in the cathode region. Whatever discharge routing it goes, the avalanche breakdown junction is still at the NWD/PW junction. The equivalent circuit of Type I is shown in Figure 3. The embedded SCR is composed of a vertical p-n-p BJT and a lateral n-p-n BJT to form a 2-terminal/4 layer PNPN (P+/NWD/PW/N+) structure.

The main difference of the other three LDNMOS-SCR devices from Type I device in Figure 2 is that the source of LDNMOS is not isolated from PSUB by NWD. Hence, the avalanche breakdown of those devices could occur either at the NWD/PSUB junction or at the NWD/PW junction. Among those three types non-isolated LDNMOS-SCR, Type III and Type IV have an additional NW surrounded P+&N+ or P+ only at the anode, which will influence their holding voltage (V_h). The equivalent circuit for device Type II, Type III and Type IV is drawn in their cross-sectional view. Although the different anode structures result in the different resistance between the b-e junctions of vertical PNP transistor, the working mechanism of all the LDNMOS-SCR devices is identical.

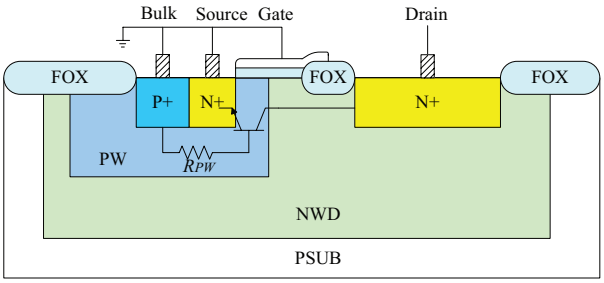

Figure 1: Cross-sectional views of conventional GG-LDNMOS device.

3 TLP testing result and discusions

The above four devices are fabricated as one-finger device with device width of 50μm. The ESD characteristics measurement is performed on the Thermo Celestron I transmission line pulse (TLP) system. It applied a current pulse to the device with a rise time of 10ns, a pluse width of 100ns, and the current stress level increasing continuously until the device failed. The leakage current is measured after each TLP zapping with 19.8V DC voltage on their anode. Once the leakage current is above ~1μA, it is considered that the device under test is failure. The TLP IV curves for LDNMOS with embedded SCR are shown in Figure 4, and corresponding TLP data is summarized in Table 1. TLP measurement data of one-finger traditional GG-LDNMOS with the same device width is also listed in this table for comparison.

It is apparent in Figure 4 that the source isolated LDNMOS-SCR (Type I) has a lower trigger voltage, which

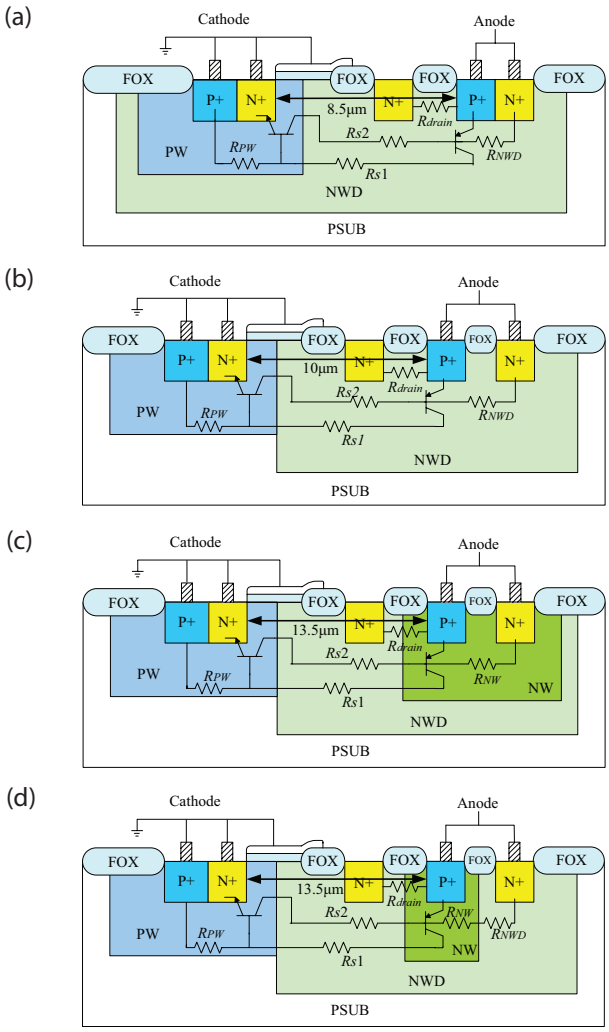

Figure 2: Cross-sectional views of four kind LDNMOS-SCR devices. (a) Type I; (b) type II; (c) type III; (d) type IV.

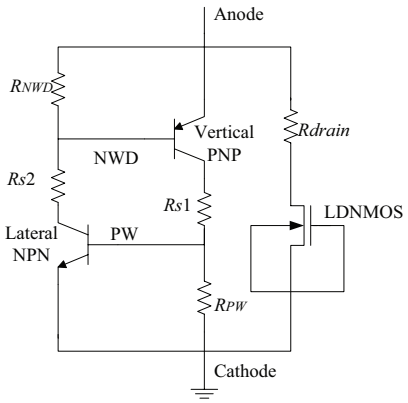

Figure 3: Equivalent circuit of Type I LDNMOS with embedded SCR.

can be triggered into its snapback region earlier. The holding voltages are below 18V, however, they have a relatively high holding current above 800 mA, which ensures the latch-up immunity under ESD stresses in HV applications. Their leakage current is remained at 7~9nA before hard failure, hence, they don't bring considerable impact on the protected core circuit in normal condition.

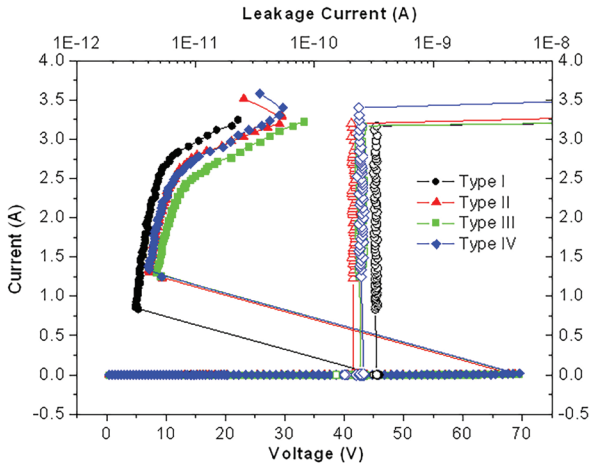

Figure 4: TLP I-V plots for four types LDNMOS embedded SCR with the same device width of 50 μm.

3.1 Trigger characteristics

The trigger voltage of Type I LDNMOS-SCR with its source isolated from PSUB is 45.79V, which is much small-er than that of other three source non-isolated LDNMOS-SCR devices. The different NWD location should take responsibility for the different V_{t1}. A two dimensional (2D) device simulation is performed on a TCAD platform to discover the root cause. Type II is a typical source non-isolated LDNMOS-SCR, whose source is not enveloped by NWD, thus, only Type I and Type II devices are simulated with a 10V voltage applied on their anode electrode. The simulated junction, depletion layer and electric field distribution for those two devices are demonstrated in Figure 5. The red heavy line in the 2D device structure is the edge of depletion layer, the thickness of depletion layer across NWD/PW junction under the poly silicon of Type I is 1.6μm, which is narrower than that of Type II (2.7μm). As the voltage applied on anode is the same, the device with narrower depletion layer will have a stronger electric field. This is proved in Figure 5 that the electric field equal strength line of Type I is denser than that of Type II at this location. Hence, Type I inclines to breakdown more easily than Type II, and a bigger avalanche breakdown voltage is needed for Type II to switch on. Therefore, Type II owns a V_{t1} of 68.78V, which is larger than Type I source isolated LDNMOS-SCR.

Table 1: TLP measured data for conventional GG-LDNMOS and four kind LDNMOS-SCR devices with the same finger width of 50 micrometers.

Device Name	V_{t1}(V)	V_h(V)	I_h(A)	I_{t2} (A)	Efficiency (mA/μm²)	Spacing (μm)
GG-LDNMOS	46.909	8.161	0.907	1.146	0.459	/
Type I	45.794	4.825	0.864	3.169	1.884	8.5
Type II	68.780	7.029	1.332	3.292	2.480	10.0
Type III	69.450	8.368	1.311	3.167	1.735	13.5
Type IV	69.554	7.082	1.379	3.399	2.086	13.5

The DC breakdown voltage (BVD) of the LDNMOS device in the core circuit is 43.5V in our CDMOS technology, and Type I LDNMOS-SCR has the lowest V_{t1} among the four investigated devices, which is only several volts bigger than BVD. And its V_{t1} is closest to the trigger voltage of conventional GG-LDNMOS used for ESD protection at I/O pad. Thus, Type I will be the optimal choice in view of transient V_{t1} measured by TLP.

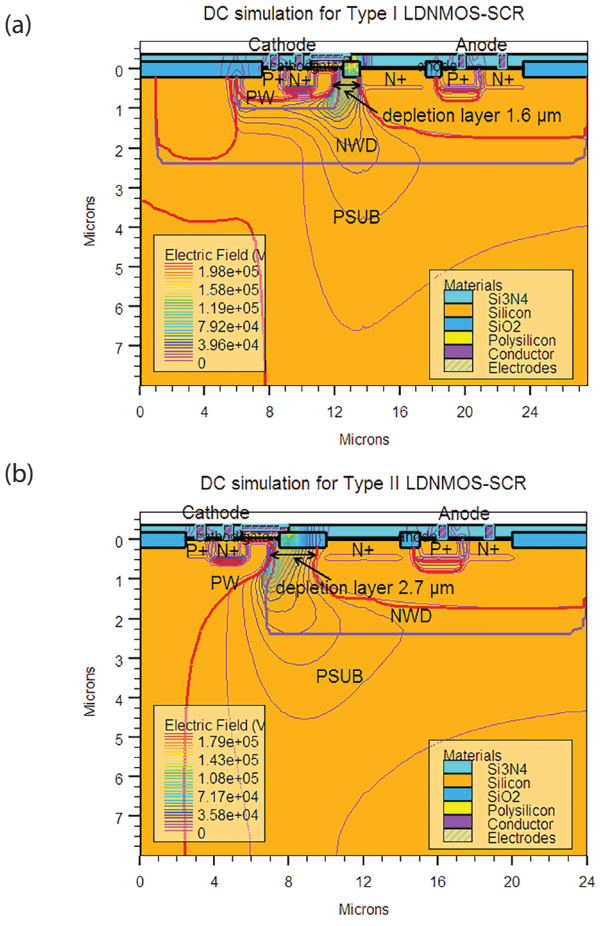

Figure 5: Junction location, depletion layer and electric field (V/cm) distribution in (a) Type I source isolated LDNMOS-SCR and (b) Type II source non-isolated LDNMOS-SCR by DC simulation with anode electrode voltage of 10V.

3.2 Holding characteristics

The V_h of four types LDNMOS-SCR are 4.83V, 7.03V, 8.37V and 7.08V, respectively. The holding voltage difference is result from the anode structure. Formula of V_h can be derived from SCR equivalent schematic in Figure 3,

$$\begin{aligned} V_h &\approx V_{ec-PNP} + (V_{be-NPN} / R_{PW} + I_{be-NPN}) \times R_{s1} + V_{be-NPN} \\ &= V_{ec-PNP} + V_{be-NPN}(1 + R_{s1} / R_{PW}) + I_{be-NPN} \times R_{s1} \\ &= V_{ce-NPN} + V_{be-PNP}(1 + R_{s2} / R_{NWD}) + I_{be-PNP} \times R_{s2} \end{aligned} \quad (1)$$

The spacing between anode P+ and cathode N+ called SCR length of Type I, Type II, Type III, Type IV are 8.5μm, 10μm, 13.5μm and 13.5μm, respectively. The wider the spacing is, the bigger the parasitic resistance R_{s1} and R_{s2} are. And it can be concluded from (e.g. Eq. (1)) that device with bigger R_{s1} and R_{s2} will obtain a lager V_h. Thus, the holding voltage relationship of Type I, Type II, Type III is $V_{h\text{-}Type\ I} < V_{h\text{-}Type\ II} < V_{h\text{-}Type\ III}$. However, there is an exception that Type III and Type IV have the same anode to cathode space, but V_h of Type IV is smaller than that of Type III. This is because the P+ & N+ diffusion regions at the anode of the Type III device are surrounded by NW, so the R_{NWD} in (e.g. Eq. (1)) is replaced by R_{NW}. While the Type IV device is partly replaced by R_{NW}, as only the P+ diffusion area is sur-rounded by the NW. For the doping concentration of NW is higher than NWD, therefore, the RNWD term in (e.g. Eq. (1)) of Type IV device is larger than Type III, so Type IV has a smaller V_h than Type III. It is noted that V_h of all those LDNMOS-SCR devices are below 18V circuit operation voltage, however, the holding current (I_h) of them is all above 800mA, which is big enough for those devices to immune from latch-up at normal operation in HV applica-tions [17-18].

3.3 ESD robustness and turn-on resistance characteristics

Table 1 shows that the second breakdown current I_{t2} of four devices are all above 3A, which is much higher than that of the traditional GG-LDNMOS of 1.146A. Thus, the ESD robustness of LDNMOS is indeed increased by adding a SCR path in it. Among those devices, Type IV has the highest second breakdown current of 3.399A, but for its bigger SCR length (13.5μm), it ocuppies larger chip area. The device has the biggest current discharge effciency is Type II, its current discharge per unit area is 2.48mA/μm², thus, it is an optional device when chip area minimization is taken into consideration.

The on-resistance (R_{on}) of devices is indicated by the slope of their I-V curves after snapback. The R_{on} versus TLP current after snapback and before second breakdown is derived from TLP testing data of those devices and shown in Figure 6. The turn-on resistances differ

from each other for different device structures, Type II & Type IV have the relatively low R_{on}, Type I has the minimum turn-on resistance, which means ESD current is more easily to discharge through it. It is also noted that the device that has a larger holding voltage owns a bigger R_{on}. And it has a trend that R_{on} decreases a little at first, and then increasing apparently as the TLP current growing around ~2.5A. This is because that a bigger current results in a higher lattice temperature, and the carrier mobility will index decrease as the lattice temperature increasing [19]. Thus, R_{on} increases dramatically until the second breakdown occurs.

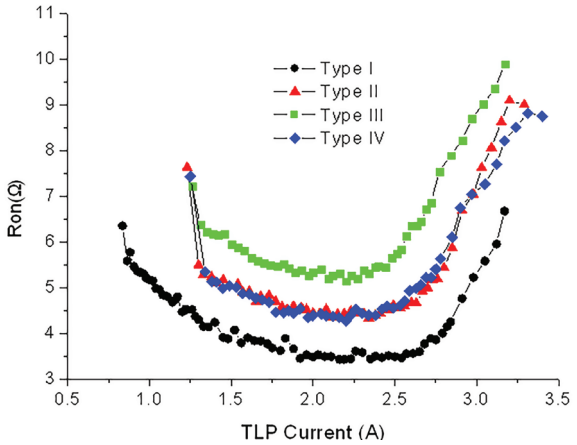

Figure 6: Turn-on resistance Ron of four types LDNMOS-SCR in their snapback region.

4 Conclusions

Four types LDNMOS-SCR ESD protection device have been fabricated in a 0.5μm 18V HV CDMOS process and measured by TLP to examine their ESD windows. The key parameters obtained in TLP I-V curves are compared and discussed.

1) The Type I source isolated device has a lower V_{t1} due to the thinner depletion layer than the non-isolated LDNMOS-SCR. The V_h of the four devices is determined by the anode to cathode SCR spacing and anode structure, and their I_h is big enough to immune from latch-up issue. Further, the second breakdown current I_{t2} of those four devices is much higher than that of traditional GG-LDNMOS, which improve the ESD robustness greatly.

2) From the analysis in section 3, it leads us to conclude that Type I is the appropriate device used for HV 18V ESD protection owning to its low V_{t1} and small R_{on}. Type II will be prior to other two non-isolated LDNMOS-SCR for its high discharge efficiency and relatively low resistance, it can be used to protect circuits with even higher operation voltage.

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6 Conflict of interest

We declare that we do not have any commercial or associative interest that represents a conflict of interest inconnection with the work submitted.

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