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Design and analysis of Low power Rapid Charge Holding Dynamic Latched Comparator

Jaspar Vinitha Sundari Thirunavukkarasu[1], Paramasivam Kuppusamy[2]

[1]Department of Electronics and Communication Engineering, Kumaraguru College of Technology, Coimbatore, Tamil Nadu, India
[2]Department of Electrical and Electronics Engineering, Kumaraguru College of Technology, Coimbatore, Tamil Nadu, India

Abstract: The need for portable devices with high precision has raised the demand for optimization of power and delay in various dynamic comparator topologies. In this paper, an efficient architecture that does timely yet rapid comparison with reduced power dissipation and optimal energy per comparison is proposed. Introducing an extra tail transistor in preamplifier of comparator, assists in holding the high gain, thereby reducing delay as well as power. The latch is meanwhile ready with a minimum threshold value at its output nodes with the help of a pass transistor in between latch output nodes. The conventional, hybrid, and proposed architecture, namely Low power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC) are simulated and verified for power, delay, and energy efficiency in Cadence Virtuoso Spectre. The proposed technique shows a significant improvement in delay and power consumption when compared to conventional comparators. Monte Carlo simulation shows that the proposed technique is robust to the process mismatch, sustaining optimal power, delay and energy efficiency.

Keywords: Average Power consumption, Latch regeneration delay, Hybrid Dynamic Latched Comparator, Rapid Charge holding Latched comparator

Oblikovanje in analiza dinamičnega komparatorja z zapahom z nizko porabo energije in hitrim polnjenjem.

Povzetek: Potreba po prenosnih napravah z visoko natančnostjo je povečala povpraševanje po optimizaciji moči in zamika v različnih dinamičnih topologijah komparatorjev. V članku je predlagana učinkovita arhitektura, ki omogoča pravočasno in hkrati hitro primerjavo z zmanjšano porabo energije. Dodajanje dodatnega repnega tranzistorja v predojačevalnik komparatorja pomaga ohraniti visoko ojačenje, s čimer se zmanjša zakasnitev in poraba energije. Zapah je medtem pripravljen z minimalno mejno vrednostjo na izhodnih vozliščih. Konvencionalna, hibridna in predlagana arhitektura, imenovana Low power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC), je simulirana in preverjena glede moči, zakasnitve in energetske učinkovitosti v Cadence Virtuoso Spectre. Predlagana tehnika kaže znatno izboljšanje zakasnitve in porabe moči v primerjavi s konvencionalnimi komparatorji. Simulacija Monte Carlo kaže, da je predlagana tehnika odporna na neskladje procesov, pri čemer ohranja optimalno moč, zakasnitev in energetsko učinkovitost.

Ključne besede: Povprečna poraba energije, zakasnitev regeneracije zapaha, hibridni dinamični komparator z zapahom, hitro polnjenje

* Corresponding Author's e-mail: jasparvinithasundari.t.ece@kct.ac.in, paramasivam.k.ece@kct.ac.in

1 Introduction

Miniaturization and portability in electronic products are highly demanded in an environment of rapid technological growth. The efficiency of any electronic system is reflected in the individual performance of every subsystem within the product. The efficacy of a comparator is reflected in the efficacy of the whole system and any device that employs it as a subcomponent. The need for high speed, low power and low offset has increased due to the demand for highly precise and fast Analog to Digital Conversion units, Operational Transconductance Amplifiers, voltage references, feedback amplifier setups and many other consumer electronic products. Comparators can be broadly classified into static and dynamic topologies. In general, Static comparators which offers high power consumption and

slow switching during latch regeneration phase are of less priority. In contrast Dynamic comparators are widely preferred since they offer better switching speed and low power consumption through positive feedback. Dynamic comparators are further categorized into single tail and double tail comparators. Single tail dynamic comparators offer optimized delays, notable offset voltage, and high dynamic power consumption. Due to single tail current path, the kickback noise is high. Most preferred parent topology of single tail comparator, namely strong-arm latch is highly influenced by the range of V_{CM} values. An advanced version and alternative to this is the double tail dynamic latched comparator. The double tail dynamic comparators incorporate two tail transistors, weakening the coupling between the preamplifier output and the outputs of the latch. Double tail comparators offer significant reduction in kickback noise due to two separate current paths which further optimize power and delay in its conventional as well as various architectures. Topological changes for power and delay optimization require a preamplifier that not only amplifies the input voltages with enough gain but also that consumes low power by remaining dormant during evaluation phase. Every topological change must ensure that the necessary output swing will be fed to latch at an appropriate time lapse for comparison. Also, the topological changes in latch always aim at a timely comparison of the preamplifier outputs with optimized power intake and less voltage headroom. Most of the comparator topologies fail to either provide a full swing output at an instant when comparison occurs or consumes power during evaluation phase.

The trade-off between power and offset, delay and kickback noise need to be counterbalanced with architectural innovations. Beyond a superseded phase of unending circuit topologies, in alteration to existing CMOS technology, emerging devices like FinFETs, TFETs, Nanosheet transistors, and Nanowires assist in fast switching and low power consumption.

2 Related works

Ata Khorami [1] has proposed a low offset low power comparator that extends full swing output of the first stage for effective comparison. Their proposed preamplifier consumes less power in addition to fast decision making for lower common mode voltages. Also, When V_{CM} values are higher, latch activation becomes complex and influences the delay even though latching process is made easy. Latch topologies that rely on positive feedback, especially sense amplifier type-based latches are usually dependent on common mode voltages despite offering low offset voltages [2]. Savani [3] embedded a pass transistor between the output nodes of latch to sustain the NMOS transistors of the cross connected inverters receive its threshold voltage. Hence the time lapse for the outputs of the preamplifier to discharge is decreased. The time taken for latch initiation is also reduced, resulting in a delay of 51 ps and power consumption of 33 µW. Uneven charging of preamplifier output nodes results in static power consumption, which is avoided in their proposed work by the inclusion of pass transistor in between the output nodes.

One of the vital reasons for kickback noise is the capacitive coupling between the output nodes of the first stage and the input transistors of the second stage. This can be eliminated when the output nodes of preamplifier are cross coupled to pull up pair, which also reduces power dissipation at the time of evaluation phase. A significant delay reduction is achieved by cascading the input transistors and latch of second stage. [4]

To address the kick back noise reduction, yet another modified latch [5] with a wider path resulting in both output nodes in same state is recorded. This architecture cuts off the direct coupling between the outputs of first stage and the inputs of second stage thus resulting in reduced kickback noise with negligible counter effect on delay. Meanwhile, this topology increases the intermediate output nodal resistance thereby significantly reducing the power consumption.

Many architectures show a significant reduction in performance parameters especially power and delay, by modifying conventional preamplifier topologies [6] [7][8], latch topologies [9], adding intermediate stages to minimize noise [10] and few architectures that neglect either of the stages and introducing compensatory combined architectures [11]

Introducing transistors (with specific bias) parallel to latch inputs makes the first stage consume power for only a short period of entire evaluation phase [12]. These architectures are designed for applications where low power is prioritized over speed. Topological improvisations have always demonstrated a trade-off amongst the performance metrics, mostly between power and delay. Using heuristic algorithms, it is validated in [9] that power and CMOS scaling have trade-off with delay and offset, respectively.

Numerous architectures have been proposed to avoid static power consumption in either reset or comparison phase. Whenever extra transistors are introduced to improve comparison speed or minimize power consumption, reduced power generates counter-effects leading to significant rise in delay and vice versa. Notable single stage architecture [14] links the latch through preamplifier currents rather than voltage. It is driven by a clock and a delayed version of the same clock that improves latching speed. Introducing currents to the latch nodes reduces both power and the number of transistors significantly. Delayed clock and specific time sequence can also be achieved by introducing control gates [15].

Most of the recorded literature proves to improve one of the performance metrics compromising the other. The tradeoff between power and delay is seen in most of the comparators where topological changes are

made in either preamplifier or latch. For applications that demand less operating voltage, regenerative type comparators with doubled transistor latch with two fully NMOS / PMOS based preamplifiers are used. This avoids completely charging and discharging of the output nodes of preamplifier reflecting a significant reduction in power concurrently increasing the speed of latch [19].

An effective topology is required to overcome these drawbacks without significant increase in area and counter effects like kickback noise. In this paper, a topology that helps reduce delay and power consumption during nodal charging and discharging of preamplifier as well as latch is proposed. The modified preamplifier and latch in tandem help in avoiding complete charging and discharging of all the output nodes during every clock transition. The proposed comparator has made a noteworthy effort to diminish power consumption by holding the minimum required charge at latch output nodes that negotiates charging and discharging time. Section 3 describes the working of the basic conventional double tail comparator and its transient response. Section 4 describes the working and circuit implementation of the proposed architecture, Low power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC) and its parent architecture, Hybrid Dynamic Latched Comparator HDLC. Section 5 describes the analysis of performance metrics with its sub sections describing the detailed analysis of delay, power and energy efficiency. Subsection 5.1.1 & 5.1.2 includes mathematical analysis of delay of the conventional comparator and proposed comparator respectively. The analysis of performance metrics with V_{CM} and V_{DIFF} is presented in section 5.1.3. Section 6 describes the comparison of the performance metrics of the proposed architecture with existing literature, process corner, influence of transistor sizing ratio, Monte Carlo analysis for various performance parameters, summary of results and key advantages. With progressive simulation results, it can be observed that there is simultaneous improvement in delay and power with minimal trade off. Section 7 concludes the paper.

3 Conventional Double tail Dynamic Latched Comparator

Figure 1 shows the topology of conventional dynamic latched comparator [7], and its transient response can be seen in Figure 2. The comparator works on recharging its intermediate and output nodes during the reset phase and performs the comparison during evaluation phase. No direct coupling of intermediate output nodes to the input terminals in conventional topology makes it more resistant to kickback noise and, this architecture lowers offset voltage. Preamplifier and latch circuits have lesser and larger tail currents respectively, thereby accomplishing lower offset voltage and high speed.

During the precharging phase where the clock is high and the clock bar is low, M_5 remains off thereby ensuring no static power consumption. In the case of the latch circuitry, the pull-down transistors M_{10} and M_{13} fed by clock turn on, forming a path for the output nodes with temporarily available charges to drain to ground. The pull up network M_1 and M_2 of the first stage fed by clock bar, turns on and charges the nodes F_n and F_p to V_{DD}. At the end of precharging phase, the preamplifier output nodes F_n and F_p are at V_{DD} and the latch output nodes out_n and out_p are at ground.
During the decision-making phase, the clock is low, and the clock bar is high. Also, with inputs fed, the tail transistor of the preamplifier turns on creating a path for the output nodes F_n / F_p to discharge.

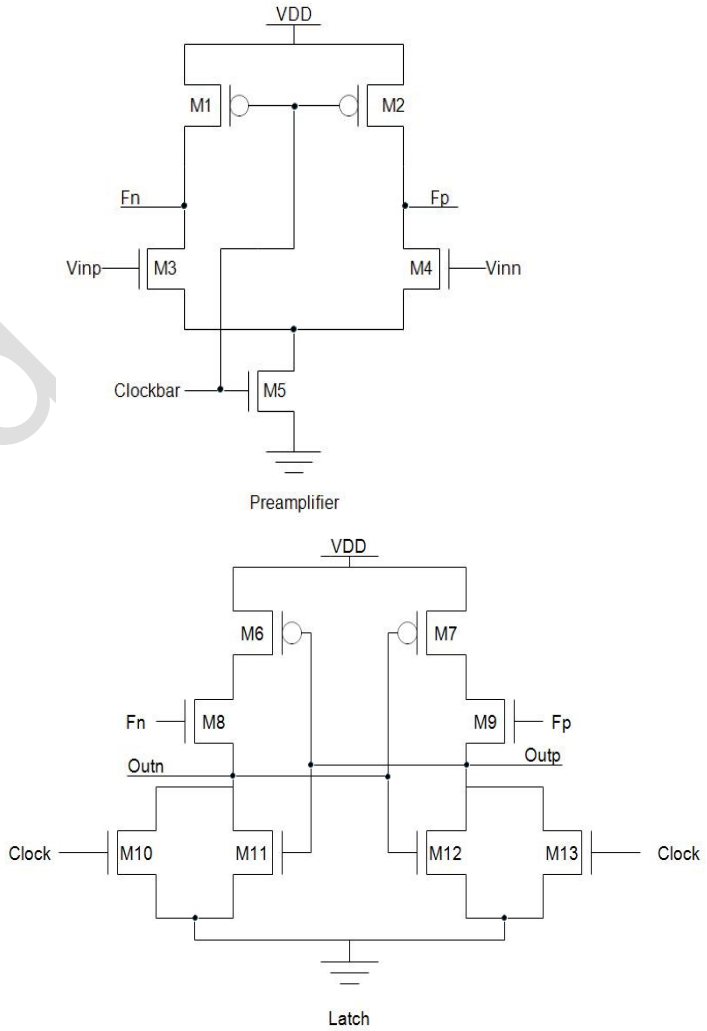


Figure 1: Conventional architecture

Depending upon the ratio of input values, the output nodes discharge with different proportions. For example, when $V_{inp}>V_{inn}$, F_p discharges faster than F_n. Once the charge at the output nodes of the preamplifier reaches the threshold of pull up transistors of latch circuit, latching is initiated. Meanwhile, in the latch circuit, the pull-down transistors M_{10} and M_{13} fed by clock turn off and both the pull-down transistor of cross con-

nected inverter is activated resulting in latching. Latching results in one of the output nodes of the latch pulled high and the other pulled down to zero.

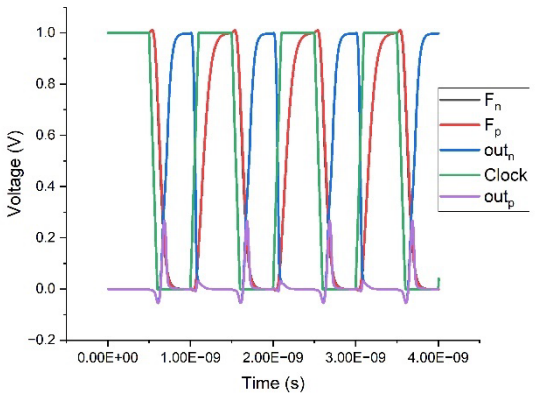


Figure 2: Transient Response of Conventional architecture

4 The proposed comparator

The proposed comparator shown in Figure 3 is the Hybrid Dynamic Latched Comparator (HDLC) combining the principles of shared charge reset [2] and charge sharing techniques [3]. Figure 5 shows the proposed architecture Low-power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC) which is an architectural improvisation from a hybrid dynamic latched comparator architecture (HDLC). The transient response of the hybrid architecture HDLC and proposed LRCHDLC are shown in Figures 4 and 6 respectively.

HDLC aims at effective optimization of power and delay with minimal tradeoff for wider range of V_{CM} and V_{DIFF}. The countereffect recorded in [3] was a high delay during high range of V_{CM} values. Similarly, the counter effect that is witnessed in [2] was high power consumption despite achieving a shorter time lapse for latching. The hybrid architecture is carefully designed with an appropriate choice of transistor sizing and capacitance values. The transient response of this HDLC architecture implemented in 90 nm CMOS technology shows a slight logic degradation in the output voltages. Also, when power and delay were analyzed for wider V_{CM} and V_{DIFF} values, the corresponding architecture offers power as well as delay without much countereffects. This concurrent optimization of power and delay using charge shared preamplifier and shared charge latch is taken as the base for the improvised architecture, LRCHDLC. In LRCHDLC, the concurrent optimization of power and delay is retained with no logical degradation, by shifting of a modified NAND based latch. The charging / discharging path is simplified and channelized smoothly in the proposed architecture, LRCHDLC.

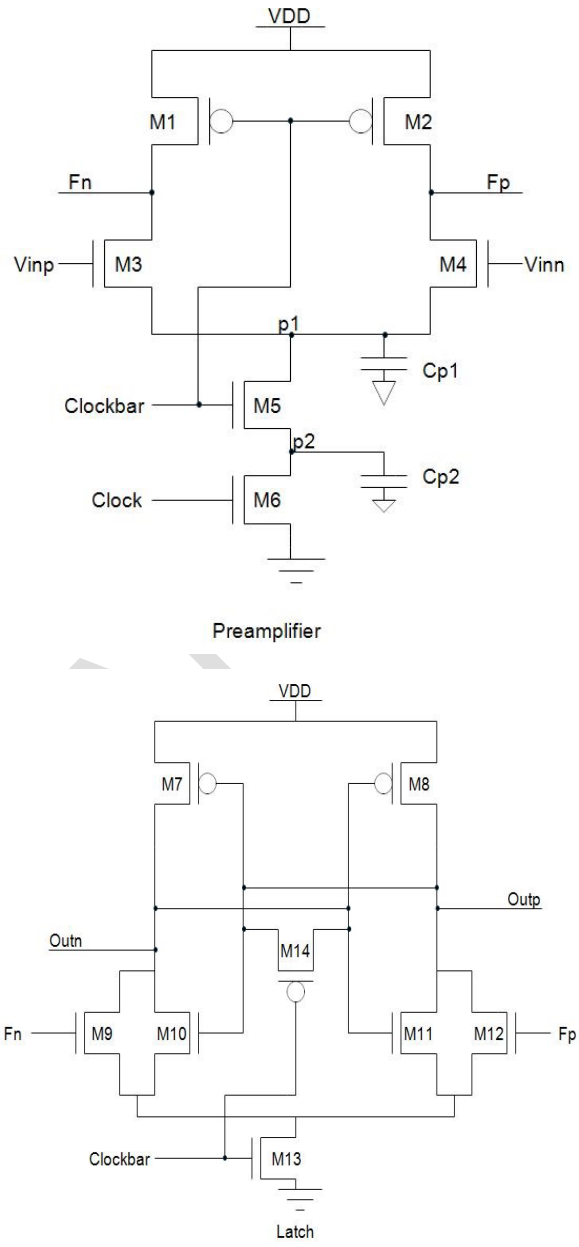


Figure 3: Schematic diagram of HDLC

The topological changes in HDLC have paved the way for further power and delay reduction, whereas switching to NAND based modified latch in LRCHDLC helps in overcoming logical degradation. In both LRCHDLC shown in Figure 5 and its parent architecture HDLC shown in Figure 3, a pass transistor presets both the output nodes, out_p and out_n ,to a minimum threshold voltage (as shown in transient waveform, around 0.5 to 0.6 V for second evaluation phase after charge shared between the nodes through pass transistor) to overcome the time lapse of the nodes to charge and discharge, making the comparison faster. The forementioned factor assures almost similar voltage levels at the latch inputs pulling both the latch outputs to a strong 1 and strong 0 at precise times even though NAND type latches are prone to metastable conditions.

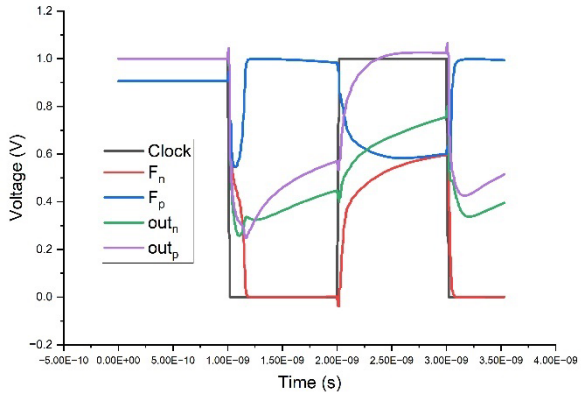


Figure 4: Transient response of HDLC simulated at 45 nm technology with V_{DD}- 1V, F_{clk} – 1 GHz, V_{CM}- 0.7 V and V_{DIFF} – 20 mV

The sustained gain from preamplifier is available exactly at the time instant when comparison happens which is achieved with the help of extra tail transistors with parasitic capacitances C_{P1} and C_{P2} at the drain of M_5 and M_6. The correct outputs are transferred to the latch within an appropriate time frame with less power consumption because of the extra tail transistors in preamplifier.

The reset phase occurs in similar fashion in both HDLC and LRCHDLC architectures. During the reset phase, the clock is high, and the clock bar is low. During this phase the output nodes of preamplifier charges to V_{DD} and only M_6 is active with no parasitic capacitances being charged. These high outputs of preamplifiers are connected to input pull down transistors M_9 and M_{10} of the latch which turns them on. The pass transistor is on through a low clock bar, which distributes the available charges at the output nodes of the latch equally.

During the evaluation phase, the inputs V_{inp} and V_{inn} are given, the clock goes low, and the clock bar goes high. Assuming V_{inp} is greater than Vinn. Thus, the transistors M1 and M_2 go off, unable to sustain the output nodes high, further. The available charge at the output nodes of preamplifier follows the path to discharge via M_3/M_5 and M_4/M_5 charging both C_{P1} and C_{P2}. Since V_{inp} is larger, the node F_n discharges faster than F_p, making the input NMOS transistor of latch circuit, say M_9 go off faster than the other one M_{12}.

In the case of hybrid architecture (HDLC), the tail transistor M_{13} of latch is on since the clock bar is high, thus draining the charge of both out_n and out_p to ground through M_{10} and M_{11}.

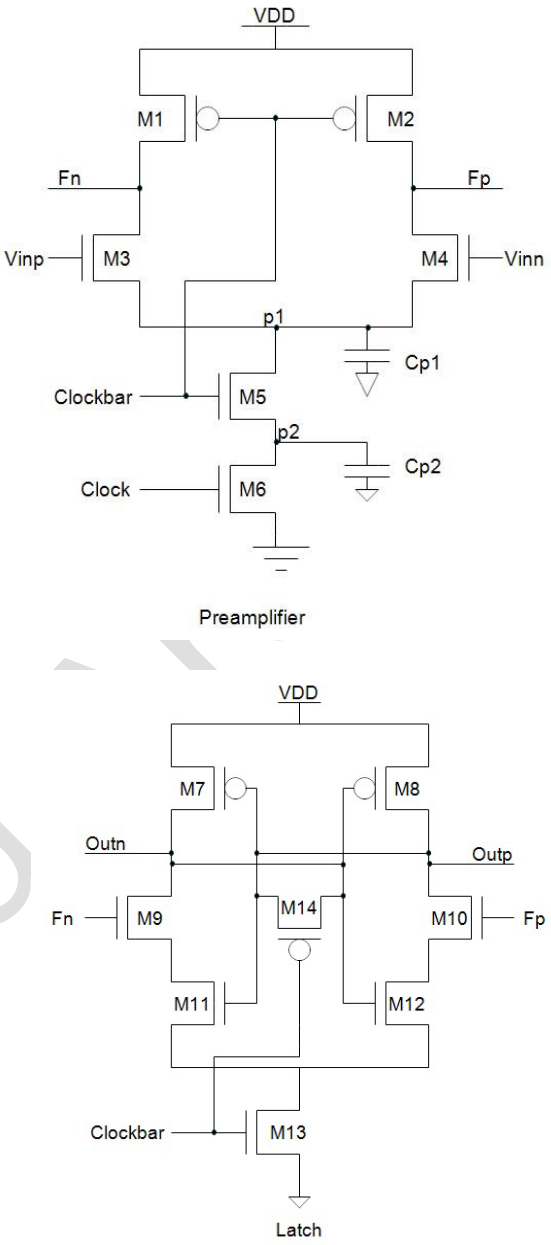


Figure 5: Schematic diagram of LRCHDLC

Similarly, in the case of LRCHDLC, the tail transistor M_{13} is on. Since $V_{inp} > V_{inn}$, the node F_p discharges faster than F_n. The sooner F_p discharges, the sooner it switches M_{10} off. It is significant that the pass transistor is off since the clock bar is high. Hence the already available shared charge at out_n and out_p is around 0.6 V. At this threshold, M_{11} and M_{12} are still in active region. In the short time of F_p falling below the threshold voltage required by M_{10}, there is discharge of out_n through $M_9/M_{11}/M_{13}$. Whereas the out_p still at 0.5 is raised to V_{DD} with regeneration of cross connected inverters.

This effectively reduces power dissipation and shortens the discharge time. Once M_9/M_{10} goes off, the latching begins. The cross connected inverters pull up the node out_n to V_{DD} and pull down the node out_p to zero both in HDLC and LRCHDLC. Also, the availability of output

nodes linked to ground directly in hybrid architecture, makes it dissipate only minimal charge. Hence constant high output is not attained at the end of comparison, which can be observed as a slight decrease from 1 V in the transient response of HDLC in Figure 4. This is overcome in LRCHDLC, which prevents the leakage at the end of comparison, offering a strong 1 as shown in Figure 6.

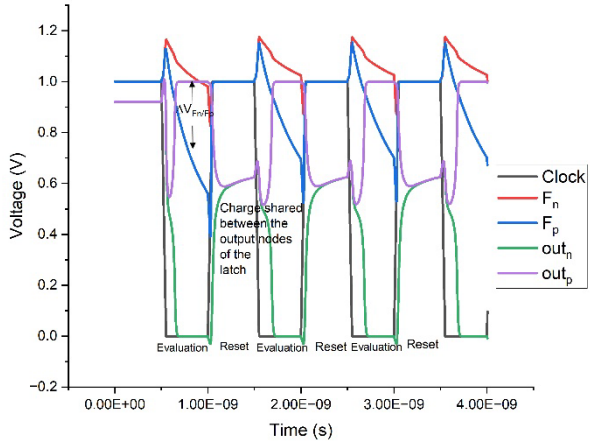


Figure 6: Transient response of LRCHDLC simulated at 45 nm technology with V_{DD}- 1V, F_{clk} – 1 GHz, V_{CM}- 0.7 V and V_{DIFF} – 20 mV

In conventional dynamic comparators, when there is a transition from reset to evaluation phase, the moment the clock changes, the differential discharging of preamplifier outputs is rapid, and the effective differential voltage is channelized into the latch for comparison. The differential voltage deteriorates before serious latching starts. Most of the conventional topologies showcases more power consumption as well as dissipation with notable delay because of this phenomenon. There are few options to overcome this technical challenge to obtain a significant performance.

i) Deactivate the preamplifier when the differential output voltage is high enough for effective latching process.
ii) Preactivated latch when the preamplifier offers maximum differential gain.

Moving the preamplifier into idle state when the output differential voltage is high, thereby sustaining the maximum differential voltage until the latch turns on is the first option. The second option creates the same power during latch activation and the time required for latch initiation remains the same. Also, the differential voltage will eventually go down during the latch initiation period. Prior activation of latch as well as freezing the preamplifier to hold its maximum output differential voltage requires separate clocking and control techniques [20] which will introduce additional power and delay.

Beyond these options, without complex gating techniques or clocking techniques, introducing parasitic capacitance is preferred. Using an extra tail transistor with parasitic capacitances holds the maximum output differential voltage of preamplifier with alternative activation of tail transistors. Proper sizing of both the tail transistors and input transistors with channelized charging of parasitic capacitances guarantee holding of maximum difference gain at the preamplifier outputs. Meanwhile latch activation is also fastened by prior charging of output nodal voltages of latch so that the time taken for latch initiation is neglected. In the conventional comparator, during the evaluation phase the output nodes of preamplifier start discharging and once it goes less than threshold required for input transistors of second stage, the latch gets activated. In the proposed comparator, when the clock moves into a transition for evaluation phase, the preamplifier is ready with maximum differential voltage and latching starts without taking time for initiation thereby significantly reducing power consumption and delay.

The proposed comparator has made significant efforts to reduce power by sustaining the latch output nodal voltages at a minimum voltage which reduces the time lapse of complete discharging down to zero and charging from initial value. In preamplifier, larger input transistors are employed to increase the transconductance which in turn deteriorates the offset voltage [4]. Amongst many topologies that render fast latching process, introducing pass transistor guarantees equal charging at both output nodes in due course reducing power consumption.

5 Analysis of performance metrics

Three performance metrics, namely delay, power and energy efficiency are analyzed for the proposed architecture to prove its suitability for high end applications. Section 5 discusses all the three-performance metrics in detail in the subsections with necessary graphs and mathematical analysis. Section 5.1 discusses the analysis of delay with sub sections discussing the mathematical analysis of delay and influence of input voltage over delay. Section 5.2 and 5.3 discusses the analysis of average power consumption and energy efficiency, respectively.

5.1 Delay

To compare the factors that influence the delay in conventional as well as proposed architectures, detailed derivation of both the architectures is presented in this section.

5.1.1 Delay of Conventional Comparator

The delay associated with conventional double tail dynamic latched comparator architecture comprises two factors, namely t_1 and $t_{latching}$. t_1 is the time taken by the output capacitance to discharge until anyone of the NMOS transistors of the cross connected inverters is on as shown in Eq. (0).

$$t_1 = R_1 C_L \quad (0)$$

The effective resistance R_1 during the discharging of C_L at output nodes can be replaced as ratio of threshold voltage and the drain current of M_{11} or M_{12} as depicted in Eq. (1)

$$t_1 = \frac{C_L V_{thn}}{I_{M11/M12}} \quad (1)$$

where V_{thn} is the threshold voltage of NMOS transistor of cross connected inverter to be on. $I_{M11/M12}$ can also be approximated as half of the tail current of T_3. Hence $I_{M11/M12}$ can be written as shown in Eq. (2)

$$t_1 = \frac{2\,C_L V_{thn}}{I_{tail3}} \quad (2)$$

The second component $t_{latching}$ is the time taken for regeneration to begin which involves the latching process and is given in Eq. (3) as follows

$$t_{latching} = \frac{C_L}{g_{m,eff}} \ln \frac{V_{DD}}{2\Delta V_o} \quad (3)$$

Where ΔV_o is the initial output voltage difference, g_{meff} is the effective transconductance of the latch stage, especially covering transistors that couple the preamplifier and latch stage. C_L is the output load capacitance. The initial output voltage difference can be derived through Eq. (4), Eq. (5), Eq. (6) and Eq. (7).

$$\Delta V_o = I_O R_O \quad (4)$$

The initial output voltage difference can be written as the product of effective resistance Ro and current difference I_o. I_o can be expanded as the product of transconductance g_{m0} and input voltage V_{io} of the corresponding stage. Also, effective resistance Ro can be written as the ratio of output nodal voltage difference $\Delta V_{Fn/Fp}$ in the preamplifier stage and the tail current of second stage.

$$\Delta V_O = g_{mo} V_{io} \frac{\Delta V_{Fn/Fp}}{I_{tail3}} \quad (5)$$

The input voltage V_{io} is the threshold requirement of pull-down transistors of preamplifier and hence replaced as follows in equation (7).

$$\Delta V_o = 2(V_{thn}) g_{mo1,2} \frac{\Delta V_{Fn/Fp}}{I_{tail3}} \quad (6)$$

The preamplifier output nodal difference can be derived as shown in eq. (7) and eq. (8). The resistance is written with time constant equivalent and hence written as the time lapse for discharging C_L.

$$\Delta V_{fn/fp} = \Delta I_{Fn/Fp} R_{o,preamp}$$

$$(7)\ \Delta V_{fn/fp} = \Delta V_{diff} g_{m1,2} \frac{t_1}{C_{L,preamp}}$$

(8)

Substituting eq. (2) in the above eq. (8), the final equation of $\Delta V_{Fn/Fp}$ is given as, $\Delta V_{fn/fp} = \Delta V_{diff} g_{m1,2} \frac{C_L\, 2V_{thn}}{I_{tail3} C_{L,preamp}}$ (9)

The final value of ΔV_o after substituting the preamplifier output nodal difference as

$$\Delta V_o = \frac{4(V_{thn})(V_{thn}) g_{mo1,2} \Delta V_{diff} g_{m1,2}\, C_L}{C_{L,preamp} I_{tail3}^2} \quad (10)$$

The total latching delay can be further obtained as equation (15) by substituting in (4).

$$t_{latching} = \frac{C_L}{g_{m,eff}} \ln V_{DD} \frac{1}{2\Delta V_O}$$

(11)

Which can be rewritten as follows as shown in eq. (14)

$$\frac{C_L}{g_{m,eff}} \ln \frac{V_{DD} C_{L,preamp} I_{tail3}^2}{8(V_{thn}^2) g_{mo1,2} \Delta V_{diff} g_{m1,2} C_L} \quad (14)$$

The total delay for a conventional comparator is derived by adding t_1 and $t_{latching}$ given in eq. (15)

$$T_{total,Conventional} = \frac{2\,C_L\,V_{thn}}{I_{tail3}} + \frac{C_L}{g_{m,eff}} \ln \frac{V_{DD} C_{L,preamp} I_{tail3}^2}{8(V_{thn}^2) g_{mo1,2} \Delta V_{diff} g_{m1,2} C_L} \quad (15)$$

5.1.2 Delay of Low power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC)

For the proposed comparator LRCHDLC, the first component of delay t1 can be derived as shown in eq. (16). In proposed comparator, the necessary threshold is offered by the charge equally shared between the output nodes by the PMOS pass transistor which is represented as V_{DD}- $2V_{tp}$.

$$t_1 = \frac{C_L (V_{DD} - 2V_{tp})}{I_{tail3}}$$

(16)

The second component of total delay, $t_{latching}$ as shown in eq. (3) can be approximated for the proposed comparator as shown below.

To find ΔV_o for the proposed comparator, it is significant to note that the preamplifier, which is equipped with two tail transistors generating only the minimum required tail current for amplification. This necessary tail current helps in sustaining the maximum gain with low power consumption. Figure 7 illustrates the tail currents of transistor M_5 in both the conventional and proposed comparators. The gain can also be increased further and sustained further with a compromise on power consumption. The differential output voltage for the proposed comparator is shown in eq. (17).

$$\Delta V_o = 2\left(V_{DD} - V_{tp}\right) g_{mo1,2} \frac{\Delta V_{Fn/Fp}}{I_{tail3}} \quad (17)$$

The sizing of the tail transistors is chosen in such a way that the preamplifier will offer maximum gain (optimal tail current which will in turn not increase the power) during the initiation of the latch. This helps with effective and fast decisions during the latching phase. The threshold offered by the PMOS pass transistor takes the place of the threshold of NMOS transistor of cross connected latch as shown below in eq. (18). Substituting $\Delta V_{fn/fp}$, the ΔV_o can be expanded as eq. (19).

$$\Delta V_{fn/fp} = \Delta V_{diff} g_{m1,2} \frac{C_L\, 2(V_{DD} - 2V_{tp})}{I_{tail3}(C_{P1} + C_{P2})}$$

(18)

$$\Delta V_o = \frac{2(V_{DD} - V_{tp})(V_{DD} - 2V_{tp})(V_{thn}) g_{mo1,2} \Delta V_{diff} g_{m1,2}\, C_L}{(C_{P1} + C_{P2}) I_{tail3}^2} \quad (19)$$

In proposed comparator, the parameter ΔV_o is not only improved since the capacitance $C_{P1} + C_{P2}$ is lesser when compared to the output capacitance $C_{L,\,preamp}$ in case of conventional comparator. The $t_{latching}$ can now be updated as eq. (19)

$$\frac{C_L}{g_{m,eff}} \ln \frac{V_{DD}(C_{P1}+C_{P2})I_{tail3}^2}{2(V_{DD}-V_{tp})(V_{DD}-2V_{tp})g_{mo1,2}\Delta V_{diff}g_{m1,2}C_L} \quad (19)$$

The total delay for the proposed comparator LRCHDLC is shown in eq. (20)

$$T_{total,Proposed} = \frac{C_L(V_{DD}-2V_{tp})}{I_{tail3}} + \frac{C_L}{g_{m,eff}} \ln \frac{V_{DD}(C_{P1}+C_{P2})I_{tail3}^2}{2(V_{DD}-V_{tp})(V_{DD}-2V_{tp})g_{mo1,2}\Delta V_{diff}g_{m1,2}C_L} \quad (20)$$

Both the discharging of preamplifier output nodes and charging of latch output nodes (to threshold required for latching) is not required in the proposed architecture. Hence the component t_1 as well as $t_{latching}$ is reduced. The transient response of the proposed comparator in Figure 6 depicts the improvement in ΔV_o through change in $\Delta V_{fn/fp}$.

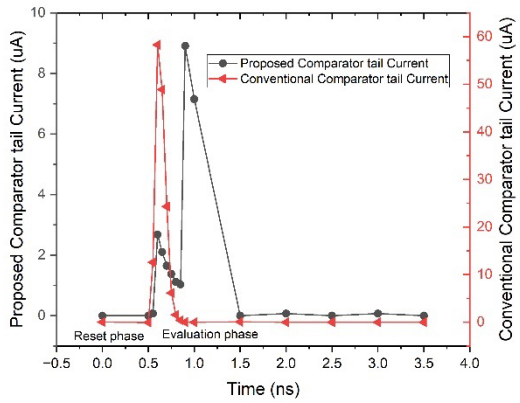


Figure 7: Tail currents of the preamplifier in conventional as well as proposed comparator

With respect to the proposed comparator, the influence of the component t_1 on the total delay is reduced qualitatively. The reason is that the proposed architecture utilizes the internal parasitic capacitances. The load capacitances are replaced by parasitic capacitances $(C_{P1} + C_{P2})$ predominantly to take up the charge from F_n/F_p nodes, rather than C_L. The outcome of t_1 which is latch initiation, is already achieved through pass transistor precharging the out_n/out_p to 0.5 during reset phase itself. Also, the preamplifier with two tail transistors transfers the maximum gain earlier to the latch. Added advantage is that the preamplifier is not actively consuming any power for amplification after the maximum gain is transferred. The need for NMOS threshold is now replaced as the threshold of PMOS Pass transistors since they pull up out_n/out_p to 0.5 or $V_{DD}/2$. There is a major reduction in $t_{latching}$ as the out_n and out_p are already charged up to 0.5 during the reset phase, way before the latching is initiated.

5.1.3 Variation of delay with V_{CM} and V_{DIFF}

A meticulous study of the variation in delay with various factors such as V_{CM}, V_{DIFF} and supply voltage is also presented in this section. A fast-decision-making process is one of the key requirements of high-speed ADC, that can be assured by analyzing the variation of delay with V_{CM} and V_{DIFF}. To determine the robustness and efficiency of the proposed architecture, rigorous and multiple simulations are carried out for a wide range of V_{CM} and $V_{DIFF.}$ The proposed architecture offers consistent range of delay and power even when V_{CM} and V_{DIFF} drops down proving its high sensitivity in decision making during evaluation phase. Simulations were carried out for observing delay at various V_{CM} values (0.5 V to 0.9 V with a step size of 0.1 V) and V_{DIFF} values (10 mV to 100 mV with a step size of 10 mV) on conventional comparator, LRCHDLC (90 nm) and LRCHDLC (45 nm) as shown in Table 1.The conventional comparator records delays ranging from 138 ps to 592 ps for various V_{CM} and V_{DIFF} values, whereas the proposed comparator shows less and consistent delay values, within lower range varying from 26.79 ps to 25.73 ps in case of LRCHDLC using 90 nm technology and from 19.79 ps to 29.09 ps in case of LRCHDLC using 45 nm technology. This implies that in case of proposed comparator, only minimal standard time lapses are taken for charging and discharging at the output nodes of the proposed comparator. Wide varying V_{CM} and V_{DIFF} does not influence the range of delays in the proposed comparator due to minimum t_1 and $t_{latching}$. Figure 8 and 9 shows the transient response of LRCHDLC and conventional architecture at 45 nm for various sets of V_{CM} ranging from 0.5 V to 0.9 V. Figure 10 shows the variations in the output nodal voltages, out_n and out_p in the transient response for various V_{DIFF} ranging from 20 mV to 100 mV with a step size of 20 mV for V_{CM} – 0.7 V. During second evaluation phase, Figure 8 shows that out_p rises first for V_{CM} – 0.5 V first and then it can be observed that it is followed by V_{CM} – 0.6 V upto 0.9 V. Similarly, in Figure 9, out_n rises first for V_{CM} – 0.9 V and then goes down to V_{CM}-0.5 V. In case of conventional comparator, Delay is inversely proportional to V_{CM} and V_{DIFF}. Whereas, in the case of proposed comparators, the delay is directly proportional to V_{CM} and inversely proportional to V_{DIFF}. The mathematical equations for total delay of conventional and proposed comparators are derived in the previous section as seen in Equations (15) and (20) respectively. The initial output voltage difference ΔV_o , which is directly proportional to $\Delta V_{fn/fp}$ is observed to be proportional to the differential voltage, ΔV_{diff} as shown in Equations (5), (6) and (8). From Equation (3), $T_{latching}$ is inversely proportional to ΔV_o proving the indirect proportionality between V_{DIFF} and delay. The reduction of delay with increase in V_{DIFF} can be explained with respect to two factors. The first factor is that when the V_{DIFF} becomes larger, the gain naturally increases, and the topology also supports by transferring maximum gain to the readily precharged latch. Secondly, the charging and discharging time during evaluation phase is well sustained by precharging of output nodes during reset phase itself, which significantly reduces the latching delay, $t_{Latching}$.

Table 1: Analysis of delay for various V_{CM} and V_{DIFF} for conventional (90 nm) and LRCHDLC (90 nm & 45 nm)

V_{DIFF} (mV)	Conventional Comparator V_{CM} (V)					LRCHDLC (90 nm) V_{CM} (V)					LRCHDLC (45 nm) V_{CM} (V)				
	0.9	0.8	0.7	0.6	0.5	0.9	0.8	0.7	0.6	0.5	0.9	0.8	0.7	0.6	0.5
10	179	206	261	404	592	26.79	26.41	26.1	25.92	25.86	19.79	19.51	19.31	19.2	19.13
20	166	190	240	369	584	26.57	26.26	26	25.86	25.83	19.72	19.46	19.28	19.18	19.12
30	158	182	228	346	578	26.37	26.11	25.91	25.81	25.81	19.64	19.41	19.25	19.17	19.12
40	153	175	219	329	572	26.2	25.98	25.84	25.76	25.79	19.57	19.37	19.23	19.15	19.11
50	150	171	212	314	567	26.06	25.85	25.76	25.72	25.78	19.51	19.32	19.2	19.14	19.11
60	147	167	206	301	560	25.91	25.75	25.69	25.68	25.76	19.45	19.29	19.18	19.13	19.1
70	144	163	200	290	554	25.78	25.66	25.63	25.65	25.75	19.39	19.25	19.17	19.12	19.1
80	142	160	195	280	545	25.66	25.58	25.58	25.63	25.74	19.34	19.22	19.15	19.11	19.1
90	140	157	191	270	535	25.55	25.51	25.53	25.61	25.74	19.28	19.19	19.13	19.11	19.09
100	138	154	186	262	521	25.46	25.44	25.48	25.59	25.73	19.25	19.16	19.12	19.1	19.09

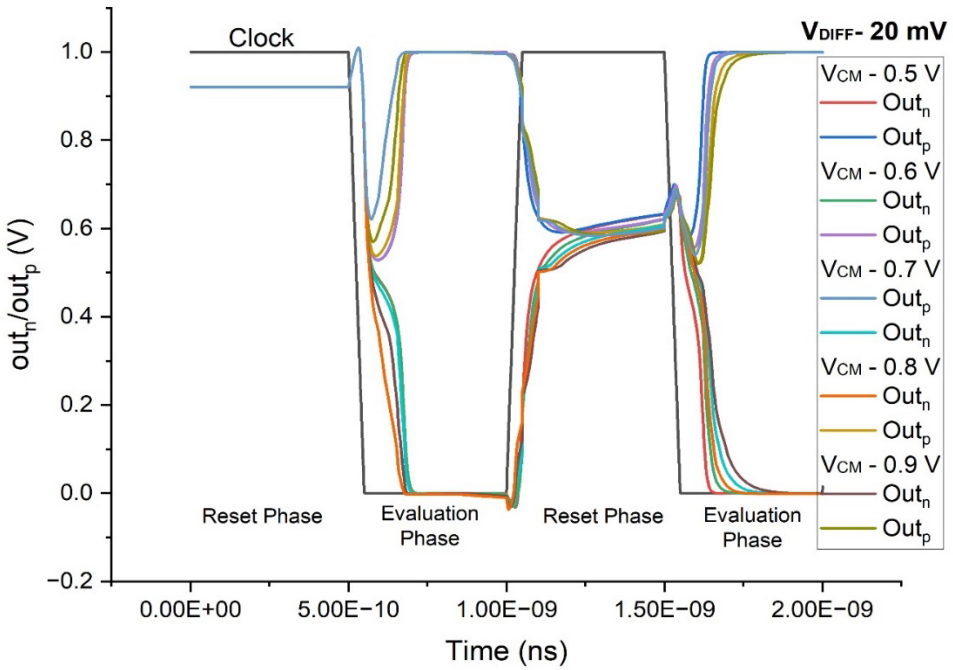


Figure 8: Transient response of LRCHDLC (45 nm) with V_{DIFF} = 20 mV for various V_{CM} values from 0.5 V to 0.9 V

In all conventional dynamic comparator topologies, a lower V_{CM} makes it difficult for the input transistors of preamplifier to switch to linear state for amplification. Also, insufficient gain further slows down the decision-making process. However, the proposed architecture precharges the output nodes out_n and out_p during reset phase, making it easier to proceed to latching phase more easily on time. In LRCHDLC, during the second evaluation phase after charge sharing, the latching time increases with a rise in V_{CM} as seen in Figure 8

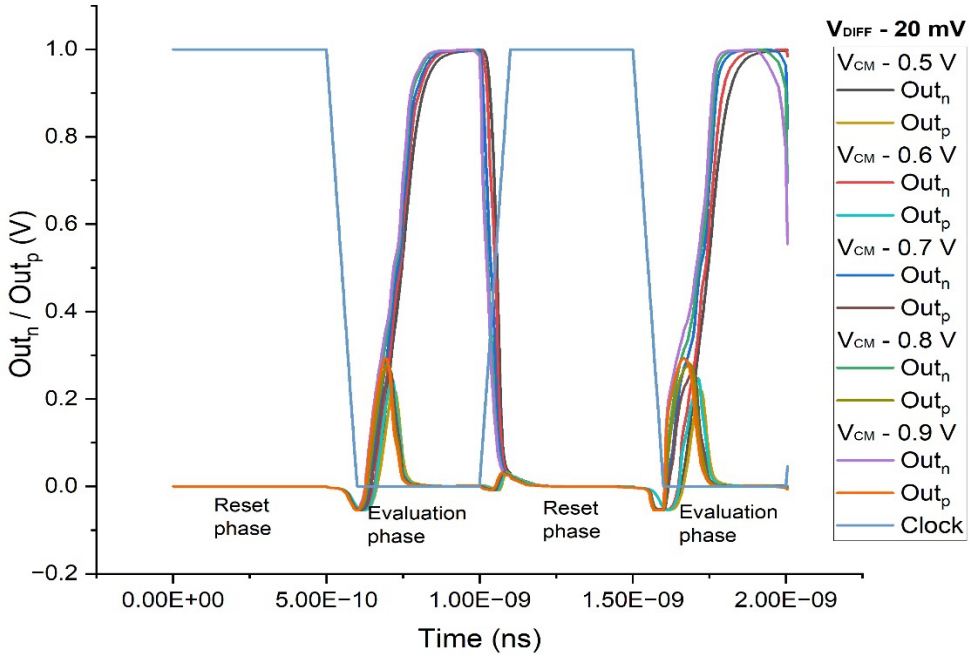


Figure 9: Transient response of Conventional comparator (45 nm) with V_{DIFF} = 20 mV for various V_{CM} values from 0.5 V to 0.9 V

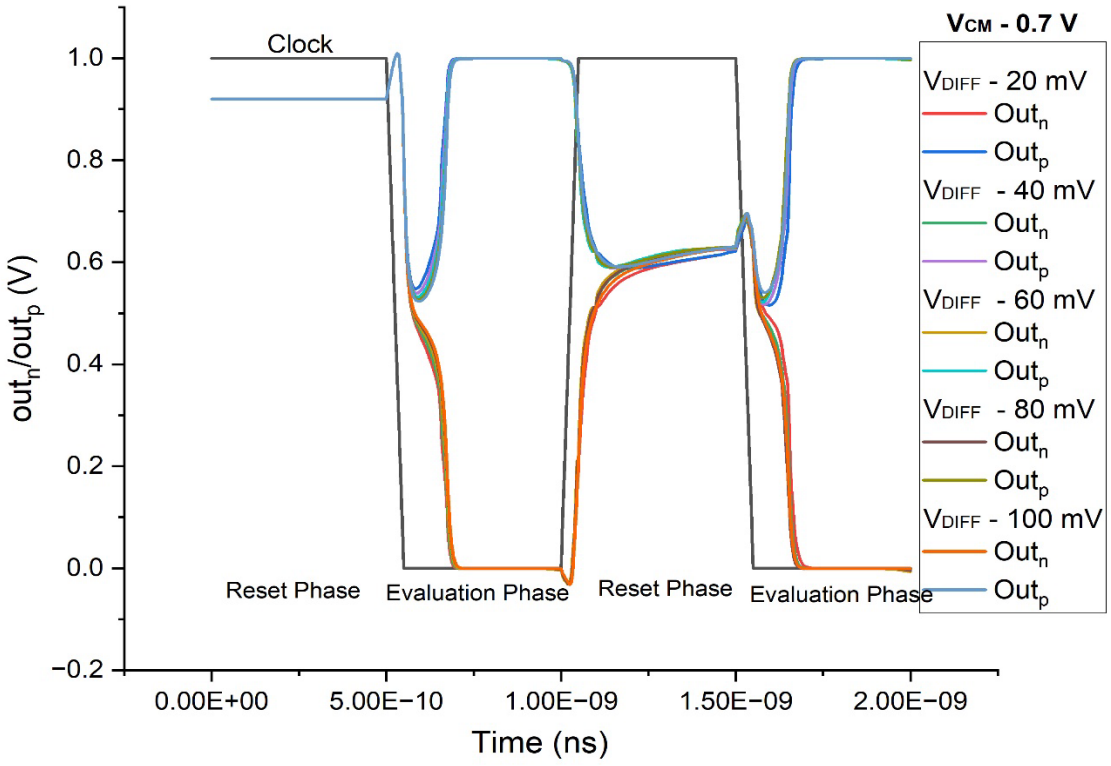


Figure 10: Transient response of LRCHDLC (45 nm) with V_{CM} – 0.7 V for various V_{DIFF} values from 20 mV to 100 mV.

Table 2: Analysis of power consumption for various V_{CM} and V_{DIFF} for conventional (90 nm) and LRCHDLC (90 nm & 45 nm)

	Conventional Comparator (90 nm)					LRCHDLC (90 nm)					LRCHDLC (45 nm)				
V_{DIFF}	V_{CM} (V)					V_{CM} (V)					V_{CM} (V)				
(mV)	0.9	0.8	0.7	0.6	0.5	0.9	0.8	0.7	0.6	0.5	0.9	0.8	0.7	0.6	0.5
10	5.01	4.96	4.91	4.87	4.76	2.62	2.54	2.47	2.4	2.31	1.49	1.32	1.11	0.88	0.69
20	4.94	4.9	4.85	4.81	4.71	2.61	2.53	2.46	2.39	2.3	1.49	1.32	1.1	0.88	0.68
30	4.9	4.86	4.81	4.76	4.67	2.59	2.51	2.44	2.38	2.3	1.5	1.32	1.09	0.87	0.68
40	4.88	4.83	478	4.72	4.64	2.58	2.5	2.44	2.37	2.3	1.5	1.31	1.09	0.86	0.67
50	4.86	4.81	4.75	4.69	4.61	2.57	2.49	2.43	2.37	2.29	1.5	1.31	1.08	0.85	0.67
60	4.84	4.79	4.73	4.66	4.58	2.55	2.48	2.42	2.36	2.29	1.49	1.3	1.07	0.85	0.66
70	4.82	4.77	4.71	4.64	4.56	2.54	2.47	2.41	2.35	2.29	1.49	1.29	1.07	0.84	0.66
80	4.8	4.75	4.69	4.62	4.54	2.54	2.47	2.4	2.34	2.28	1.49	1.29	1.06	0.84	0.65
90	4.79	4.74	4.68	4.6	4.53	2.53	2.46	2.4	2.34	2.28	1.48	1.28	1.05	0.83	0.65
100	4.78	4.72	4.66	4.59	4.51	2.52	2.45	2.39	2.33	2.27	1.48	1.28	1.05	0.83	0.65

Whereas in conventional architecture, Figure 9 shows that the latching time decreases with rise in V_{CM} but results in a larger delay due to the absence of a charge sharing mechanism. Quantitatively, this can also be observed seen in Table 1 where there is a direct proportionality between V_{CM} and delay values. It can be observed from Figure 8 and 9 shows that the decision-making time is larger in the case of conventional architecture, when compared to the proposed architecture, LRCHDLC.

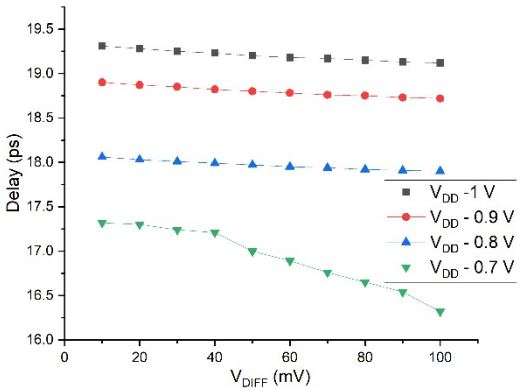


Figure 11: Variation of delay with V_{DD} for V_{CM} -0.7 V and V_{DIFF} – 20 mV, F_{clk} – 1GHz (LRCHDLC – 45 nm)

The delay of the proposed architecture, LRCHDLC (45 nm) is analyzed for various supply voltages ranging from 0.7 V to 1 V as shown in Figure 11. As the supply voltage increases, the charge quantity to be held by the nodes also increases. As per the latching mechanism in the proposed circuit, $t_{latching}$ increases as the minimum charge to be held at the output nodes also increases. The regeneration time required for decision making also proportionally increases. It can be noted from Figure 11 that the proposed architecture offers stable delay irrespective of V_{DIFF} values for V_{DD} values from 1 V to 0.8 V, reassuring the robustness of the proposed architecture.

5.2 Average Power consumption

Analogous to delay, power consumption is also analyzed for the conventional dynamic comparator, LRCHDLC (90 nm), and LRCHDLC (45 nm) with respect to variations in V_{CM} and V_{DIFF}, as shown in Table 2. With respect to average power consumption, conventional architecture reflects a direct proportionality with V_{DIFF} and indirect proportionality with V_{CM}. The significant change in the case of the proposed comparator is that the overall range has dropped to a greater extent, maintaining the same direct proportionality with V_{CM} and indirect proportionality with V_{DIFF}. Power consumption at each instant is measured for two cycles of complete comparison process for both conventional and LRCHDLC simulated at 45 nm technology, as shown in Figure 12.

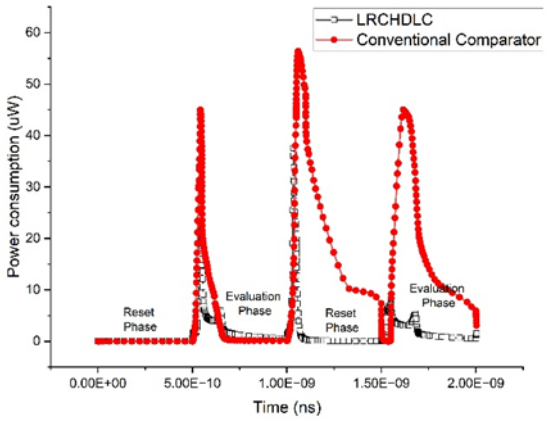


Figure 12: Power consumption of Conventional and proposed comparator, LRCHDLC with V_{DIFF} – 20 mV, V_{CM} – 0.7 V, V_{DD} – 1V at 45 nm technology

In the case of LRCHDLC, the modified preamplifier with two tail transistors limits power dissipation by turning off the preamplifier once maximum gain is transferred. Figures 13 and 14 show power consumption at every

instant of the proposed architecture for various sets of V_{DIFF} and V_{CM} respectively, to observe their influence on the performance. Power consumption during the second evaluation phase shows a significant drop when compared to the evaluation phase before successful charge sharing, ensuring minimal power consumption. Also, the time lapse of active state of preamplifier is less in the case of proposed comparator, thereby offering a regularized power consumption for all wide variations in V_{CM} and V_{DIFF}.

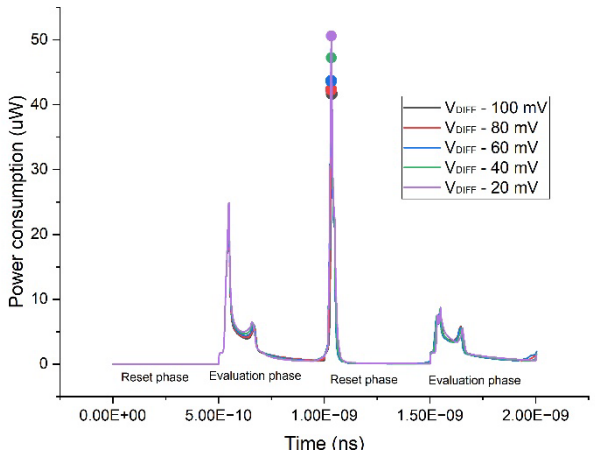


Figure 13: Power consumption of LRCHDLC (45 nm) at every instant for various V_{DIFF} values

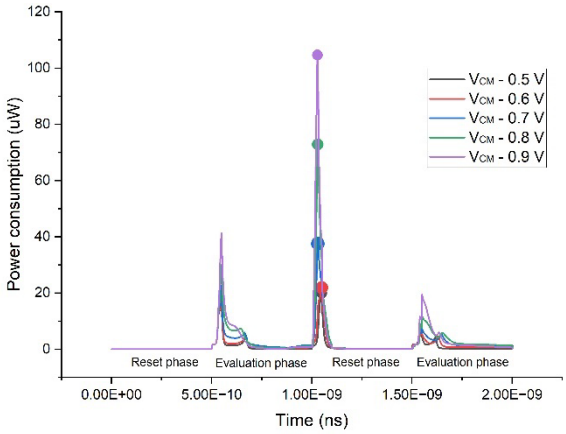


Figure 14: Power consumption of LRCHDLC (45 nm) at very instant for various V_{CM} values

Figures 13 and 14 clearly align with Table 2, proving the direct proportionality with V_{CM} and indirect proportionality with V_{DIFF}. Peak power consumption points are highlighted for various V_{CM} and V_{DIFF} values. The peak power is consumed exactly at the onset of the second reset phase where charge sharing is set to occur. It is highly significant to note that the power consumed during the second evaluation phase is lower than the previous evaluation phase, irrespective of changes in V_{CM} and V_{DIFF}.

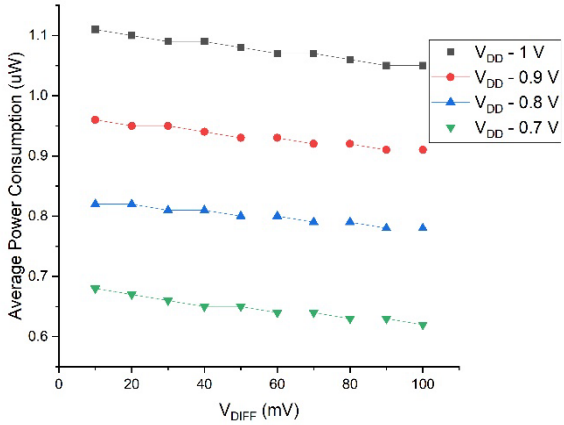


Figure 15: Variation of power consumption with V_{DD} for V_{CM} -0.7 V and V_{DIFF} – 20 mV, F_{clk} – 1GHz

Like delay, average power consumption is analyzed for proposed architecture for various supply voltages ranging from 0.7 V to 1 V as shown in Figure 15. The power consumption of any analog circuit is directly proportional to V_{DD} until there is no major variation in current proportionality due to change in device physics. Both delay and power are highly stable irrespective of V_{DIFF} for V_{DD} values ranging from 1 V to 0.8 V.

5.3 Energy Efficiency

Energy efficiency is a metric that indicates the ability of the comparator to complete a full cycle of reset phase and comparison phase, with minimal power consumption while maintaining maximum accuracy and performance. By integrating the power formulae over a period of two full cycles, energy efficiency is calculated. In the case of proposed comparator, the range of energy efficiency has drastically decreased when compared to the conventional architecture as seen in Table 7.

This can be aligned with the drastic reduction in overall power consumption. This is mainly because complete charging and discharging of output nodes is not required in the proposed architecture, which reduces power and energy efficiency. Because of this charge held at the output nodes of the latch by the pass transistor, significant amount of power dissipated during charging and discharging of latch output nodes at every cycle (reset & evaluation) is reduced and hence there is a reduction in energy spent per comparison. The energy spent for effective comparison is observed varying the supply voltages for proposed architecture, LRCHDLC with V_{CM} – 0.7 V varying the value of V_{DIFF} from 10 to 100 mV, as shown in Figure 16.

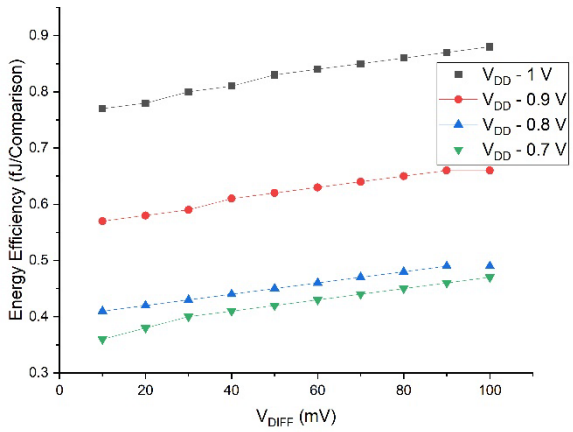


Figure 16: Variation of energy efficiency with V_{DD} for V_{CM} -0.7 V and V_{DIFF} – 20 mV, F_{clk} – 1GHz

The overall range of energy efficiency decreases with a reduction in V_{DD}, but the individual response shows direct proportionality with V_{DIFF}, whereas delay and power show stable responses with V_{DIFF}. This is one of the reasons that as the technology of the proposed comparator goes from 90 nm to 45nm, energy efficiency increases as seen in Table 7.

6 Results and discussion

6.1 Monte Carlo analysis

Monte Carlo simulations were performed for all the performance parameters which in case of hybrid architecture, gives a delay of 56 ps, power consumption of 8.6µW, and energy efficiency of 98 aJ/comparison. For the final proposed architecture, LRCHDLC simulated in 90 nm, Monte Carlo simulation offered better performance parameters such as a delay of 15.32 ps, power consumption of 2.42 µW, and energy efficiency of 37.15 aJ/comparison. When Monte Carlo simulations performed for LRCHDLC at 45 nm CMOS technology, the architecture offered Power consumption of 890.62 nW, an energy efficiency of 1.1 fJ/comparison and delay of 18.67 ps. The mean and standard deviation of the performance metrics say power consumption, delay and energy efficiency for the proposed comparator (both 90 nm and 45 nm technology) are listed in Table 3.

Monte Carlo simulations are carried out to analyze the robustness of the proposed architecture for every mismatch and fabrication errors. Mathematically, it can be proven that the histogram follows a gaussian distribution since 99% of the samples in histogram lie between +3 σ and -3 σ.

Table 3: Mean and standard deviation of performance metrics using Monte Carlo Simulation

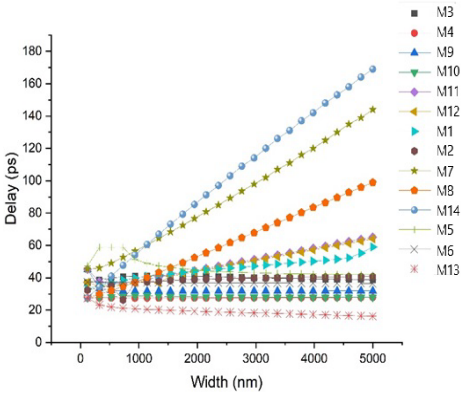
Monte Carlo simulation (N=1000)	Mean	Standard deviation
LRCHDLC at 90 nm technology		
Power consumption	2.42 µW	195.37 nW
Delay	15.32 ps	2.48 ps
Energy efficiency	37.15 aJ	16.09 aJ
LRCHDLC at 45 nm technology		
Power consumption	890.62 nW	23.81 nW
Delay	18.67 ps	1.32 ps
Energy efficiency	-1.11 fJ	53.17 aJ

Also, more than 90% of the samples lie between +2σ and -2σ and 70% of samples in the histogram fall between +1σ and -1σ. The lower standard deviation values in the case of the proposed comparators ensure consistency and reliability of the design. Most of the values fall within +1σ and -1σ in the normal distribution, proving the robustness of the design. Also, the histogram matches the Gaussian curve with slight skewness.

6.2 Influence of transistor sizing ratio on performance

The sizing ratio of the transistors is chosen after wide variation of widths of all transistors to optimize delay and power without causing any logic degradation, thereby ensuring accurate transient response for every comparison. For the proposed architecture LRCHDLC simulated at 45 nm technology, the variation of performance parameters like delay, energy efficiency and power with respect to transistor sizing are depicted in Figures 17, 18 and 19 respectively.

Figure 17: Variation of delay with respect to width of



the transistors in LRCHDLC (45 nm)

Figure 18: Variation of Energy Efficiency with respect to width of the transistors in LRCHDLC (45 nm)

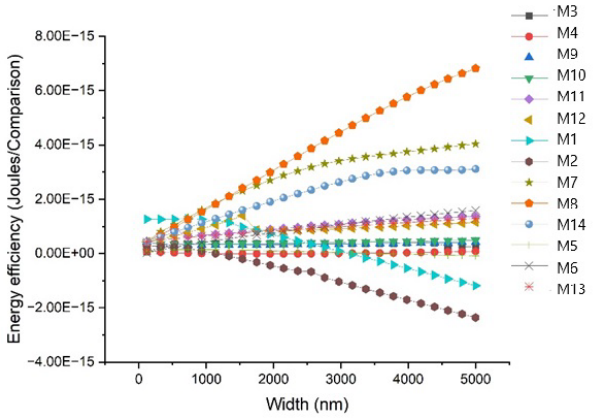


Table 4: Sizing of the transistors used in the proposed architecture, LRCHDLC (45 nm)

Transistors	Width
M1	3µ
M2	1 µ
M3, M4	120n
M5	3.1 µ
M6	1 µ
M7 – M12	120n
M13	300n
M14	120n

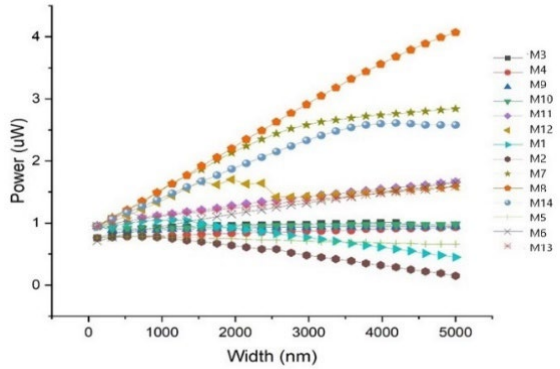


Figure 19: Variation of Power consumption with respect to width of the transistors in LRCHDLC (45 nm)

The sizing of the transistors influences the transconductance thereby causing a major change in power consumption and delay of the circuit. From Figure 17, it is observed that there is a drastic increase in delay when the transistor width increases in the case of pass transistor M_{14} and Pull up transistors M_7 and M_8, ranging up to 160 ps. This influence tends to decrease in the case of the pull-down input transistors of the latch M_9 and M_{10}. The rest of the transistors show stable yet minor variations in the range of 20 ps to 40 ps.

The graph in Figure 18 shows the variation of energy efficiency with respect to transistor width. The pull up transistors of the preamplifier M_1 and M_2 shows a decline in energy efficiency per comparison, whereas the pass transistor M_{14} as well as pull up transistors of the latch M_7 and M_8 shows a significant increase in energy efficiency per comparison. The rest of the transistors show very minor variation in the range of atto joules rather than femto joules from which it can be inferred that the overall range of energy efficiency is narrow and robust to sizing changes. The graphical plot depicted in Figure 19 shows the variation of power with respect to the width of the transistors. The pass transistor M_{14} as well as pull up transistors of the latch M_7 and M_8 offers a notable increase in power consumption up to 4 µW. The intensity of variation is reduced yet minimal rise in power until 2.5 µW is seen when the width of transistors M_{11}, M_{12}, M_5, and M_{13} is increased.

The input pull-down transistors of the preamplifier as well as latch say M_3, M_4, M_9, and M_{10} offer almost constant power consumption in the range of 0.9 nW to 1 µW. On the contrary, the transistors M_5, M_1 and M_2 offer a decline in power when their widths are increased. The transistor sizing used in LRCHDLC (45 nm) is shown in Table 4. It is inferred from simulations and mathematical study that the delay and power solely depend not only on transistor sizing but also on the supply voltage, the input differential voltage, load capacitances used in preamplifier and latch, and the common mode voltage. The transistor sizing impacts the delay by enhancing the effective transconductance of preamplifier and latch input transistors. Inferred from mathematical analysis of delay, the differential voltage ΔV0 is increased in the proposed architecture.

6.3 Summary and Discussion

For proper comparison, the conventional and proposed comparator LRCHDLC are designed in 90 nm as well as 45 nm technology with a clock frequency of 1 GHz for optimized transistor sizing ratios using Cadence Virtuoso Spectre Simulator. Also, process corner variations are analyzed for power, delay, and energy efficiency in case of conventional, hybrid and proposed architectures shown in Table 7. The simulation results in Table 7 are carried out using Cadence Virtuoso Spectre using 90 nm and 45 nm CMOS technology, for V_{DD} =1 V, F_{CLK}=1 GHz, V_{CM} = 0.7 V and V_{DIFF} = 20 mV.

Table 5 shows the comparison of the performance metrics of the proposed architecture with existing architectures from literature. When compared to the existing works in the literature review, the proposed architecture demonstrates a significant reduction in power consumption, energy efficiency and delay without any compromise between each other. Compared to the existing works as seen in Table 5, it is significantly evident that the Power delay product is optimized with optimization in both power and delay rather than increased power with lowered delay or vice versa. The proposed

comparator shows significant improvement in delay and power when compared to conventional architecture, [1], [4], [8], [17], and [21]. Rather than achieving drastic improvement in one of the performance parameters, compromising the other performance metrics, concurrent improvement in power and delay is achieved in the proposed architectures. The trade-off observed between power and delay in the proposed comparator is low when compared to the existing topologies of the literature. Table 6 shows the progressive reduction of power and delay right from conventional architecture to the proposed architecture. The modified preamplifier with an extra tail transistor and latch with pass transistor to hold charge shows a drastic improvement in power consumption, reduced three times when compared to conventional comparator architectures. The drastic reduction in power and delay simultaneously is solely due to the architectural change in latch and the tail transistors in preamplifier that helps in parallel sustaining of charge in output nodes and holding maximum gain in preamplification respectively.

Table 5: Comparison of the proposed work with existing literary works

Ref	[1]	[8]	[4]	[21]	[17]	[2]	Conventional	HDLC	LRCHDLC	LRCHDLC
Technology (nm)	65	90	180	180	90	90	90	**90**	**90**	**45**
Operating frequency (GHz)	5	1	1.5	0.5	0.5	1	1	**1**	**1**	**1**
V_{DD} (V)	1	1	1.8	1.8	1	1	1	**1**	**1**	**1**
Offset voltage(mV)	8	2.44	2.60	2.19	1		-	**-**	**-**	**-**
Power (μW)	73	-	-	347	140.76	32.62	4.8	**6.53**	**2.46**	**1**
Delay (ps)	-	20.95	196.9	-	91.19	-	276	**47**	**26**	**19**
Energy efficiency(fJ)	0.253	8.18	40.45	-	-	32.6	12.61	**0.48**	**0.33**	**0.969**
No of transistors	14	18	19	15	15	14	12	**15**	**15**	**15**
PDP (fJ)	-	-	-	-	12.8	-	0.41	**0.30**	**0.063**	**0.019**

Table 6: Comparison of delay and power of literature and proposed work for V_{CM} = 0.7 V and V_{DIFF} = 20 mV

Technology	Architecture	Delay(ps)	Power(μW)
90 nm	Conventional DTDLC	276	4.83
65 nm	Charge sharing DTDLC [1]	-	73
90 nm	Shared charge reset DTDLC [2]	51	32.62
90 nm	Hybrid DTDLC	47	6.53
90 nm	Low power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC)	26	2.46
45 nm	Low power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC)	19	1

Table 7: Comparison of conventional and proposed architecture with improvisation for V_{CM} =0.7 V V_{DIFF} = 20 mV F_{clk} = 1 GHz for various process corner variations

	Conventional architecture (90 nm)			Hybrid Architecture HDLC (90 nm)			Proposed architecture LRCHDLC (90 nm)			Proposed architecture LRCHDLC (45 nm)		
	Average power (μW)	Delay (ps)	Energy efficiency (fJ)	Average power (μW)	Delay (ps)	Energy efficiency (fJ)	Average power (μW)	Delay (ps)	Energy efficiency (fJ)	Average power (μW)	Delay (ps)	Energy efficiency (fJ)
FF	5.02	130	13.21	8.68	41	0.834	2.65	19	0.581	1.32	14	0.563
SS	4.63	645	11.91	4.99	58	0.250	2.28	36	0.170	0.675	28	1.5
SF	4.60	590	11.91	5.10	43	0.285	2.35	38	0.185	0.888	24	1.2
FS	4.89	192	12.81	8.03	56	0.743	2.55	18	0.536	1.15	14	0.655
TT	4.83	276	12.61	6.53	47	0.480	2.46	26	0.332	1	19	0.969

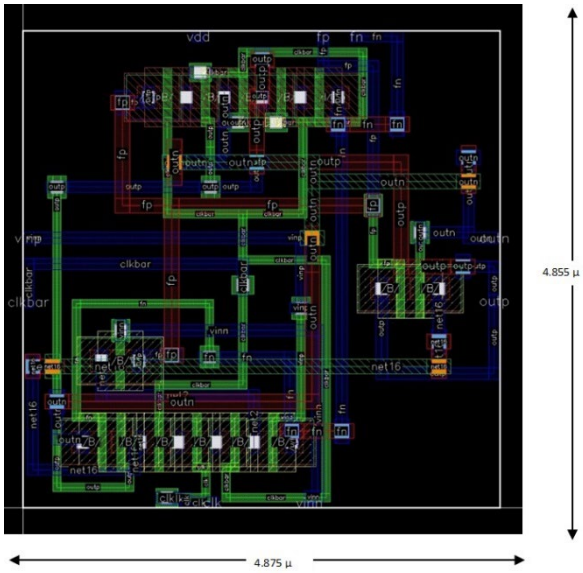


Figure 20: Layout of the proposed architecture, LRCHDLC

The layout of the proposed architecture using 45 nm CMOS technology is shown in Figure 20. The proposed architecture LRCHDLC using 45 nm CMOS technology holds an area of 23.66 μm^2. (4.855 µm * 4.875 µm).

6.4 Key advantages of the proposed architecture

- The power consumption of the proposed topology, LRCHDLC, is reduced by restricting the active duration of the preamplifier and prior precharging of the output nodes of the latch.
- The process of latching starts without waiting for the latch output nodes for charging up to minimum threshold as its already completed in reset phase, thereby reducing the overall time for completing decision making phase.
- Peak differential voltage is sustained by ensuring maximum voltage swing with the help of the additional tail transistor (through nodal parasitic capacitances) in the preamplifier circuit. This helps with accurate decision making and improves the sensitivity of the comparator.
- The proposed architecture achieves concurrent optimization of power and delays using a simplified control phenomena with an additional transistor in both preamplifier and latch, say M6 and M14 respectively.
- The proposed architecture is suitable for Flash ADC which requires high speed and low power consumption, with minimum complexity in clocking and control schemes.

7 Conclusion

This paper demonstrates that the proposed latch stage is more effective in achieving optimized power and delay without any counter mechanisms rising one another parameter. Monte Carlo analysis considering corner and mismatch concludes that the proposed comparator LRCHDLC simulated at 45 nm CMOS technology offers a delay of 18.67 ps, power consumption of 0.890 µW, and an energy efficiency of 1.1fJ/conversion. A thorough simulation study validates the effectiveness of managing the counter effects that arise when there is a rise in power with a delay reduction. When the proposed LRCHDLC (90 nm) is compared to conventional architecture, the delay is reduced by 91%, energy efficiency is reduced by 92%, and the average power consumption is reduced by 49%.

8 Conflict of Interest

The authors declare no conflict of interest.

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