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Memristor based Majority Logic Adders for Error Resilient Image Processing Applications

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Abstract: Approximate Computing (AC) enables energy-efficient and high-performance computation for error-resilient applications such as data analytics, image processing, and multimedia. With the growing demand for low-power, high-density storage in Artificial Intelligence and Machine learning applications, researchers are exploring emerging technologies like FinFETs, memristors, Carbon Nano Tube FET(CNTFET), and Quantum-dot Cellular Automata (QCA) to mitigate the constraints of CMOS scaling. This paper proposes an efficient majority logic design using hybrid memristor-CMOS technology for low-power arithmetic applications. A power-efficient 1-bit adder, comprising three majority gates and one inverter, is designed and compared with existing memristor-based adders. Three Approximate Adder designs such as MAA1, MAA2, and MAA3 are implemented in 8-bit fully approximate ripple carry structure and 8-bit error-tolerant ripple carry structure, integrating four approximate and four accurate adders. Circuit performance, including power and delay, is analyzed using Cadence Virtuoso, where MAA1 achieves the lowest Power-Delay Product (PDP) in both structures. Image quality metrics, assessed using MATLAB with 8-bit pixel depth images, indicate that MAA3 attains the highest Peak Signal-to-Noise Ratio (PSNR) in the fully approximate structure. Error analysis using Verilog coding shows that the proposed MAA2 design achieves a 24.12% error rate reduction in the error-tolerant structure compared to its fully approximate counterpart, demonstrating its efficiency in balancing accuracy and power consumption.

Keywords: memristor, majority logic, approximate computing, image processing, HRTEM image

Memristorski logični večinski seštevalniki za aplikacije za obdelavo slik, odporne proti napakam

Izvleček: Približno računanje (AC) omogoča energetsko učinkovito in visoko zmogljivo računanje za aplikacije, odporne na napake, kot so analiza podatkov, obdelava slik in multimedija. Zaradi naraščajočega povpraševanja po nizkoenergijskem shranjevanju z visoko gostoto v aplikacijah umetne inteligence in strojnega učenja raziskovalci raziskujejo nastajajoče tehnologije, kot so FinFET, memristorji, FET z ogljikovimi nano cevkami (CNTFET) in kvantno-točkovni celični avtomati (QCA), da bi zmanjšali omejitve CMOS-skaliranja. Članek predlaga učinkovit večinski logični dizajn z uporabo hibridne memristor-CMOS tehnologije za nizkoenergijske aritmetične aplikacije. Oblikovan je energijsko učinkovit 1-biten seštevalnik s tremi vrati in inverterjem. Tri zasnove seštevalnikov, kot so MAA1, MAA2 in MAA3, so implementirane v 8-bitno strukturo polne propagacije prenosa in propagacije prenosa tolerantne na napako. Delovanje vezja, vključno z močjo in zakasnitvijo, je analizirano z uporabo Cadence Virtuoso, kjer MAA1 doseže najnižji produkt moči in zakasnitve (PDP) v obeh strukturah. Merila kakovosti slike, ocenjena z uporabo MATLAB-a s slikami z 8-bitno globino pikslov, kažejo, da MAA3 doseže najvišje razmerje med signalom in šumom (PSNR) v polni približni strukturi. Analiza napak z uporabo kodiranja Verilog kaže, da predlagana zasnova MAA2 doseže 24,12-odstotno zmanjšanje stopnje napak v strukturi, tolerantni do napak, v primerjavi s polno približno strukturo, kar dokazuje njeno učinkovitost pri uravnoteženju natančnosti in porabe energije.

Ključne besede: memristor, večinska logika, približno računanje, obdelava slik, HRTEM slika

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1 Introduction

The rapid evolution of Artificial Intelligence and Machine Learning applications, particularly in big data processing, has amplified the demand for high-density storage solutions, driven further by the extensive integration of the Internet of Things (IoT). Efficient handling of these data-intensive tasks necessitates storage technologies characterized by low power consumption, high density, and fast operation speeds. AC has gained recognition as an efficient technique to reduce power and area requirements in arithmetic circuits, making it well-suited for error-resilient tasks such as data analytics, image and video processing, multimedia, and signal processing in communication systems. Unlike conventional computing paradigms that prioritize absolute accuracy, AC architectures emphasize performance and efficiency by allowing controlled imprecision in computations [1].

As conventional CMOS technology approaches its scaling limits, challenges such as leakage current, power dissipation, and reduced switching speed hinder further miniaturization and performance improvements. To address these limitations, alternative nanoelectronic devices such as FinFETs, Ferroelectric FETs (FeFETs), memristors, CNTFETs, and QCA are being explored for advanced logic applications [2]. Among these, memristors, first theorized by L. Chua in 1971 and experimentally proven by HP Labs in 2008, have shown promise in enabling high-density, energy-efficient computing [3]. The HP researchers fabricated nanoscale TiO_2 junction devices with platinum electrodes, demonstrating fast bipolar non-volatile switching. Memristors are made from organic or inorganic materials, with inorganic options such as TiO_2, Ta_2O_5, HfO_2, and ZnO offering high electrical performance, stability, energy efficiency, and CMOS compatibility. In contrast, organic materials, including polymers, graphene oxide derivatives, and biomaterials, exhibit lower performance and reproducibility [4].

Device modeling is essential for developing semiconductor devices, providing accurate insights, optimal designs, and specification compliance [5]. Various models with window functions for memristors have been developed, each optimized for specific applications, balancing accuracy, complexity, and computational efficiency. Among this, SPICE and Verilog-based models like linear ion drift and VTEAM are widely used for their simplicity in circuit-level implementation [6]. Memristive logic designs, advancing VLSI and CMOS scaling, use memristors for logic gates with resistance states representing logic '0' and '1.' IMPLY [7] and MAGIC [8] are key memristive logics, with IMPLY facing high latency and MAGIC suffering with gate connections. Memristor-based design faces challenges like signal degradation, fanout, and sneak-path currents, which hinder performance and scalability. Integrating memristors with CMOS improves logic density and mitigates degradation, particularly in AND, OR, NOR, and NAND gate implementations. Memristor Ratioed Logic (MRL) [9] integrates with CMOS inverters for low-power designs, while Hybrid NMOS-Memristor logic replaces PMOS transistors for efficient NOR logic [10]. In [11], a comprehensive survey on Memristive Threshold Logic (MTL)-based circuits is presented, which forms the foundation for our proposed work.

This research investigates the implementation of majority logic using an experimentally demonstrated memristor. Initially, an Al2O3/HfO2-based memristor device was fabricated, and its structural and electrical properties were thoroughly characterized. High-Resolution Transmission Electron Microscopy (HRTEM) analysis confirmed the correct formation of the device structure. The electrical characteristics, measured using a DC probe station, were subsequently modelled mathematically through Verilog-A coding for integration into circuit simulations within the Cadence Virtuoso environment [12]. A comprehensive description of the process flow and device modelling is provided in Section 7. Further, this paper is structured as follows: Section 2 surveys the preliminary works related to memristor based adders, along with previously implemented approximate adders using both CMOS and emerging technologies. Section 3 presents the experimental details of the proposed memristor. Section 4 details the implementation of memristor-based majority logic. Section 5 explores the design of a 1-bit adder using the majority logic and provides a comparative analysis with existing memristor-based adders. Section 6 introduces and implements majority logic-based approximate adder designs in 8-bit complete approximate and error-tolerant adder structure. Finally, Section 7 discusses the results and performance analysis.

2 Prior Studies

The comprehensive review of memristor-based 1-bit adders are detailed as follows:

A 4T-1M-based XOR gate and a non-volatile full adder using an Ag/AlST/Ta memristor were modelled with a threshold memristor model in 0.35μm CMOS technology. This hybrid memristor-CMOS XOR gate achieves significant area and power reductions, offering a compact, energy-efficient solution. However, issues such as signal degradation in cascading stages and the necessity of CMOS inverters for level restoration remain bottlenecks [13]. The memristor-based MeMOS approach streamlines integration with existing CMOS processes and provides a flexible platform for computational architectures [14]. A Silver-Chalcogenide-based Memristor-CMOS design was introduced for primitive logic blocks and extended to specialized logic structures [15]. In this approach, the memristor is set to its ON state while the NMOS transistor remains open, and a pull-up nanowire resistor controls the charging rate of the load capacitor to maintain proper voltage levels at the node.

Memristor Ratioed Logic (MRL) has been widely employed for designing universal logic gates, including AND, OR, and XOR functions [16]. However, these designs often lack de-

tailed power and delay analysis. A combinational circuit using TiO_2 memristors replaced PMOS transistors with memristors to reduce leakage current and improve speed and energy efficiency, particularly in 180nm CMOS technology. An MRL-based full adder, consisting of XOR, AND, and OR gates along with two inverters, was simulated in 180nm CMOS technology using SPICE, demonstrating potential for reduced area and power consumption [17]. Similarly, a full adder using silver chalcogenide memristors incorporated multifunctional XOR and AND gates, achieving a delay improvement compared to conventional CMOS designs [18]. Additionally, it combines traditional MRL logic with a 1-memristor 1-NMOS (1M1N) design to address output signal amplification issues.

A transistor-free memristor-based full adder employing XOR and OR gates in MRL logic, using 14 memristors and two inverters [19], yielding a simplified design similar to prior MRL based implementations reported in [16]. Further advancements in memristor-based logic include the 1T2M design, which exploits the non-volatile nature of memristors for XOR/XNOR operations, reducing power consumption and circuit complexity while integrating one-bit full adder and comparator functionalities [20]. Additionally, a Y_2O_3-based memristor model was designed to enhance signal integrity and prevent output degradation, though it requires initialization of memristance value for proper operation [21]. A calibrated HfO_2 memristor model was assessed for variability and timing analysis in a full adder circuit [22], while yttrium oxide memristors were employed for low-power logic circuit designs where, the memristor functions as a programmable resistor controlled by an NMOS transistor for enhanced logic performance [23].

A Hybrid Memristor-CMOS (HMC) logic-based adder design, combining transmission gates, MRL-based AND/OR gates, and 1T-1M inverters, demonstrated efficiency through its simple structure and implementation in 32-bit ripple carry adders [24].A TaO_x memristor, modelled with a compact Verilog-A model, demonstrated correct functionality in a 1-bit full adder. Minor glitches from delay mismatches between MRL and CMOS components had minimal impact on performance at 1 MHz frequency [25]. In [26], a full adder implementation using a universal logic circuit improve integration density and reduce power consumption by enabling multiple logic functions within a single structure. The hybrid full adder by combining MRL based AND and OR gates with NMOS-memristor based inverter is proposed in [27].

The preliminary studies related to approximate adders are as follows:

Approximate computing (AC) is applied at various levels, but its most critical use is in circuit design, particularly for arithmetic circuits. This approach intentionally introduces errors to optimize parameters such as power, delay, energy, and area. AC aims to balance performance trade-offs, where reducing transistor count lowers power consumption but increases error rates. Thus, transistor count and error rate remain crucial considerations in circuit design. The Approximate Mirror Adder (AMA) designs are implemented by modifying conventional mirror adder for low complexity digital applications [28]. The CMOS based energy efficient and variation aware Approximate Full Adder (AFA) designs are introduced for imprecision tolerant image processing applications [29]. The Approximate Adder (AA) designs aim to integrate adders and multipliers at the fundamental level of Digital Signal Processor design [30]. Area and power efficient reversible full adders were implemented using GDI logic in [31].

Beyond CMOS-based designs, emerging technologies such as FinFET, CNTFET, QCA, memristors and spintronic devices based approximate adders have been explored. Gate Diffusion Input (GDI) logic implemented using 11nm FinFET technology based approximate adders known as FFA face challenges related to output voltage level degradation [32]. CNTFET-based approximate adders such as GMFA design suffer from non-full swing operation, leading to voltage level degradation [33]. QCA-based majority logic adders have been designed [34] and labelled as PAA, but their practical adoption is hindered by fabrication complexity, temperature sensitivity, defect tolerance, scalability issues, clocking overhead, and high-power dissipation. Spintronic full adders using Magnetic Tunnelling Junctions (MTJs) exhibit high power consumption and delay, though reconfigurable magnetic full adders have been explored to mitigate some of these drawbacks [35, 36]. Additionally, approximate adders and subtractors using memristor-based architectures have been explored, further highlighting the advantages of memristors in logic circuit implementations [37].

Among emerging technologies, memristors have gained significant prominence due to their high compatibility with CMOS transistors, enabling the development of compact and energy-efficient logic circuits.

3 Experimental Section

The fabrication process for the $Pt/Al_2O_3/HfO_2/Ti/TiN$ nanoscale device, outlining the specific materials, deposition techniques, and process parameters used to achieve its precise dimensions and well-defined structure is illustrated in Figure 1. The device was annealed at 400 °C, and the incorporation of a Ti capping layer enables forming-free switching behavior with reduced set and reset voltages. The annealing process, combined with the forming-free nature of the device, contributes to improved uniformity and reduced variability. A detailed analysis of its electrical characteristics is provided in our previous work [38]. HRTEM analysis was employed to examine the morphological and structural properties of the device, confirming the uniformity, interface quality, and thickness consistency of the deposited layers. Additionally, Energy Dispersive Spectroscopy (EDS) mapping, shown in Figure 2. provides a detailed representation of the elemental distribution within the fabricated

device. The observed elemental distribution closely matches the expected outcomes based on the fabrication process flow, confirming the consistency and accuracy of the device fabrication.

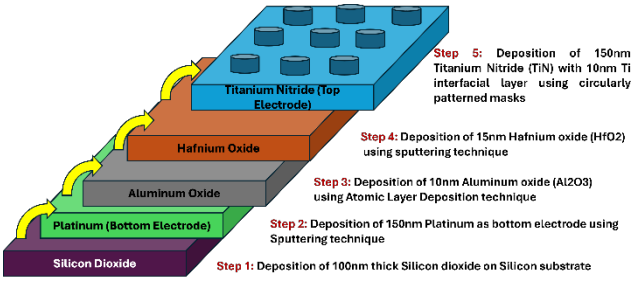


Figure 1. Fabrication process flow of proposed device

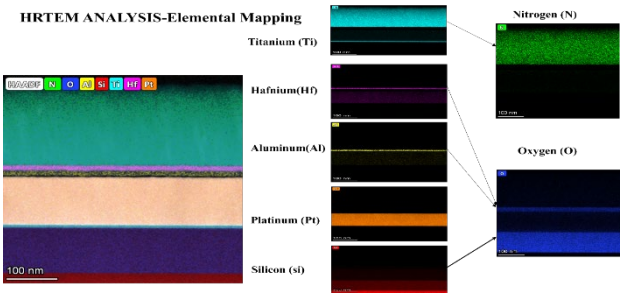


Figure 2. The nanostructure and interfacial morphologies of the proposed Al2O3/HfO2bi-layer RRAM device were investigated using HRTEM.

3.1 Experimental and modelled IV Characteristics

The electrical performance of the fabricated device was rigorously characterized using a DC probe station, enabling precise measurement of key electrical parameters such as resistance states and switching voltages. The mathematical modelling is done using the model [12]. The Table 1. describes the modelling parameters implemented using Verilog-A in Cadence virtuoso environment. The comparison of experimental I-V characteristics and modelled I-V characteristics with a compliance current of 100 µA are illustrated in Figure 3. The memristor device is implemented in Cadence Virtuoso, and its compatibility with CMOS technology is validated through the design and simulation of a memristor–NMOS-based inverter [38]. In this configuration, the proposed memristor functions as a resistive pull-up element, replacing the PMOS transistor. This design maintains acceptable noise margins in the CMOS circuit, as the memristor provides an optimal resistance that results in minimal voltage drop at the output.

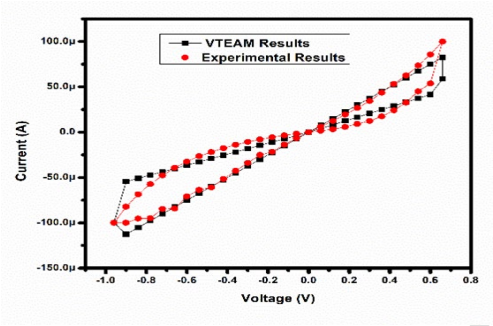


Figure 3. Comparison of Experimental and modelled I-V Characteristics

Table 1. Mathematical Model Parameters

Parameters	Pt/Al2O3/HfO2/Ti/TiN Memristor device
Roff (off-Resistance)	36729
Ron (on-Resistance)	6600
Von(on voltage)	-0.93
Voff (off Voltage)	0.61
Koff (Fitting parameter)	8e-5
Kon(Fitting parameter)	-8e-5
Alphaoff (Fitting parameter)	2.25
Alpha on (Fitting parameter)	3.2

These experimental findings provide valuable insights into the device's behaviour, serving as a foundation for performance optimization and further studies.

4 Memristor Majority Logic (M-ML)

Majority logic is a crucial component in the approximate computing paradigm, and is widely adopted across various emerging technologies, including QCA, ferroelectric devices, spintronic devices, and CNTFETs. In these technologies, majority logic is typically implemented using capacitive or resistive elements, enhancing area and power efficiency. Majority logic is commonly utilized in the design of adders and can be extended to approximate compressors with minimal error distance. These compressors are integral components in multipliers and digital filters, which are used to develop area-efficient image processing architectures with a reduced number of transistors. This reduction in transistor count leads to lower overall power consumption and enables high-speed computing, where minor compromises in accuracy have negligible impact on image quality. However, implementing majority logic in CMOS technology is often area-inefficient due to the requirement of a greater number of transistors.

The M-ML logic circuit is implemented by combining memristors and CMOS inverters as shown in Figure 4. In this design, two inputs A and B, along with a control input, are fed into a CMOS-based inverter Via memristors. When the

control input is set to either 0 or 1, the input voltages at A and B determine the resistances of M1 and M2 memristors respectively. To configure the circuit as a NAND gate, the control input is set to '0' or below the threshold voltage; in this case, the output is logic '1' for all input combinations except when A=B=1, where both memristors conduct and the output becomes logic '0'. Conversely, to operate the circuit as a NOR gate, the control input is set to 1, resulting in an output of logic '0' for all combinations except when A=B=0, where the output is logic '1'.

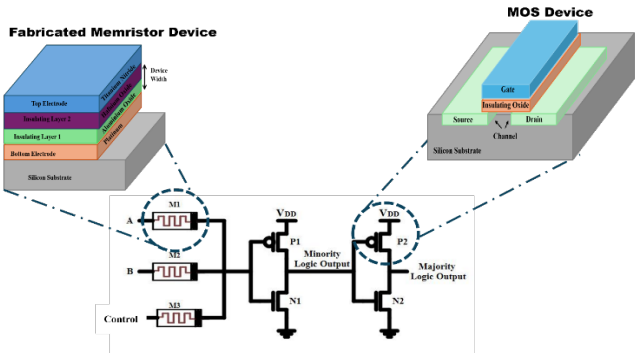


Figure 4. Majority and Minority logic circuit with device structure

Table2. Truth table for majority logic

Inputs			Working condition of transistors		Outputs	
Control	B	A	P1	N1	Minority Logic	Majority Logic
0	0	0	ON	OFF	1	0
0	0	1	ON	OFF	1	0
0	1	0	ON	OFF	1	0
0	1	1	OFF	ON	0	1
1	0	0	ON	OFF	1	0
1	0	1	OFF	ON	0	1
1	1	0	OFF	ON	0	1
1	1	1	OFF	ON	0	1

Additionally, the circuit can be configured to operate as minority logic, where the least frequent input value determines the output. For instance, if A=0, B=1, and the control input is 1, the output is logic '0'. Similarly, the output is '1' for all '0' inputs and '0' for all '1' inputs. When an inverter consisting of transistors P2 and N2 is integrated into the proposed circuit, the resulting configuration implements majority logic, producing the output corresponding to the majority value of the inputs. For instance, when A=B=Control=0, the output is 0. Conversely, when A=B= Control = 1, the majority of the inputs is 1, thus the output is 1. Functionally, the circuit behaves as an AND gate when the Control input is set to 0, and as an OR gate when the Control input is set to 1 as given in Table 2.

5 M-ML Based 1-Bit Adder (M-MLA)

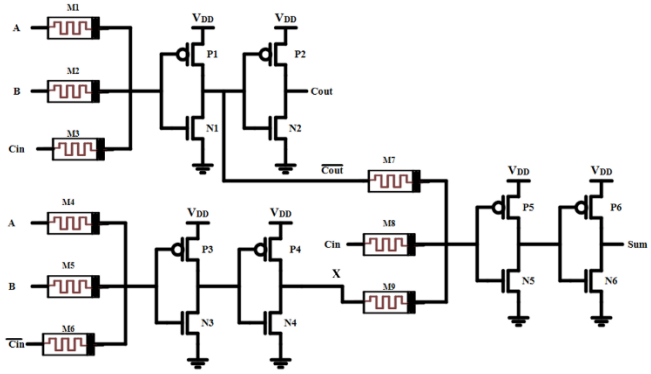


Figure 5. 1-bit Majority Logic based full adder

The proposed M-MLA circuit shown in Figure 5. is designed using majority logic. The carry circuit is constructed with transistors P1-P2, N1-N2 and M1, M2, M3. When Cin=0, the output is A AND B; when Cin=1, the output is A OR B. The sum circuit is realized using transistors P3–P6 and N3– N6. At node X, the circuit generates the output A OR B when Cin=0 and A AND B when Cin=1. The final sum output is derived by using Cin as a control input, with X and Cout' as inputs. The Table 3 illustrates the functionality of the majority logic in generating the sum and carry output.

Table 3. Truth table for output of 1-bit M-MLA

Inputs			Intermediate Inputs			Sum output	Carry Output
Cin'	B	A	Cin	Cout'	X	Maj (Cin,Cout',X)	Maj (A,B,Cin)
1	0	0	0	1	0	0	0
1	0	1	0	1	1	1	0
1	1	0	0	1	1	1	0
1	1	1	0	0	1	0	1
0	0	0	1	1	0	1	0
0	0	1	1	0	0	0	1
0	1	0	1	0	0	0	1
0	1	1	1	0	1	1	1

The M-MLA is simulated in Cadence Virtuoso and compared with other memristor-based adders implemented in 180 nm technology, using the process parameters specified in [23]. The experimental section 3 provides detailed information on the memristor's design parameters, structural configuration, and electrical characteristics for implementing the proposed majority logic in memristor-based architectures.

Table 4. Performance Evaluation of Proposed vs. Existing Memristor based Adders in 180nm Technology

Adder Types	Model Used	Device count	Power	Delay	References
MeMOS logic	TEAM	16T+18M	17.87uW	212.3ps	[14]
MRL Logic	Non-Linear dopant drift	4T+18M	53.08uW	62.4ps	[17]
Hybrid Memristor-NMOS only logic	Analytical	23T+14M	38uW	200ps	[23]
Transmission gate logic with 1T1M inverters and MRL based AND/OR logic	VTEAM	12T+6M	8.2uW	112.7ps	[24]
CMOS logic with MRL logic	Compact	16T+10M	0.615mW	1.78ns	[25]
MRL logic with 1T-1R inverter and CMOS inverter	Non-Linear	14T+12M+2R	121.78uW	62.55ps	[26]
M-ML Logic	VTEAM	14T+9M	4.752uW	218ps	Proposed Logic

*R-Resistors; M-Memristors; T-Transistors

Table 4 provides a comparative analysis of traditional memristor based adders with proposed majority logic adder. The logic circuits reported in [14, 17, 26] employ titanium dioxide (TiO_2)-based memristors, which exhibit set and reset voltages exceeding 1 V and require an electroforming voltage above 2 V. The design presented in [23] utilizes an yttrium oxide (Y_2O_3)-based memristor with relatively high switching voltages of > 4V. Although operated at a 1 V input level, this implementation achieves a power consumption of about 38 µW and a delay of approximately 200 ps. The work in [25] employs a tantalum oxide (TaO_x)-based memristor with a set voltage of 0.7 V, but it still requires an electroforming step. In contrast, the proposed memristor demonstrates a low set voltage of 0.66 V and forming-free operation. A comparison of various mathematical models, as discussed in Section 1, indicates that threshold-based approaches such as TEAM and VTEAM are preferred for their simplicity and ability to capture asymmetric switching behavior, resulting in minimal deviation between experimental and simulated characteristics.

The adders presented in [23] employ 1NMOS-1Memristor-based inverters, where the gate terminal of the transistor in the off state consistently experiences a high output, contingent on the high off-resistance value. MRL logic is utilized exclusively for AND and OR gate implementations and necessitates CMOS-based inverters for other logic circuit implementation [14,17,25]. By modifying MRL logic through the inclusion of a memristor with a control input, a stacked NAND/NOR output is achieved. Additionally, integrating an extra inverter facilitates majority logic implementation. Majority logic exhibits higher power consumption compared to MINI logic [39], but MINI logic is affected by output voltage level degradation. Conversely, post-CMOS majority logic offers high output driving capability and does not require additional buffers or resistors to restore output levels, as indicated in [26]. The proposed post-CMOS majority logic-based memristor adders offer the potential for extending the design towards more complex logic circuit implementations, enhancing their applicability in advanced computing architectures.

6 M-ML Based Approximate Adder (MMA) Designs

The approximate adders are increasingly being utilized for high-density image processing applications, where performance is prioritized over perfect accuracy. Three distinct types of approximate adders are proposed and numbered based on the number of inverters required such as MAA1, MAA2, MAA3 respectively shown in Figure 6(a-c). Table 5 compares the proposed approximate adders with accurate full adders and calculates the error distance (ED) by obtaining the absolute difference between exact and approximate output.

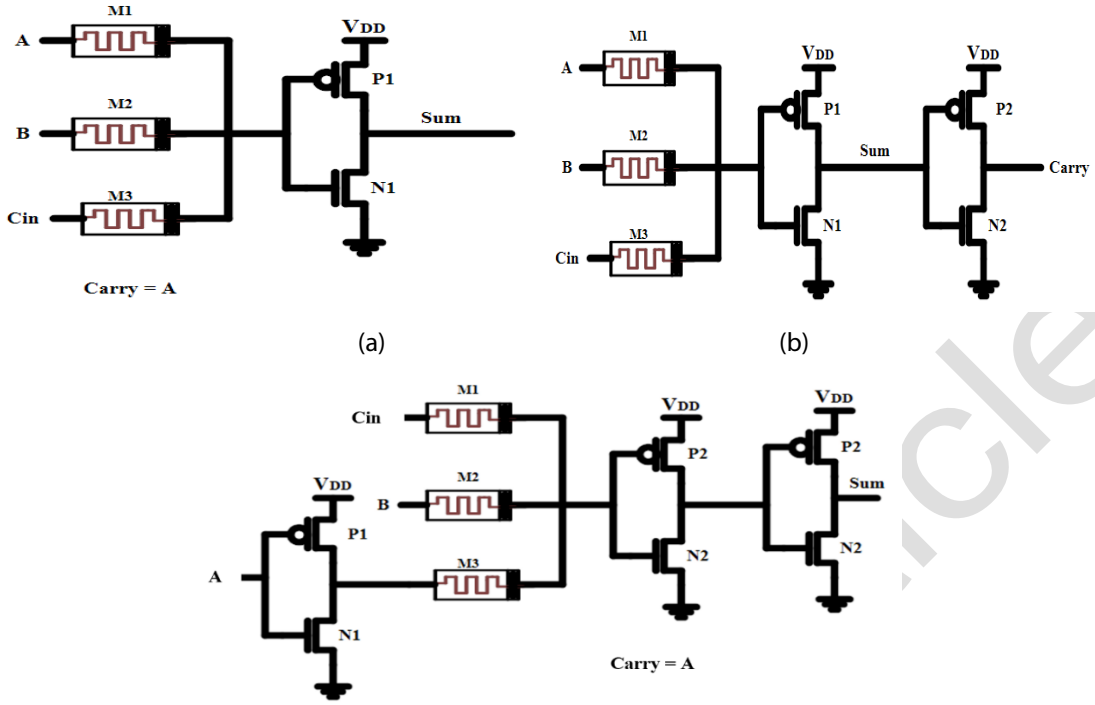


Figure 6. Proposed approximate adder designs (a) MAA1 (b) MAA2 (c) MAA3

Table 5. Truth table of Proposed Majority logic based Approximate adders

Inputs			FA			MAA1			MAA2			MAA3		
a	b	Cin	Carry	Sum	ED	Carry	Sum	ED	Carry	Sum	ED	Carry	Sum	ED
0	0	0	0	0	0	0✓	1×	1	0✓	1×	1	0✓	0✓	0
0	0	1	0	1	0	0✓	1✓	0	0✓	1✓	0	0✓	1✓	0
0	1	0	0	1	0	0✓	1✓	0	0✓	1✓	0	0✓	1✓	0
0	1	1	1	0	0	0×	0✓	2	1✓	0✓	0	0×	1×	1
1	0	0	0	1	0	1×	1✓	2	0✓	1✓	0	1×	0×	1
1	0	1	1	0	0	1✓	0✓	0	1✓	0✓	0	1✓	0✓	0
1	1	0	1	0	0	1✓	0✓	0	1✓	0✓	0	1✓	0✓	0
1	1	1	1	1	0	1✓	0 ×	1	1✓	0 ×	1	1✓	1✓	0

The MAA2 is designed to introduce two errors in the sum output while maintaining an error-free carry output. The carry output, being error-free, is propagated to the next stage, effectively reducing the overall error rate in the adder. This feature makes the MAA2 particularly suitable for applications where minimizing carry propagation errors is essential, such as in arithmetic units of image processing systems. However, due to the nature of the majority logic, the MAA2 may experience a slight degradation in sum accuracy, which is compensated by its error-free carry output.

The MAA1 incorporates two errors in both the sum and carry outputs. It uses one inverter and three memristors, resulting in a smaller area footprint compared to other adder designs. This reduction in area translates directly to lower power consumption and improved speed efficiency, making the MAA1 a suitable candidate for high-performance, power-efficient image processing applications. This efficiency comes at the cost of increased image quality degradation compared to the MAA2, as the additional errors in both sum and carry outputs contribute to more significant distortion in the processed image.

The MAA3 is designed using 3 memristors and 3 inverters. It introduces two errors at the sum and carry output for same combinations of inputs.

6.1 Comparison of 1-bit approximate adders

Tables 6 and 7 present the outputs of approximate adders along with the corresponding error distance (ED) for conventional CMOS logic and emerging logic technologies, respectively.

The ED is calculated using eq. (1). The error rate (ER) quantifies the percentage of ED occurrences relative to the total possible input combinations as shown in eq. (2). The normalized mean error distance (NMED) is computed for each approximate output by dividing the ED by the total number of inputs as shown in eq. (3).

The error metrics for approximate adders are evaluated using the parameters formulated as follows:

$$ED_i = |Exact_{Output_i} - Approximate_{Output_i}| \quad (1)$$

$$ER = \frac{Number\ of\ Erroneos\ Outputs}{n} \times 100 \quad (2)$$

$$NMED = \frac{1}{n} \sum_{i=1}^{n} \frac{|Exact_{Output_i} - Approximate_{Output_i}|}{Exact_{Output_{max}}} \quad (3)$$

Table 6. CMOS Logic based Approximate adders

Inputs			FA	AMA1	AMA2	AMA3	AMA4	AFA1	AFA2	AFA3	AA2	AA4
a	b	Cin	CS	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)
0	0	0	00	00	01(1)	01(1)	00	01(1)	00	00	00	00
0	0	1	01	01	01	01	01	01	00(1)	00(1)	01	01
0	1	0	01	10(1)	01	10(1)	00(1)	01	01	01	01	01
0	1	1	10	10	10	10	01(1)	01(1)	11(1)	01(1)	10	01(1)
1	0	0	01	00(1)	01	01	10(1)	01	01	01	10(1)	10(1)
1	0	1	10	10	10	10	10	10	11(1)	11(1)	10	10
1	1	0	10	10	10	10	10	10	11(1)	11(1)	10	10
1	1	1	11	11	10(1)	10(1)	11	10(1)	11	11	10(1)	11

Table 7. GDI Logic and emerging logic based Approximate adders

Inputs			FFA2	FFA3	GMFA	MFA	PAA1	PAA2
A	b	Cin	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)
0	0	0	00	00	01(1)	00	00	01(1)
0	0	1	01	01	00(1)	11(2)	01	00(1)
0	1	0	01	01	00(1)	00(1)	00(1)	01
0	1	1	01(1)	00(2)	10	11(1)	11(1)	10
1	0	0	00(1)	00(1)	01	00(1)	00(1)	01
1	0	1	11(1)	11(1)	10	00(2)	11(1)	10
1	1	0	10	10	10	10	10	11(1)
1	1	1	11	11	10(1)	11	11	10(1)

*ED-Error Distance, C-carry output, S-Sum output

Table 8. Error Metric Analysis of Approximate adders

Approximate adder	Sum Equation	Carry Equation	Number of Errors	DC	ER (%)	NMED
AMA1 [28]	$\bar{A}.\bar{B}.Cin + ABCin$	$B + A.Cin$	2	20	25	0.083

AMA2 [28]	$\overline{Cin}.(\bar{A}+\bar{B})+(\overline{A}.\bar{B})$	$A.B+B.Cin+A.Cin$	2	16	25	0.083
AMA3 [28]	$\overline{B+(A.Cin)}$	$B+(A.Cin)$	3	13	37.5	0.125
AMA4 [28]	$Cin.(\bar{A}+B)$	A	3	15	37.5	0.125
AFA1 [29]	$\overline{A.(B+Cin)}$	$A.(B+Cin)$	3	8	37.5	0.125
AFA2 [29]	$A+B$	$Cin.(A+B)+A.B$	4	18	50	0.167
AFA3 [29]	$A+B$	$A.(B+Cin)$	4	14	50	0.167
AA2 [30]	$\overline{(BCin+\bar{B}.\overline{Cin})+A}$	$A+(B.Cin)$	2	20	25	0.083
AA4 [30]	$Cin.\overline{(A\oplus B)}+B(A\oplus B)$	A	2	14	25	0.083
FFA2 [32]	$(\bar{A}.B+Cin)$	$A.(B+\bar{B}.Cin)$	3	10	37.5	0.125
FFA3 [32]	$(\bar{A}.B\oplus Cin)$	$A.(B+\bar{B}.Cin)$	3	12	37.5	0.125
GMFA [33]	$\overline{B+Cin}$	$\bar{A}.B.Cin+A.(B+Cin)$	4	8	50	0.167
MFA [37]	$\bar{A}.\bar{B}.Cin+\bar{A}.B.\overline{Cin}+A.\bar{B}.\overline{Cin}+A.B.Cin$	$\bar{A}.B.Cin+A.\bar{B}.Cin+A.B.\overline{Cin}$	5	10M+6T	62.5	0.208
PAA1 [34]	Cin	$Maj(A,B,Cin)$	4	3M+2T	50	0.167
PAA2 [34]	$\overline{Cin}$	$Maj(A,B,Cin)$	4	3M+6T	50	0.167
MAA1	$Min(A,B,Cin)$	A	4	3M+2T	50	0.167
MAA2	$Min(A,B,Cin)$	$Maj(A,B,Cin)$	2	3M+4T	25	0.083
MAA3	$Maj(\bar{A},B,Cin)$	A	2	3M+6T	25	0.083

Table 8 outlines the logic equations for 1-bit existing approximate adders, detailing the number of errors, Device Count (DC), ER and NMED. The memristor-based approximate adder (MFA) exhibits a high error rate of 62.5%, with five errors exceeding the 50% threshold. Adders with an error rate of ≤ 50% have been selected for the implementation of 8-bit approximate adder architectures. Furthermore, the PAA1 and PAA2 adders, originally designed in QCA technology, have been re-simulated utilizing the proposed memristor-based majority logic to ensure a fair comparative analysis.

7 Performance Analysis of 8-bit Approximate Adders

This section investigates the effects of seventeen approximate full adders, as described in Table 8, by implementing them within 8-bit Ripple Carry Adder (RCA) structures. Two types of memristor-based approximate adder architectures have been designed: the 8-bit Memristor-based Complete Approximate Adder (MCAA), which utilizes approximate adders for all eight bits, as illustrated in Figure 7 (a), and the 8-bit Memristor-based Error-Tolerant Adder (META), which employs a hybrid approach. In the META design, the least significant 4 bits (LSBs) are implemented using approximate adders, while the most significant 4 bits (MSBs) utilize exact adders based on majority logic for PAA's and MAA's and CMOS based conventional full adder for other approximate adders, as shown in Figure 7 (b).

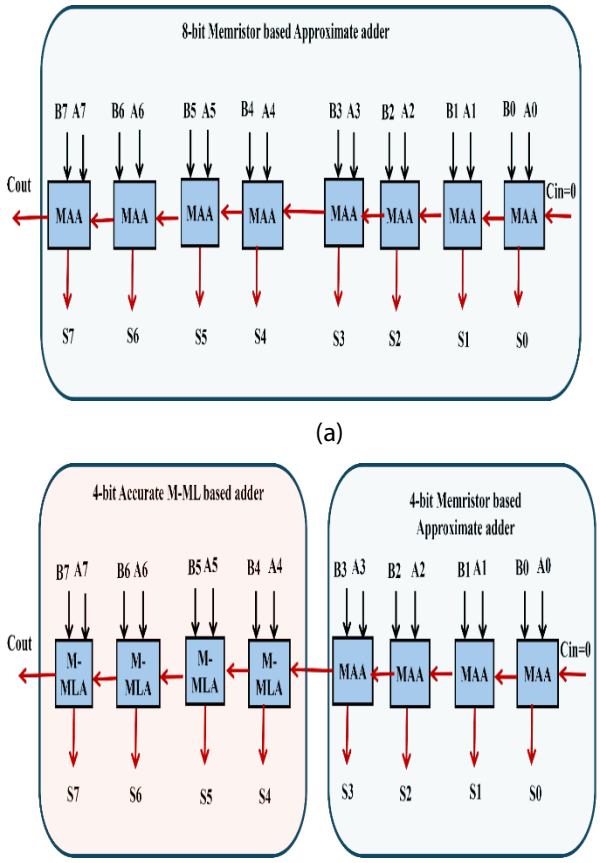


Figure 7. Block diagram of 8-Bit Memristor based (a) Complete Approximate Adder (MCAA) (b) Error Tolerant adder (META)

7.1 Circuit metrics of 8-bit Approximate Adders

The 1-bit adder structure were simulated at a frequency of 100 MHz, with power and delay metrics extracted for comparative analysis. The performance of the 1-bit adders were evaluated in the context of 8-bit META and 8-bit MCAA architectures. The FFA and GMFA, implemented using Gate Diffusion Input (GDI) logic, exhibit non-full-swing voltage output characteristics. Instead of achieving the expected 1V VDD output level, an output voltage of 0.702V was obtained, with some instances producing VDD/2. While this voltage level remains above the noise margin, the output driving capability for ripple-based structures is significantly reduced. The comparative analysis of DC, power consumption, and delay is presented in Figure 8(a-c).

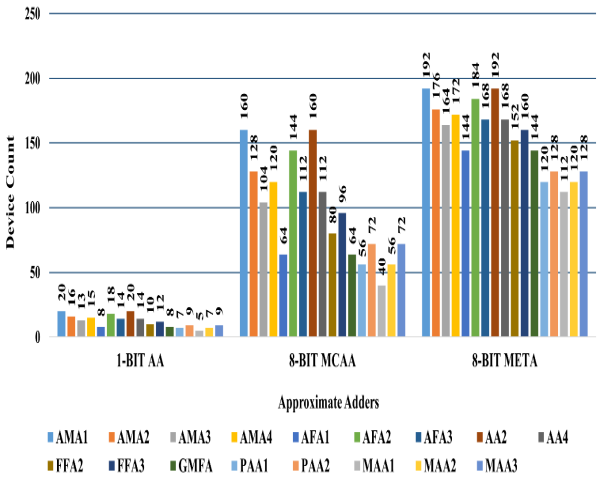
The MAA1 adder is designed with a minimal DC, utilizing only three memristors and two transistors. In contrast, the AMA1 and AA2 adders incur significant area overhead due to their reliance on 20 transistors. The AFA1 and GMFA architectures exhibit area efficiency comparable to MAA-based designs within the 8-bit MCAA configuration. However, in error-tolerant 8-bit META architectures, the DC increases. Notably, the MAA1 requires only 5 DC, achieving a reduction of 41.67% and 75% compared to AMA1 and AA2 in 8-bit META and MCAA structures, respectively. Moreover, conventional adders such as AMA and AA, as well as most AFA designs except AFA1, implemented using standard CMOS logic, require a significantly higher DC compared to emerging logic-based approximate adders, resulting in increased area and power consumption.

Power analysis reveal that MAA1 exhibit better power efficiency compared to all evaluated cases. Within the 8-bit MCAA configuration, GMFA consume less power than MAA3 and AFA1 due to its non-full-swing output characteristics. The delay analysis is calculated for the longest propagation path, where the sum output exhibits the highest delay in most approximate adders. However, in architectures such as PAA, FFA, and AFA, the carry output experienced the highest delay. Among the evaluated circuits, AMA1 and AA2 demonstrate the highest worst-case delay. Additionally, GDI logic-based approximate adders exhibit increased delay compared to MAA-based designs.

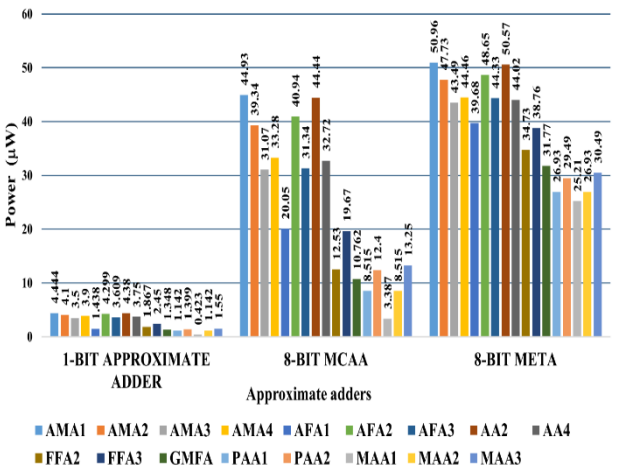
The PDP analysis for the 1-bit adder, as illustrated in Figure 9(a), includes a Conventional Full Adder (CFA) implemented using CMOS transistors. The CFA exhibits a power consumption of 5.771 µW and a delay of 0.289 ns. Additionally, the power and delay characteristics of the Majority Full Adder (MFA) are presented in Table 4. The Power-Delay-Area-Product (PDAP) analysis is done by calculating

$$\boldsymbol{PDAP = PDP \times DC}$$

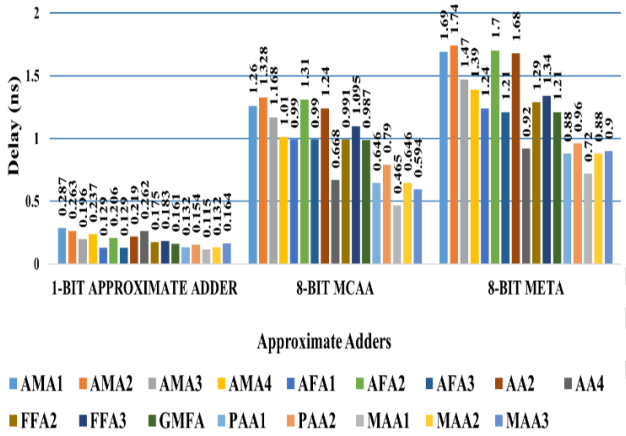
and graphically represented in Figure 9(b). The PDP analysis, as depicted in Figure 10, is presented in decreasing order for the 8-bit MCAA and 8-bit META structures, evaluated using all approximate adders. The MAA1 show an improvement of 23.40% and 33.85% compared to MAA2 and MAA3 respectively in 8-bit META architecture. Similarly, MAA1 shows 71.37% and 79.99% improvement in PDP compared to MAA2 and MAA3 designs in 8-bit MCAA architecture. These findings provide insights into the trade-offs between area, power, and delay in various approximate adder designs, highlighting the advantages and limitations of different implementation approaches for low-power and energy-efficient arithmetic circuits.



(a)

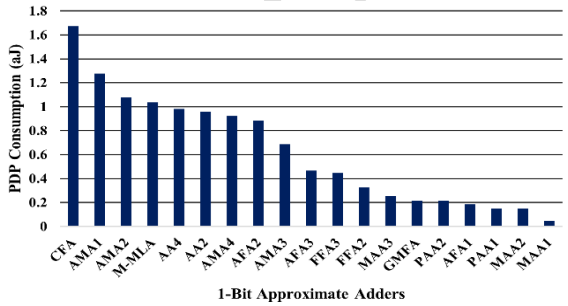


(b)

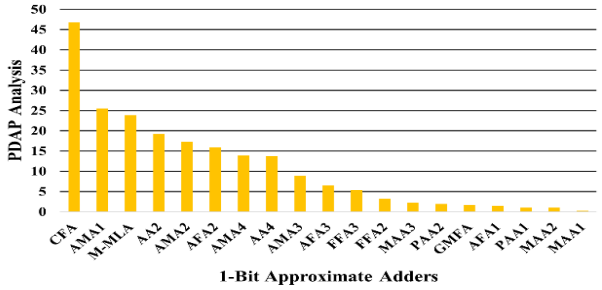


(c)

Figure 8. Comparative analysis of 1-Bit AA, 8-Bit MCAA, 8-Bit META structures in terms of (a) Device Count (b) Power (c) Delay



(a)



(b)

Figure 9. Comparison of 1-bit accurate and approximate adders (a) PDP analysis (b) PDAP analysis

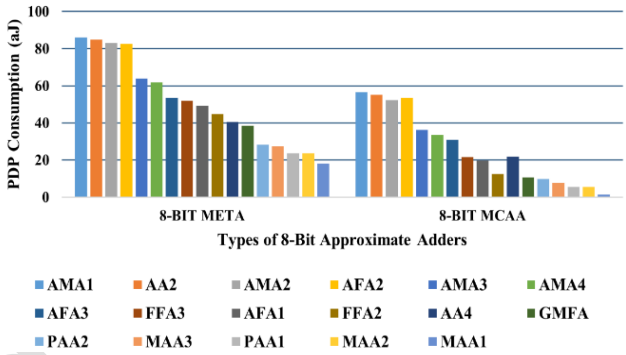


Figure 10. PDP analysis of approximate adders in 8-Bit META and MCAA structure

7.2 *Error metrics of 8-bit Approximate Adders*

The accuracy of the proposed majority-based adders is evaluated using key error metrics, including the NMED, ER, and Mean Absolute Error (MAE). These adders are compared with previously reported approximate adders by implementing in 8-bit architectures and testing them against all possible input combinations using a Verilog-based testbench. Table 9 presents the average PDAP values alongside the error metrics. The analysis indicates that for the 8-bit META adders, MAA2 and AMA2 exhibit the lowest error rates with minimal error distances. However, in terms of PDAP, MAA2 demonstrates superior efficiency, achieving an 80.54% reduction in PDAP compared to AMA2. Additionally, MAA1 in META and MCAA architectures also report lower PDAP values at the cost of reduced accuracy.

Furthermore, the error rates of PAA's and FFA2 designs are significantly higher than those of other adders. Notably, MAA2 exhibits the lowest MAE value, contributing to a reduction in NMED. In the case of the 8-bit MCAA adder, AMA1 achieves a lower error rate than MAA-based designs, albeit with an increase in PDAP. The analysis of PDP versus NMED highlights the trade-off between accuracy and circuit performance in majority-logic-based adders compared to other adder designs. The majority-logic-based adders demonstrate efficiency, as their PDP values predominantly fall

within the left half of the vertical axis in both 8-Bit MCAA and 8-bit META structure as shown in Figure 11 (a) and (b) respectively.

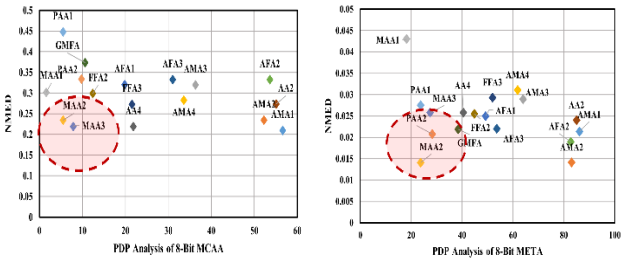


Figure 11. PDP vs NMED analysis for (a) 8-Bit MCAA (b) 8-Bit META structure

Additionally, MAA2 and MAA3 exhibit lower error rates, positioning them in the first half of the horizontal axis, along with GMFA and PAA2 in 8-Bit META structure as shown in Figure 11(b). However, GMFA produces a non-full-swing output, reinforcing the advantage of majority-logic-based adders in achieving an optimal balance of performance, accuracy, and efficiency.

Table 9. Comparison of error metrics with average PDAP for 8-bit approximate adders

Approximate adder	8-BIT MCAA				8-BIT META			
	Average PDAP	NMED	MAE	ER	Average PDAP	NMED	MAE	ER
AMA1	9057.888	0.2099	255	86.05	16535.5	0.02138	255	73.63
AMA2	6687.171	0.2342	255	89.98	14616.84	0.014101	15	68.27
AMA3	3774.135	0.3198	255	97.44	10484.57	0.02892	255	86.57
AMA4	4033.536	0.2827	255	97.57	10629.5	0.031062	255	86.72
AFA1	1270.368	0.3201	255	96.12	7085.261	0.02499	254	78.42
AFA2	7722.922	0.3321	255	89.81	15217.72	0.01890	15	68.22
AFA3	3474.979	0.3321	255	89.81	9011.402	0.0220	255	68.22
AA2	8816.896	0.2733	254	89.97	16311.86	0.0240	252	68.17
AA4	2447.98	0.2189	254	90.08	6803.731	0.0258	255	68.26
FFA2	993.3784	0.2988	255	96.05	6809.858	0.0255	253	78.37
FFA3	2067.71	0.2728	254	95.09	8310.144	0.0293	252	78.37
GMFA	679.814	0.3734	255	99.60	5535.605	0.0219	15	93.78
PAA1	308.0386	0.4475	255	99.58	2843.808	0.02751	15	93.76
PAA2	705.312	0.3335	255	99.60	3623.731	0.02078	15	93.74
MAA1	62.9982	0.3013	255	97.86	2032.934	0.0430	254	88.68
MAA2	308.0386	0.2342	255	89.98	2843.808	0.01410	15	68.27
MAA3	566.676	0.2189	254	90.08	3512.448	0.0258	255	68.26

7.3 Image Quality metrics of 8-bit approximate adders

Three distinct sets of 512 X 512 sized input images with 8-bit pixel depth were selected from an image database [40] and processed using accurate adders. For comparison, the same images were processed using all proposed approximate adders implemented in MCAA and META based 8-bit ripple carry structures. The adders were implemented using Verilog and integrated into MATLAB via the importhdl command for image quality analysis. Image quality metrics, including PSNR and Structural Similarity Index (SSIM), are evaluated.

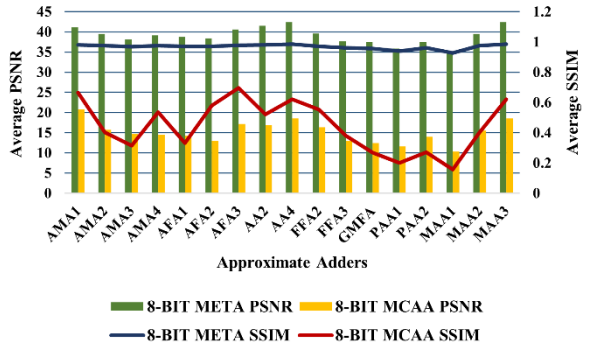


Figure 12 Comparative analysis of image quality metrics in 8-bit META and MCAA

The graphical representation of PSNR and SSIM analysis for 8-bit META and 8-bit MCAA adders is shown in Figure 12. The majority-logic-based adders demonstrate superior performance, achieving higher PSNR and SSIM values, particularly in the META structure. Among them, MAA3 exhibits the highest PSNR and SSIM values; however, it requires an additional inverter compared to MAA2.

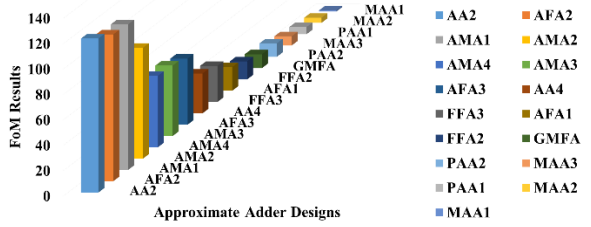
7.4 Figure of Merit

The circuit performance analysis and Error metrics can be jointly analysed using Figure of Merit (FOM) calculations in approximate computing [36]. The FoM is calculated using the formula:

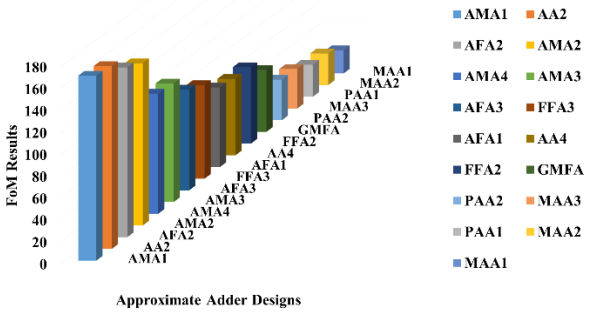
$$FoM = \frac{Normalized\ PDAP}{1 - Average\ NMED}$$

It must be noted that the circuit performs better for lower FoM. The FoM values for the 8-bit META and 8-bit MCAA adders are presented in decreasing order, highlighting the optimal performance of the proposed majority-logic-based designs compared to existing adders. Among these, MAA1 achieves the lowest FOM due to its minimal power-delay product (PDP); however, its output image quality is inferior to that of MAA2 and MAA3. For fully approximate adders, MAA2 and MAA3 provide a better trade-off between accuracy and efficiency. Conversely, in error-tolerant applications, where only the least significant bits (LSBs) utilize approximate adders, MAA1 emerges as the most efficient choice due to its low FOM.

The post-CMOS majority-logic-based approach demonstrates greater efficiency compared to traditional CMOS logic, making it a promising alternative for arithmetic circuit design. Each of the proposed approximate adders is tailored to specific application requirements, with MAA1 proving highly efficient for error-tolerant computing by ensuring an optimal balance between power consumption and accuracy. Meanwhile, MAA2 and MAA3 are well-suited for fully approximate architectures, excelling in applications that tolerate higher error rates in exchange for reduced power consumption and delay.



(a)



(b)

Figure 13 FoM analysis for 8-bit adders using (a) MCAA (b) META

Compared to conventional CMOS-based designs such as AMA, AFA, and AA adders, the FOM of emerging logic-based designs is significantly lower, reflecting their superior performance. Notably, the PAA2 and MAA3 designs, as well as the PAA1 and MAA2 designs, have an equal device count. However, the proposed MAA2 and MAA3 architectures achieve a lower FOM, resulting in improved performance over PAA1 and PAA2, primarily due to their lower error rates and reduced normalized mean error distance (NMED). Additionally, GDI logic, an optimized variant of conventional CMOS logic, demonstrates a relatively small FOM difference when compared to the proposed majority-based designs in the MCAA architecture, while a more significant difference is observed in the META architecture as shown in Figure 13 (a) and (b) respectively.

The proposed 8-bit approximate adder can be scaled to higher bit-width versions using a modular design, with LSBs approximated and MSBs kept accurate to limit worst-case error. In 16-bit implementations, MCAA architecture shows higher error rates compared to the

META architecture. Simulations of 16-bit META architecture with 50% approximation is validated by writing Verilog testbench and results show error rates of 90% for MAA2 and MAA3, still lower than other designs reaching up to 99%, indicating better error efficiency.

Accuracy can be enhanced by reducing the approximation ratio or employing dynamic approximation techniques based on input sensitivity. However, decreasing the extent of approximation introduces area overhead due to the increased transistor count in the accurate portion of conventional designs. For instance, at a 25% approximation level, the accurate adder section using conventional design requires 60 additional transistors compared to a majority logic-based implementation in error tolerant architecture. Notably, majority logic in the META architecture proves efficient across all metrics, offering improved PDAP and linear scalability, making it ideal for larger arithmetic units. Overall, these adders provide a balanced trade-off among power, delay, and accuracy, making them effective for energy-efficient, high-performance computing.

8 Conclusion

This work presents the design and analysis of a majority-logic-based 1-bit adder using experimentally assessed and modelled memristor technology. The proposed design is evaluated against various existing memristor-based adders to assess its performance and efficiency. Additionally, three 1-bit approximate adders are developed using majority logic by integrating memristors with CMOS inverters, offering a balance between performance, power consumption, and circuit complexity. Among the designed approximate adders, MAA1 achieves the lowest Power-Delay-Area Product (PDAP) and Power-Delay Product (PDP), making it the most suitable choice for error-tolerant adder structures, where power efficiency and computational accuracy need to be balanced.

Conversely, MAA2 and MAA3, incorporating two and three inverters respectively, offer an optimal solution for fully approximate adder architectures, enabling enhanced performance in applications that can accommodate higher levels of approximation while benefiting from reduced power consumption and latency. The analysis of both META and MCAA architectures positions MAA2 as an intermediate solution, balancing the trade-offs between MAA1 and MAA3.

Comparative evaluation with conventional CMOS and Gate Diffusion Input (GDI)-based approximate adders demonstrates that majority-logic-based designs offer significant advantages in device count optimization, leading to reduced circuit complexity and improved efficiency. Extensive simulations assess key performance parameters, including power consumption, propagation delay, error metrics, and image quality metrics. These evaluations contribute to the estimation of the Figure of Merit (FoM), where majority-logic-based adders consistently outperform conventional logic-based approximate adders. By considering various design parameters, trade-offs, and application-specific requirements, the most suitable adder architecture can be selected for integration into complex logic circuits.

The results highlight the potential of emerging memristor-based majority logic for designing high-performance, energy-efficient adder architectures. Applications such as neural network accelerators, digital signal processing (DSP), and encryption circuits can leverage the power and area benefits of approximate computing. Neural networks and DSP algorithms are inherently error-tolerant, while non-critical components in encryption circuits can be approximated without compromising security. As memristor technology continues to advance, majority-logic-based designs could play a pivotal role in the development of next-generation computing systems. Broadening the application scope to these domains further underscores the practical relevance and impact of the proposed design for next-generation energy-efficient computing systems.

9 Acknowledgments

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10 Conflict of Interest

The authors declare that they have no conflict of interest.

11 References

[1] A.M. Dalloo, A J. Humaidi, A.K. Al Mhdawi and H. Al-Raweshidy, "Approximate Computing: Concepts, Architectures, Challenges, Applications, and Future Directions," IEEE Access, vol. 12, pp. 146022-146088, 2024, https://doi: 10.1109/ACCESS.2024.3467375.

[2] J.Stremfelj, F. Smole, "Nanotechnology and Nanoscience – From Past Breakthroughs to Future Prospects," Inf. Midem-J. Microelectron. Electron. Compon. Mater.,vol.51, no., pp. 25-48, 2021, https://doi.org/10.33180/InfMIDEM2021.102

[3] L. Chua, "Memristor-The missing circuit element," IEEE Transactions on Circuit Theory, vol. 18, no.5, pp. 507-519,1971, https://doi: 10.1109/TCT.1971.1083337.

[4] D.Yadav ,A.K. Dwivedi ,S.. Verma and D.K. Avasthi, "Transition metal oxide based resistive random-access memory: An overview of materials and device performance enhancement techniques," Journal of Science: Advanced Materials and Devices, vol. 9, no.4, 2024, https://doi.org/10.1016/j.jsamd.2024.100813.

[5] R. K. Tan et al., "Examination of Resistive Switching Energy of Some Nonlinear Dopant Drift Memristor Models," Inf. Midem-J. Microelectron. Electron. Compon. Mater., vol. 54, no. 1, pp. 25–38, 2024 https://doi.org/10.33180/InfMIDEM2024.103

[6] D.Panda, P.P.Sahu and T.Y.Tseng , "A Collective Study on Modeling and Simulation of Resistive Random Access Memory," Nanoscale Research Letters, vol. 13, no.8,2018, https://doi.org/10.1186/s11671-017-2419-8.

[7] N.Kaushik and B.Srinivasu , "High-Speed and Area-Efficient Serial IMPLY-Based Approximate Subtractor and Comparator for Image Processing and Neural Networks", IEEE Transactions on Nanotechnology, vol. 23, pp. 748-757, 2024, https://doi: 10.1109/TNANO.2024.3487223.

[8] C.K. Jha , K. Qayyum, K.Coskun, S. Singh S,M. Hassan, R. Leupers , F. Merchant and R.Drechsler, "veriSIMPLER: An Automated Formal Verification Methodology for SIMPLER MAGIC Design Style Based In-Memory Computing," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 71, no.9, pp. 1-11,2024, https://doi:10.1109/TCSI.2024.3424682.

[9] K.A. Ali, M. Rizk, A. Baghdadi, J.P. Diguet and J. Jomaah, "Hybrid Memristor–CMOS Implementation of Combinational Logic Based on X-MRL," Electronics, vol.10, no.9, 2021, https://doi.org/10.3390/electronics10091018.

[10] A.Singh, "Memristor based XNOR for high speed area efficient 1-bit full adder," 2017 International Conference on Computing, Communication and Automation (ICCCA), Greater Noida, India, 2017, pp. 1549-1553, doi: 10.1109/CCAA.2017.8230048.

[11] A. K. Maan, D. A. Jayadevi and A. P. James, "A survey of memristive threshold logic circuits", IEEE Trans. Neural Netw. Learn. Syst., vol. 28, no. 8, pp. 1734-1746, 2017, https://ieeexplore.ieee.org/document/7464347

[12] S. Kvatinsky, M. Ramadan, E.G. Friedman and A. Kolodny, "VTEAM: a general model for voltage-controlled memristors," IEEE Trans. Circuits Syst. II Express Briefs , vol.62,no. 8 pp. 786–90 ,2015, doi: 10.1109/TCSII.2015.2433536.

[13] Y. Zhou, Y. Li , L. Xu , S. Zhong , R. Xu and X.A. Miao, "hybrid memristor-CMOS XOR gate for non-volatile logic computation," Physica Status Solidi (a), vol. 213, no.4, pp.1050–1054,2015, https://doi.org/10.1002/pssa.201532872.

[14] T. Singh, "Hybrid Memristor-CMOS (MeMOS) based logic gates and adder circuits," X: 1–10, 2015, http://arxiv.org/abs/1506.06735.

[15] K.Cho K, S.J Lee S and K. Eshraghian, "Memristor-CMOS logic and digital computational components," Microelectronics Journal, vol. 46, no.3, pp. 214–220, 2015, https://doi: 10.1016/j.mejo.2014.12.006.

[16] M. Teimoori ,A. Ahmadi ,S. Alirezaee and M.Ahmadi , "A novel hybrid CMOS-memristor logic circuit using Memristor Ratioed Logic," In: 2016 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE), 2016. https://doi:10.1109/ccece.2016.7726661

[17] M. Khalid, S. Mukhtar, M.J. Siddique and S.F. Ahmed, "Memristor based full adder circuit for better performance," Trans. Electr. Electron. Mater. Vol.20, pp.403–10 ,2019, https://doi.org/10.1007/s42341-019-00135-5.

[18] G. Liu, S. Shen, P. Jin, G. Wang and Y. Liang, "Design of memristor-based combinational logic circuits," Circuits Syst. Signal Process., vol. 40, ,pp. 5825–5846 ,2021, https://doi.org/10.1007/s00034-021-01770-1

[19] M.H. Maruf, M.S.I. Ashrafi, A.S.M. Shihavuddin and S.I. Ali, "Design and comparative analysis of memristor-based transistor-less combinational logic circuits," Int. J. Electron., Vol.109, pp.1291–1306,2022, https://doi.org/10.1080/00207217.2021.1966672.

[20] B. Su, J. Cai, Y. Zhang, Y. Wang, S. Wang and K. Wen, "A 1T2M memristor-based logic circuit and its applications," Microelectronics J. vol.132, no.105674, 2023,https://doi.org/10.1016/j.mejo.2022.105674

[21] S.S. Ghodke, S. Kumar, S. Yadav, N.S. Dhakad and S. Mukherjee, "Combinational logic circuits based on a power- and area-efficient memristor with low variability," J. Comput. Electron. Vol.23, pp. 131–141 ,2024, https://doi.org/10.1007/s10825-023-02117-6

[22] S. Guitarra , R. Taco, M.. Gavilánez ,J. Yépez and U. Espinoza , " Assessment of a universal logic gate and a full adder circuit based on CMOS-memristor technology," Solid-State Electronics, vol. 207, no.108704,2023,https://doi.org/10.1016/j.sse.2023.108704.

[23] M. Nawaria, S. Kumar, M.K. Gautam, N.S. Dhakad, R. Singh, S. Singhal et al., "Memristor-inspired digital logic circuits and comparison with 90-/180-nm CMOS technologies," IEEE Trans. Electron. Dev. vol.71, pp. 301–7 ,2024, https://doi: 10.1109/TED.2023.3278625.

[24] Shalini, K. Singh , "High Performance and Scalable Hybrid Memristor-CMOS Based Full Adder," IETE Journal of Research, vol. 70, no.7, pp.6412–6422, 2023,https://doi.org/10.1080/03772063.2023.2297362.

[25] Z. Tao, L. Wang, C. Sun, X. Wan, X. Liu, Z. Cai and X. Lian, "Design of memristor-based combinational logic circuits," IEICE Electron. Express, vol. 21, no.3, pp. 20230587–20230587,2024, https://doi.org/10.1587/elex.21.20230587

[26] L. Xiaojuan ,S. Chuanyang and T. Zeheng , "Realization of complete boolean logic and combinational logic functionalities on a memristor based

universal logic circuit," Chinese Journal of Electronics, vol. 33, no.4, pp.1–10, 2023, https://cje.ejournal.org.cn/article/doi/10.23919/cje.2023.00.091

[27] H.S. Rasheed and R.P. Nelapati, "Design of Hybrid CMOS-Memristor Combinational Circuits: Maximizing Efficiency with Low Power, Area, and Delay," Circuits Syst Signal Process, 2024,https://doi.org/10.1007/s00034-024-02935-4

[28] V.Gupta ,D. Mohapatra ,A. Raghunathan and K. Roy , "Low-power digital signal processing using approximate adders," IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, vol.32, no.1, pp.124–37,2013, https://doi.10.1109/TCAD.2012.2217962.

[29] M. Mirzaei and S. Mohammadi, "Process variation-aware approximate full adders for imprecision-tolerant applications," Computers & Electrical Engineering, vol. 87, no.106761,2020, https://doi.org/10.1016/j.compeleceng.2020.106761.

[30] A. Tirupathireddy ,M. Sarada and A. Srinivasulu , "Energy-efficient approximate adders for DSP applications," Analog Integr Circ Sig Process., vol. 107, pp. 649–657, 2021, https://doi.org/10.1007/s10470-020-01768-w.

[31] S.F. Deymad, N. Shiri and F. Pesaran, "Realized High-Performance Swing Compensator Approximate Reversible Full Adders Using Gate Diffusion Input Technique," Arabian Journal for Science and Engineering, vol. 49, pp. 7079–7094,2024, https://doi.org/10.1007/s13369-023-08637-4.

[32] K.M. Roodbali , K. Abiri and E. Hassanli, "Highly efficient low-area gate-diffusion-input-based approximate full adders for image processing computing," Journal of Supercomputing, vol. 80,pp. 8129–8155,2024, https://doi.org/10.1007/s11227-023-05768-1.

[33] N.Shiri, A.Sadeghi and M. Mahmood Rafiee, "High-efficient and error-resilient gate diffusion input-based approximate full adders for complex multi-stage rapid structures," Computers and Electrical Engineering, vol. 109,pp.108776,2023, https://doi.org/10.1016/j.compelceng.2023.108776.

[34] M.C. Parameshwara and N. Maroof, "An Area-Efficient Majority Logic-Based Approximate Adders with Low Delay for Error-Resilient Applications," Circuits Systems and Signal Processing , vol.41, pp.4977–4997,2022, https://doi.org/10.1007/s00034-022-02014-6

[35] S. Angizi , H. Jiang ,R.F. DeMara, J. Han and D. Fan, "Majority-Based Spin-CMOS Primitives for Approximate Computing," IEEE Transactions on Nanotechnology, vol. 17, no.4, pp. 795-806, 2018, https://doi: 10.1109/TNANO.2018.2836918

[36] S.Rangaprasad and V. K. Joshi, "A Fully Non-Volatile Reconfigurable Magnetic Arithmetic Logic Unit Based on Majority Logic," IEEE Access, vol.11, pp.118944-118961, 2023, https://doi: 10.1109/ACCESS.2023.3327261.

[37] S. Muthulakshmi , Chandra Sekhar Dash and S.R.S. Prabaharan , "Memristor augmented approximate adders and subtractors for image processing applications: An approach," AEU - International Journal of Electronics and Communications, vol. 91,pp. 91-102,2018,https://doi.org/10.1016/j.aeue.2018.05.003.

[38] Nithya Natarajan and Paramasivam Kuppusamy, "Pt/Al2O3/HfO2/Ti/TiN bi-layer RRAM device for imply–inhibit logic applications: Unveiling the resistive potential by experiment and simulation", Materials Science-Poland vol. 43,pp.196-209,2025. https://doi.org/10.2478/msp-2025-0016

[39] N. Nithya , K. Paramasivam, "MINI Logic 1-Bit Adder: A Comparison with Hybrid NMOS-Memristor-Logic Styles Using Ta2O5/Al2O3 Based RRAM Device," Advances in Electrical and Computer Engineering, vol. 24,no. 3, pp. 33-44,2024, https://doi:10.4316/AECE.2024.03004.

[40]Image Database Source: https://ccia.ugr.es/cvg/CG/base.htm

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