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Small Signal Modeling of Scaled Double-Gate MOSFET for GHz Applications

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Abstract: The limits on scaling suggest the technology advancement for the solid-state devices. The double-gate (DG) MOSFET has emerged as an alternative device structure due to the certain significant advantages, i.e. increase in mobility, ideal sub-threshold slope, higher drain current, reduced power consumption and screening of source end of the channel by drain electric field (due to proximity to the channel of the second gate, which reduces the short channel effects). In this work, we have analyzed the double-gate MOSFET (undoped body because the doping rapidly varies the threshold voltage). The analytical expressions has been derived on the basis of surface potential model, which has been further used to yield the potential distribution, drain current, conductance and trans-capacitance. This illustrate the volume inversion effect is quite significant in this device upto the certain range of dimensions. In addition to this, we have analyzed the performance of symmetric DG MOSFET based on the circuit design prospective using S-parameters.

Keywords: Short channel effect; Double-gate MOSFET; S-parameters, RF devices; Microelectronics; VLSI.

Modeliranje majhnih signalov na pomanjšanem MOSFET z dvemi vrati za GHz aplikacije

Izvleček: Meje pomanjševanja zahtevajo napredno tehnologijo polprevodniških elementov. MODFET z dvojnimi vrati se kaže kot alternativen element zaradi očitnih prednosti, kot so: večja mobilnost, idealen naklon pod pragom, višji ponorni tok, znižana poraba in spremljanje izvorne strani kanala z električnim poljem ponora (zaradi bližine drugega kanala, kar zmanjšuje vplive kratkih kanalov). V delu smo analizirali MOSFET z dvemi vrati (nedopiran, saj dopiranje vpliva na pragovno napetost). Analitičen izraz je bil pridobljen na osnovi modela površinskega potenciala in je bil nadalje uporabljen za določanje porazdelitve potenciala, ponornega toka ter prevodnosti in trans kapacitivnosti. Volumski inverzijski vplivi so pomembno do določenih dimenzij. Dodatno smo raziskali učinkovitost simetričnega MOSFET z dvemi vrati na osnovi načrtovanja veza z S parametri.

Ključne besede: kratki kanal; MOSFET z dvemi vrati; S parameteri, RF elementi; mikroelektronika; VLSI.

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1 Introduction

The MOSFETs are basic cells for the integrated circuits but the demand to increase the switching speed, packing density and reduction in power consumptions are the reasons to extend the work in the direction of miniaturization as suggested by ITRS [1]. Initially, the scaling was the basic tool for miniaturization, however with the advancement in scaling, certain undesirable effects restrict the performance of the device such as short channel effects (SCE) [2, 3]. This motivated to move onto the new device structures. Therefore, *Balestra et. al*. [4] have proposed the first double-gate (DG) MOSFET with significant volume inversion effect. Currently, the DG MOSFET is a subject of intense very large scale integration (VLSI) research and a replacement for conventional bulk MOSFET beyond the *45-nm* technology [5]. It can be scaled to the shortest possible channel length for a given oxide thickness and more electrostatically robust than the earlier reported MOSFETs due to the dual-gate shielding and the reduced SCE [6].

Fossum et. al. [7] have analyzed the higher processing speed of DG MOSFET as compared to that of the single-gate MOSFET which further encouraged *Solomon et. al.* [8] to confer the advantages of the two gates over one gate. Fig. 1 shows the schematic of a DG MOSFET and the Fig. 2 presents the two major DG MOSFET structures:

Symmetric type with both gates of identical work-functions where both the surface's channels turn on at the same gate voltage [9] and *Asymmetric type* with either different work function of the gates or different gate oxide thicknesses where only one channel turns ON at the threshold voltage [10, 11].

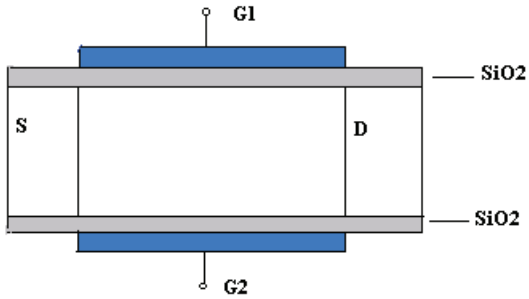

Figure 1: The schematic of double-gate MOSFET.

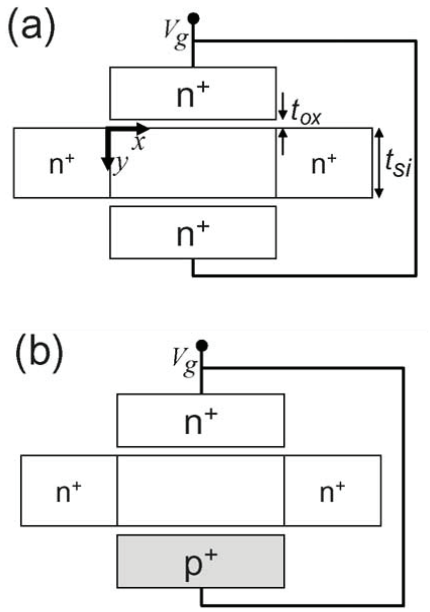

Figure 2: (a) Symmetric Double-gate MOSFET, (b) asymmetric Double-gate MOSFET [11].

Taur et. al. [12] have derived the analytical model based on the charge sheet approximation which is applicable to all operating regions such as cutoff, linear and saturation. Lu et. al. [13] also have developed a design based on the *Poisson theory* and the current continuity equation without charge sheet approximation and accounting the volume inversion concept. The drain current, terminal charges and the capacitances are further developed based on the numerical iterations. However, both the authors [12, 13] discussed the asymmetric DG MOSFET which is more sensitive as compared to the symmetric, to Silicon body thickness which further varies the threshold voltage. Yu et. al. [14] have proposed an algorithm and the PSP model for approximation of the surface potential of both the single-gate (SG) MOSFET and DG MOSFET. The model can cover all the operating regions without the use of fitting parameters or charge sheet approximation. However, this algorithm is really complex for implementation.

In addition to this, *Conde and Sanchez* [15] have developed a unified model for symmetric, asymmetric DG MOSFET and bulk MOSFET by using the mix-formulation of the charge and surface potential approaches. The mathematical expression derived for the drain current depends on the Silicon body thickness. However, the assumption is made that for the symmetric DG MOSFET, the electric field vanishes at the mid-point of the front and back surfaces but for the asymmetric DG MOSFET, the electric field is present. In addition to this, for the conventional MOSFET the charge coupling factor is zero and charge sheet approximation has not been used in ref. [15]. The state of the art of compact models for undoped DG MOSFET using the 1-D *Poisson equation* with the introduction of the SCE has been discussed in detail in ref. [16]. The threshold voltage based model for undoped DG MOSFET was also explored in ref. [17] and discusses the feasibility and the advantages of DG MOSFET over the conventional MOSFET. In ref. [18], an analytical expression for electric potential of the symmetric and asymmetric DG MOSFET with undoped body has been derived by considering the mobile charge in the *Poisson equation* and it has been illustrated that the *ON-state* currents differ slightly from each other when the Silicon thickness is significantly small. *Cakici and Roy* [19] have discussed a circuit perspective with the effect of connected gates or independent gates DG MOSFET, and illustrated that the significantly high noise immunity at low dynamic power dissipation can be achieved by the independently operating gates (as it increases the gate to gate coupling). In addition to this, it also affects the delay, leakage power and process variations. Moreover, with the use of independent-gates technology, the dynamic threshold voltage control is feasible. *Singh and Jiang* [20] showed that with the help of asymmetric DG MOSFET high performance and low power circuits are feasible in the nanometer regime. Therefore, this structure can be used in phase locked loop where the requirement is high speed, low voltage and low power operation [21]. Further, the other application of symmetric DG MOSFET is as a fast switching device [22]. Recently,

Srivastava et. al. [22-24] have analyzed the DG MOSFET and cylindrical surrounding double-gate (CSDG) MOSFET for the application as a double pole four throw switch.

In this research work, we have analyzed the performance of the symmetric DG MOSFET based on the potential distribution, sheet charge, drain current, terminal charges and trans-capacitance. Further, the trans-capacitances are used for the circuit simulation. The work has been organized as follows. Section 2 has discussion about the symmetric DG MOSFET with its design philosophy and working operation. Section 3 deals with the analysis and the simulation model. Section 4 explores the simulation results of the symmetric DG MOSFETs. Finally, the Section 5 concludes the work and recommends the future aspects.

2 Symmetric Double-Gate MOSFET

The planar DG MOSFET is an extension of the single-gate MOSFET which consist two gates designated as front-gate and back-gate, and a sandwiched ultra thin Silicon layer between these gates [25]. The additional gate significantly increases the electrostatic gate control over the channel and these gates are effective in shielding the drain electric field lines from reaching the source to reduce the potential barrier as well as reducing the short channel effects (SCE). Due to undoped / lightly doped body, the problem of random dopant fluctuation is also negligible. Moreover, both the gates contribute to inversion carriers, which have high drive capability and two channels for the current flow are formed (when these two gates simultaneously control the charge). Also, due to the very thin Silicon film, a better coupling between front-gate and back-gate exists, which affects the terminal characteristics of the MOSFET.

Double-gate silicon-on-insulator transistor with volume inversion has been analyzed by Balestra et. al. [26]. The basics of the fabrication processes are helpful in the fabrication of DG MOSFETs [27]. Yesayan et. al. [28] have included the effect of interface traps in nanowire and double-gate junction-less devices through a charge-based model that has been developed previously. *Roy et. al.* [29] have accurately handled both *Fermi–Dirac statistics* and *bias-dependent diffusivity* regarding core compact model for undoped, high mobility, and low density of states materials in a double-gate device architecture. Taur et. al. [13, 30] have presented an analytic potential model for long-channel symmetric and asymmetric double-gate MOSFETs. This design has been derived from the solution of *Poisson's* and current continuity equation without the charge-sheet approximation. This results in the analytic expressions of the drain-current, terminal charges, and capacitances for long channel DG MOSFETs continuous in all operation regions (linear, saturation, and sub-threshold), making it suitable for compact modelling. The extension of the DG MOSFET is as cylindrical surrounding-gate MOSFET has been analyzed by Sood et. al. [31].

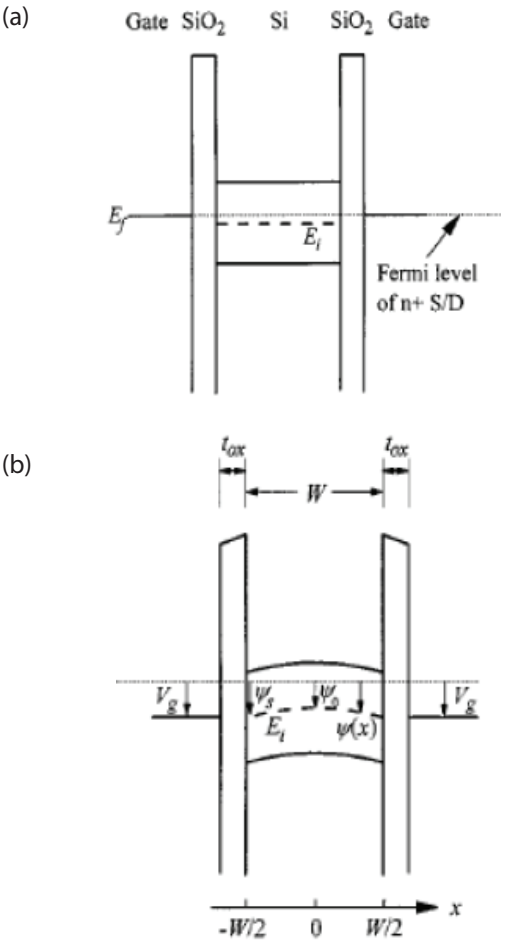

Figure 3: The band model of the symmetric DG MOSFET a) $V_{gs} = 0\ V$ b) $V_{gs} = V_{th}$ [9].

For the symmetric double-gate device structure, at the zero gate voltage the Silicon bands are flat for the mid-gap gate work function as shown in Fig. 3(a). However, at $V_g = V_{th}$, the edge of conduction band (Silicon body) near the surface bents as in Fig. 3(b) and approaches the conduction band edge of the n^+ source/drain. However, the conduction bands in both surfaces, under both gates, are bent by the similar value as the work functions of two gates are identical. At ON-state, two conductive channels (under both the gates) are formed for the symmetric double-gate device, unless the Silicon body is not very thin [12].

3 Analysis of Parameters

To analyze the various parameters, we have first analyzed the *1-D Poisson's equation* in the Cartesian coordinate system with gradual channel approximation which is given as [32]:

$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\varepsilon_{Si}} e^{q(\psi - V)/kT} \tag{1}$$

where, q and ε_{si} are the electron charge and dielectric permittivity of Silicon respectively. The n_i, k, and T are the intrinsic concentration of Silicon, the Boltzmann constant, and working room temperature, respectively. The V represents the quasi-Fermi potential $V = 0$ at source side and $V = V_{ds}$ at drain side. We have considered the n^+ DG MOSFET, therefore the holes density is negligible and the Silicon film is undoped or lightly doped that is:

$$n_b << n_i e^{q(\Psi - V)/kT} \tag{2}$$

where, n_b is the doping concentration. However, integrating the Equation (1) twice, we can get the potential distribution equation as a function of '*x*' which is position in the Silicon body thickness. In the symmetric DG MOSFET, the electric field is zero at $x = 0$ that is the center of the Silicon body thickness.

3.1 Surface Potential

The surface potential (ψ_s) for DG MOSFET is:

$$\psi_s = \psi_o - \frac{2kT}{q}\left\{\log\left[\cos\left(\sqrt{\frac{q^2 n_i}{2kT\varepsilon_{Si}}} e^{q(\psi_o - V)/2kT} x\right)\right]\right\} \tag{3}$$

The boundary condition for symmetric DG MOSFET:

$$\frac{\varepsilon_{ox}}{t_{ox}}\left(V_{gs} - \Delta\phi_i - \psi_s\right) = \pm\varepsilon_{Si}\left.\frac{d\psi}{dx}\right|_{x=\pm w/2} \tag{4}$$

where, ε_{ox}, V_{gs} and t_{ox} are the permittivity of oxide, gate voltage and oxide thickness respectively. After boundary conditions are satisfied, the center potential is given by:

$$\psi_s = V + \frac{2kT}{q}\left\{\ln\left[\frac{2}{at_{Si}} Sin^{-1}\frac{q\varepsilon_{ox}(V_{gs} - \psi_s)}{2\varepsilon_{Si}kTa} e^{-q(\psi_s - V)/2kT}\right.\right. \tag{5}$$

where, t_{si} is the Silicon body thickness. The surface potential is given by:

$$Sin\left(\frac{at_{Si}}{2}\sqrt{1-\left(\frac{qC_{ox}(V_{gs}-\psi)}{2kTa\varepsilon_{Si}} e^{-q(\psi-V)/2kT}\right)^2} * e^{q(\psi-V)/2kT}\right) = \tag{6}$$
$$= \frac{qC_{ox}(V_{gs}-\psi)}{2kTa\varepsilon_{Si}} e^{-q(\psi-V)/2kT}$$

where,

$$a = \sqrt{\frac{q^2 n_i}{2kT\varepsilon_{Si}}} \tag{7}$$

3.2 Drain Current

By following the dual integral [33], the drain current can be written as:

$$\begin{aligned} I_{ds} &= \frac{2\mu W}{L}\int_0^{V_{ds}} Q(V)dV \\ &= \frac{2\mu R}{L}\int_{\psi_{ss}}^{\psi_{sL}} Q(\psi_s)\frac{dV}{d\psi_s}d\psi_s \end{aligned} \tag{8}$$

where *Q* represents the inversion charge. Therefore, the drain current becomes:

$$I_{ds} = \frac{2\mu C_{ox}W}{L}\left[\frac{2kT}{q}\left(V_g - (\psi_{sL} - \psi_{ss})\right) - \frac{1}{4}\left(V_g - (\psi_{sL} - \psi_{ss})\right)^2 + \right.$$
$$\left. + \frac{8\varepsilon_{Si}k^2T^2}{q^2WC_{ox}}\ln\left(\frac{C_{ox}\left(V_g - \psi_{sL}\right) + \frac{4\varepsilon_{Si}kT}{qW}}{C_{ox}\left(V_g - \psi_{ss}\right) + \frac{4\varepsilon_{Si}kT}{qW}}\right)\right] \tag{9}$$

where, ψ_{ss} and ψ_{sL} are the potential at source side ($V = 0$) and potential at drain side ($V = V_{ds}$) which can be found through Equation (6).

3.3 Terminal Charges

For the modeling of total inversion charge, Ward Dutton charge partition method [24] has been used where the total inversion charge given by $Q = C_{ox}\left(v_{gs} - \psi_s\right)$ is partitioned into source charge (Q_s), drain charge (Q_d), and gate charge (Q_g) such as [34]:

$$Q_g = \int_0^L Q(y)dy,\ Q_d = \int_0^L \frac{y}{L}Q(y)dy,\ Q_s = \int_0^L\left(1 - \frac{y}{L}\right)Q(y)dy \tag{10}$$

We are modeling the charges based on the surface potential, therefore transforming y to ψ_s in all the equations and then performing the integration analytically which yields the expressions for the terminal charges.

3.4 Trans-Capacitance

Based on the expressions of the terminal charges, the capacitances of the double-gate MOSFET such as gate to source (C_{gs}), gate to drain (C_{gd}), and source to drain

(C_{sd}) can be written as:

$$C_{gs} = \frac{\partial Q_g}{\partial \psi_{ss}} \frac{\partial \psi_{ss}}{\partial V_s} \quad C_{gd} = \frac{\partial Q_g}{\partial \psi_{sL}} \frac{\partial \psi_{sL}}{\partial V_d} \quad C_{ds} = \frac{\partial Q_s}{\partial \psi_{sL}} \frac{\partial \psi_{sL}}{\partial V_d} \quad (11)$$

where the values of charges Q_s, Q_d, and Q_g are given in Equation (10). These capacitances were used in circuit simulations. The DG MOSFET with same potential applied to both gates is a combination of two single-gate MOSFETs connected in parallel.

3.5 Small Signal Model

The small signal equivalent circuit as shown in Fig. 4 has been analyzed. This equivalent circuit has been derived from the formation of capacitance and resistance at the junctions and the body of the double-gate MOSFET. Based on the intrinsic parameters of the device, the *Y-parameters* can be derived. However, scattering parameters can be obtained by applying the normal conversion based on the *Y-parameters* [35, 36].

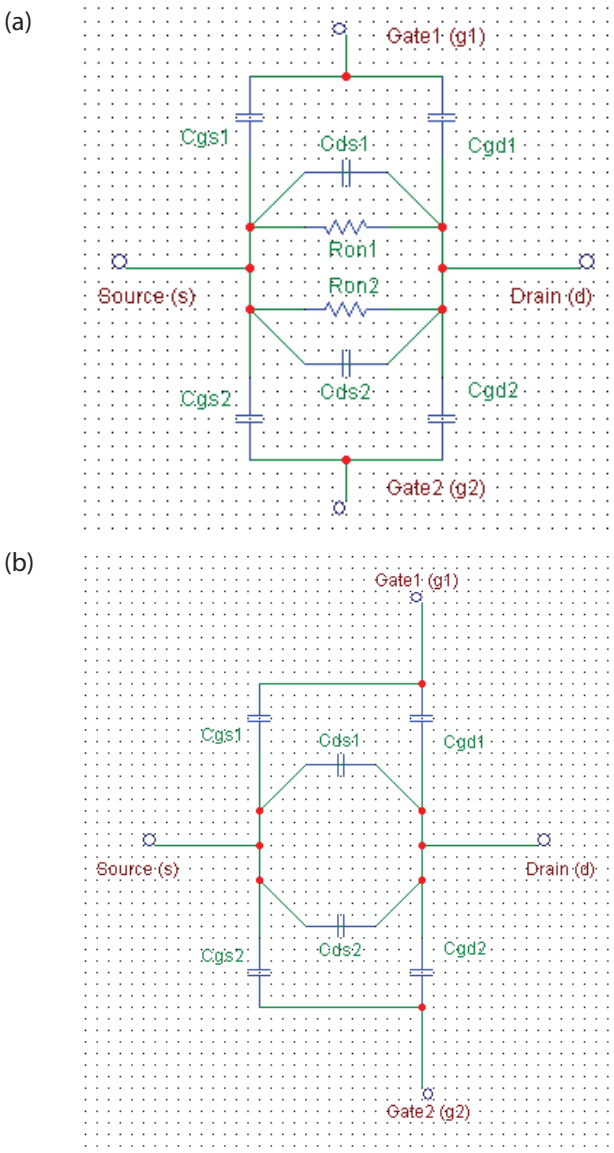

Figure 4: Small signal modeling of DG MOSFET at (a) Switch-ON state, and (b) Switch-OFF state.

4 Results and Its Analysis

We have presented the simulion results for symmetric DG MOSFET based on the electric potential, electron density, drain current, conductance, terminal charges and transcapacitance. In addition to this, the S-parmeter and gain analysis has also been performed.

4.1 Volume Inversion Analysis

The volume inversion effect is quite significant when the gate-source voltage is less than that of the threshold voltage. With the increase in gate voltage, the potential increases at the surface as the channel is formed on the surface and the minimum electric potential lies at center of the body $x = 0$, due to the screening of the center of the Silicon body by the charges on the surface as shown in Fig. 5. In addition to this, the significant effect can be seen for the $V_{gs} = 0.412\ V$ and $V_{gs} = 0.845\ V$.

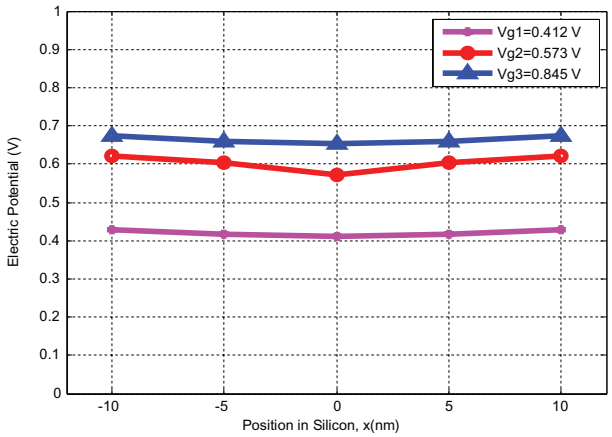

Figure 5: Electric potential variation with Silicon body thickness (nm).

The volume inversion effect is significant up to threshold voltage, $V_{th} = 0.4\ V$ but as the gate voltage crosses the threshold voltage the surface and the center potentials are decoupled. The center potential saturates at a specific value of potential as the arcsine argument in the Equation (5) cannot grow beyond $\pi/2$ but the surface potential keeps on increasing. It is illustrated through the Fig. 6 that the surface potential variation above the threshold voltage is independent of the Silicon body thickness. The input and output charecterstics of the DG MOSFET as shown in Fig. 7(a) and Fig.

7(b) are similar to that of the conventional MOSFET. The response of drain to source voltage over the drain current with various values of V_{gs} shown in Fig. 7(b) reveals the two operating regions (i. e. linear and saturation regions). By extrapolating these curves and finding the intersection with the x-axis the corresponding values of threshold voltage can be obtained (V_{th} = *0.6 V* and V_{th} = *0.7 V* for V_{ds} = *0.5 V* and V_{ds} = *1 V*, repectively).

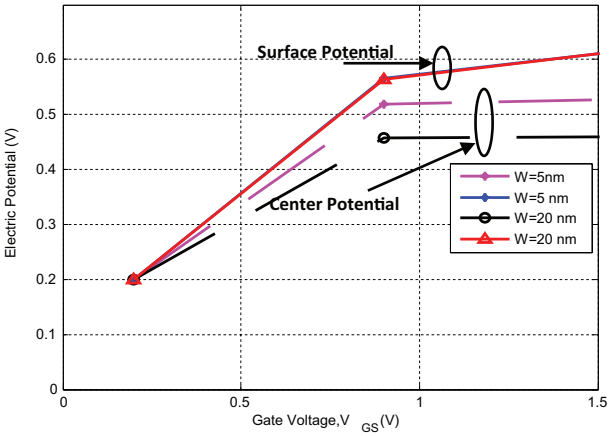

Figure 6: Electric potential variation with gate to source volatage.

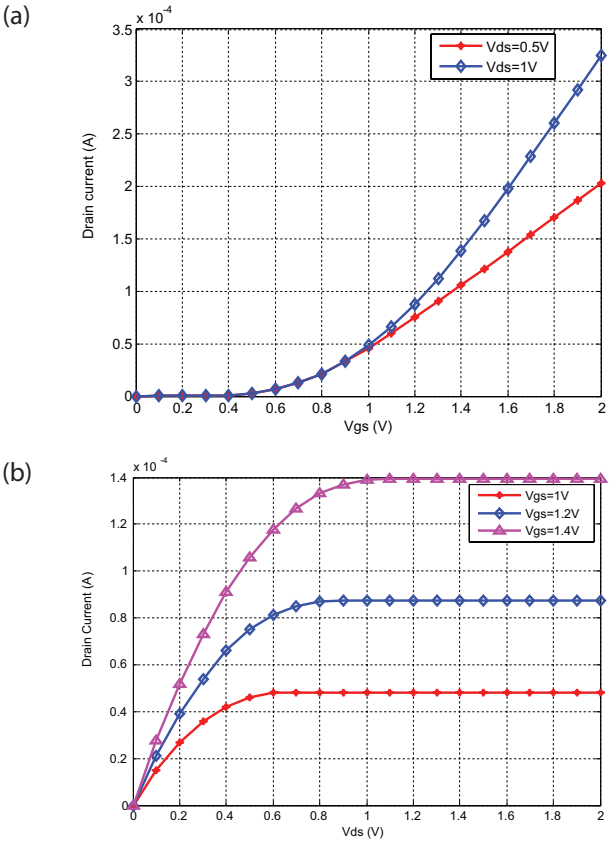

Figure 7: Drain current variation of DG MOSFET for t_{ox} = *2 nm*, *W = 30 nm* and *L = 90 nm* at various (a) gate to source voltage and (b) drain to source voltage.

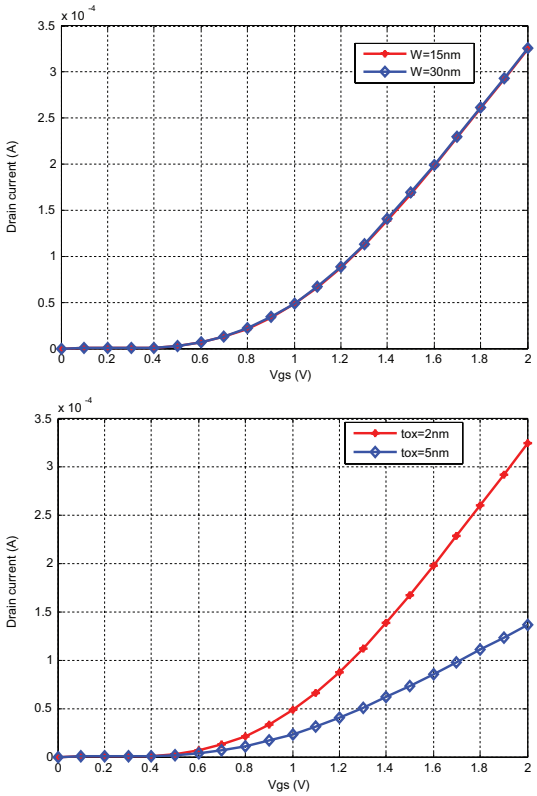

Figure 8: Response of drain current for various gate to source voltage at V_{ds} = *1 V* and *L = 90 nm* for (a) *fixed* t_{ox} = *2 nm* and (b) fixed width *W = 30 nm*.

4.2 Drain current analysis

The drain current is independent of the device width, however, its dependence over the oxide thickness is quite significant as shown in Fig. 8. It is well illustrated in Fig. 8(b) that the charge formation on the surface increases with the reduction in the oxide thickness, hence results in the increased device current.

4.3 Conductance and Transconductance Analysis

Fig. 9 shows the effect of oxide thickness on the conductance and transconductance for *W = 30 nm* and *L = 90 nm*. As the drain to source voltage increases for chosen oxide thickness, the conductance of the device decreases and reduces to zero as the pinch-off point is achieved as shown in Fig. 9(a). In addition to this, with the decrease of oxide thickness, the conductance of the device increases. In Fig. 9(b) as the gate voltage reaches the threshold voltage the transconductance increases with increasing V_{gs}. However, transconductance $G_m = {}^{\partial I_{ds}}/_{\partial V_{gs}}$, depends on C_{ox} as in Equation (9) through I_{ds}. Therefore with the increase of oxide thickness (which reduces the C_{ox}), the transconductance decreases. This concludes the significant enhancement in the overall gain of the device.

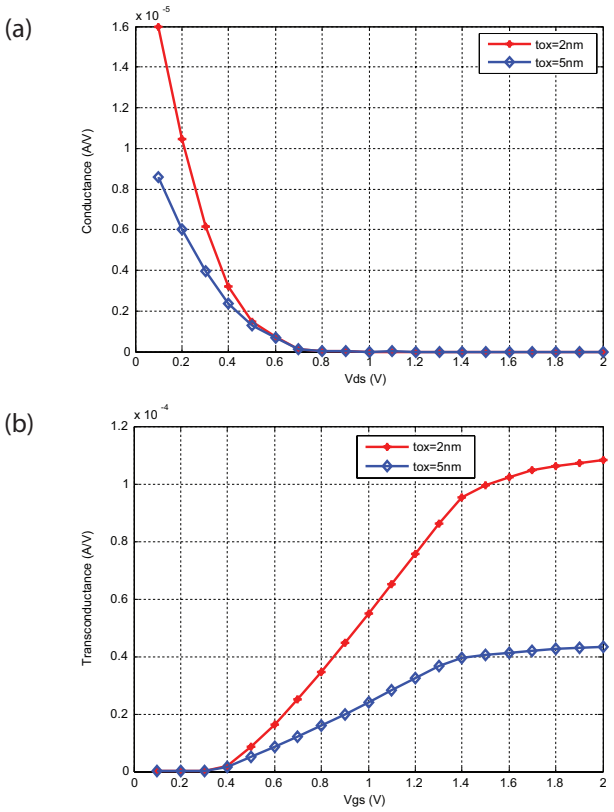

Figure 9: Effect of oxide thickness on the (a) conductance at $V_{gs} = 1\ V$ and (b) trans-conductance at $V_{ds} = 1\ V$.

4.4 Trans-Capacitance and Terminal Charge Analysis

Fig. 10(a) and Fig. 10(b) illustrate the trans-capacitance and the variation of terminal charges with V_{ds} for specific value of the oxide thickness. As the oxide thickness increases, the charge storage capacity decreases which further results in the decrease in capacitance of the device. However, the gate to drain capacitance (C_{gd}) and the source to drain capacitance (C_{sd}) do not depend on drain voltage after the saturation is achieved. Fig. 10(c) and Fig. 10(d), where $t_{ox} = 2\ nm$, $W = 20\ nm$ shows the variation with width of device (W). When comparing Fig. 10(a) and Fig.10(b) with these, it can be seen that as the width reduces the terminal charges the trans-capacitances are also reduces due to smaller device area. It is illustrated by Fig. 10(b) and Fig. 10(d) that the source charge always saturates to the value of *6/10* of the gate charge and drain charge saturates to *4/10* of the gate charge.

4.5 S-Parameters Analysis

Fig. 11 shows the S-parameters computed analytically using equivalent circuit of DG MOSFET with $t_{ox} = 2\ nm$, $W = 40\ nm$, $L = 1\ \mu m$, $V_{gs} = 1\ V$ and $V_{ds} = 0.9\ V$. The S_{11} represents the input reflection coefficient and it has been illustrated that the S_{11} reduces for high frequency,

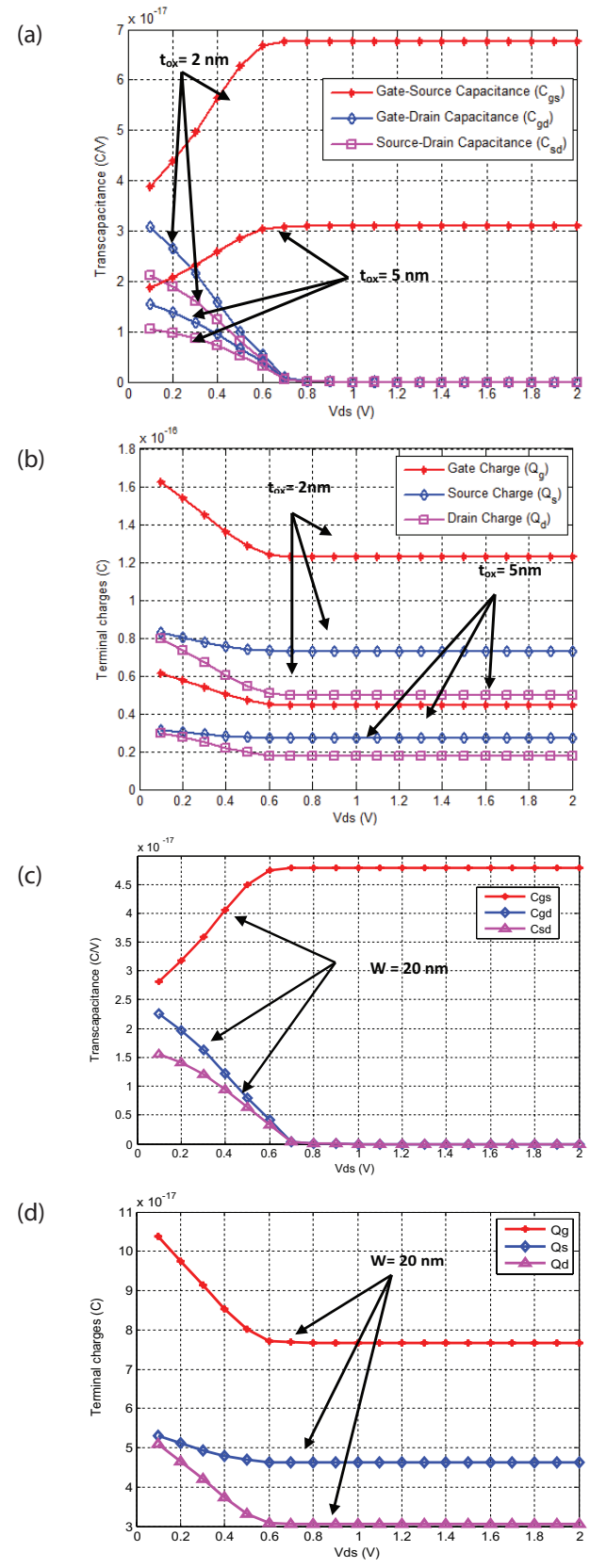

Figure 10: (a) Trans-capacitance, (b) terminal charges for $W = 30\ nm$ and $L = 90\ nm$, (c) Trans-capacitance, and (d) terminal charges for $W = 20\ nm$, $t_{ox} = 2\ nm$ and $L = 90\ nm$, at $V_{gs} = 1\ V$.

which is an advantage as the return loss is reduced for the device. The S_{21} represents the amount of power transferred from the input port to the output port and it also illustrates that as the frequency increases the S_{21} parameter remains constant which implies constant forward gain at higher frequencies.

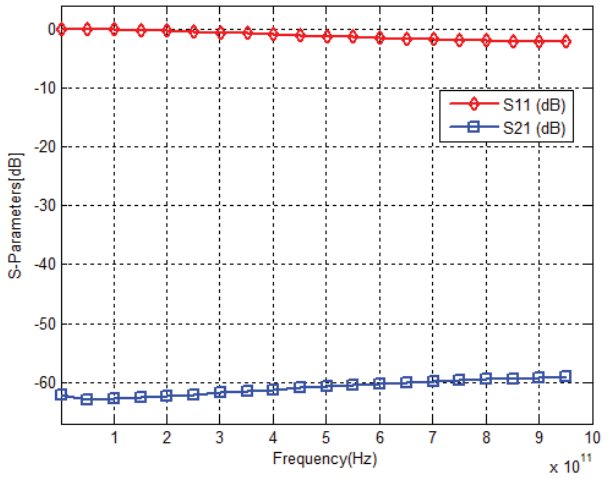

Figure 11: S-parameters over a range of high frequencies.

4.6 Power Gain Analysis

Fig. 12 represents the power gain achieved by the DG MOSFET over the range of frequencies. The unilateral power gain is the gain achieved when the input and the output port are matched simultaneously and the feedback is neutralized by adding a feedback network. As the frequency increases, this gain decreases exponentially and the decrease is smaller at high frequency due to the dual gate controllability. By extrapolating the curve for the gain of *1 dB*, the maximum frequency of oscillation can be inferred from the Fig. 12 to be around *254 GHz*. The gain achieved (when the two ports are simultaneously matched) is known as maximum stable power gain. It is predicted by the Fig. 12 that as the frequency increases the input-output mismatch decreases. In addition to this, the gain always remains above *0 dB* which suggests a major figure-of-merit for low noise amplifiers. The maximum unilateral transducer power gain is the ratio of power delivered to load to the power available at the source when the neutralization is provided which further enhances the maximum power transfer. All these gains are stable with the frequency only due to the dual gate controllability as suggested by Fig. 12. Therefore, the DG MOSFET with the analyzed dimensions is useful for high frequency applications.

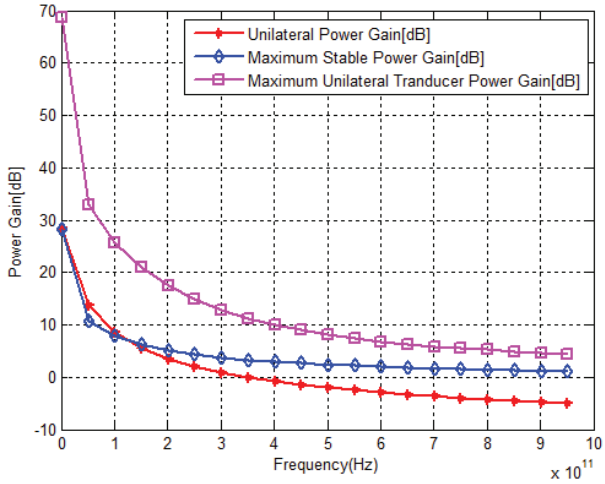

Figure 12: Response of the power gain at various frequencies for the DG MOSFET.

5 Conclusions and Future Recommendations

In this work, the analytical modeling of symmetric DG MOSFET with undoped Silicon body has been presented. The results reveals that for the symmetric DG MOSFET the electric potential varies in proportion with the gate voltage and the minimum potential lies at the center of the Silicon body due to the symmetric nature of device. In addition to this, the volume inversion effect is also significant and the surface potential variation beyond the threshold voltage is independent of the Silicon body thickness.

The *I-V* and *C-V* model are also reproduced and it is seen that the drain current in strong inversion region is invariant to width of device. Moreover, the intrinsic model has been proposed from where the high frequency characteristics in terms the S-parameters and gain are obtained. The results show that the DG MOSFET is useful for high frequency applications. However, with the optimization of the device structural parameters, the performance can be improved, which will be reported in future communication.

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