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DOE Study of Epitaxial Layer Thickness and Resistivity Effects on P-i-N Diode for beyond 300 V of Reverse Voltage Applications

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Abstract: A discrete power switching device used in the applications of computer and telecommunications requires operating less than 300 V during reverse bias, but for the use of motor control, robotics, and power distribution, it requires operating at beyond 300 V. With the current design structure, the P-i-N diode device can only operate at 250 V. To widen the operating range of the P-i-N power switching avalanche diode that can be operated more than 300 V, we studied the effects of the epitaxial layer thickness (WD) and resistivity (ρ) during forward and reverse biasing by performing a process simulation as well as the confirmation on the two level factorials of design of experiment (DOE) of physical wafers. The result shows that, the changes of the WD of 42 µm and ρ of 32 ohm·cm on a P-i-N diode can increase the reverse breakdown voltage (VR) performance beyond 300 V during reverse bias.

Keywords: Forward voltage; Breakdown voltage; Power device

Načrtovanje eksperimenta vplivov debeline in upornosti epitaksijske plasti P-i-N diode pri reverznih napetostih nad 300 V

Izvleček: Diskretni močnostni stikalni element za uporabo v računalnikih in telekomunikacijah zahteva delovanja pri zaporni napetosti pod 300 V. Pri krmiljenju motorjev, v robotiki ali pri močnostnih aplikacijah pa zahteva delovanje v zaporni smeri preko 300 V. Trenutna struktura P-i-N diode lahko deluje le do 250. Za višje napetosti je potrebna močnostna plazovita P-i-N dioda, na kateri smo preučevali vplive debeline epitaksijske plasti in upornosti pri prevodni in zaporni napetosti. Analiza sloni na simulaciji procesa dvonivojske faktorizacije načrtovanja eksperimenta silicijeve rezine. Rezultati izkazujejo, da sprememba debeline za 42 µm in upornosti za 32 ohm·cm zviša prebojno napetost preko 300 V.

Ključne besede: Forward voltage; Breakdown voltage; Power device

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1 Introduction

Diode is a simple semiconductor device with two terminals, allowing only unidirectional current to flow. It is created with the presence of p-type and n-type semiconductor materials in intimate contact on an atomic scale, yielding the P-N junction in between [1]. The formation of P-N junction occurred by diffusion of acceptor impurities (p-type dopant) into an n-type silicon crystal or vice versa. A depletion region formed instantaneously across a P-N junction and it is easily to be described when the junction is in thermal equilibrium or in a steady state: in both of these cases, the properties of the system does not vary in time; thus, it is known as dynamic equilibrium [2, 3]. Figure 1 (a) shows the diode 2D structure and electrical field distribution of P-N diode. For high power applications, an ideal power diode should be able of conducting high forward bias current (I_F) during forward bias voltage (V_F) of ~0.7 V and supporting high reverse breakdown voltage (V_R) in the range of 50 to 200 V [4, 5].

During reverse bias, P-N diode experiences the avalanche breakdown. To achieve the avalanching, besides the requirement of a large field, it also requires a sufficient distance to allow the electron to accelerate, hence gain enough kinetic energy, and lead to an avalanche of multiple hole-electron pair's creation [6]. In other words, to ensure the high V_R, a thick n-type substrate bulk is required for a vertical structure of simple P-N junction diode. For a vertical structure of P-N junction diode, a very thick wafer substrate bulk can be used to fulfill the requirement of a power diode. However, thicker substrate exhibits several drawbacks, which are 1) greater weight and 2) higher production cost.

Alternatively, higher V_R and I_F can be achieved by using the P-i-N diode structure with a thinner substrate. The P-i-N diode was one of the very first semiconductor devices developed for power circuit application [4, 7]. This evolution came from a conventional P-N junction diode with the addition of an extra intrinsic layer deposited between p-type and n-type regions. Figure 1 (b) (i) illustrates the P-i-N diode structure in 2D structure and electrical field distribution of P-i-N diode. In P-i-N diode, the reverse breakdown voltage is dependence on the depletion region formed with a P-N junction structure. The voltage is primary determined within the N-type drift region. Thus low doping concentration for the N-type drift region is more beneficial in order to hold the carrier from flowing between P- and N-region. The silicon P-i-N diode is designed to support large voltages, which rely upon the high level injection of minority carrier in the N-type drift region [8]. Therefore, to support a large voltage in the reverse breakdown voltage mode, an appropriate choice of doping concentration and thickness of the N-drift region needs to be made. Nevertheless, a narrower drift region is preferable because it can contain smaller amount of stored charges during the on-state operation, enabling faster turn-off.

Material substitution is one way to achieve narrower drift region thickness [9]. For example, by using silicon carbide, narrower drift region can be attained when compared to silicon devices. This is due to much larger electric field can be supported in silicon carbide. As a result, it favors a faster switching speed with reduced reverse recovery current and very high breakdown voltage can be achieved [10]. However, the high cost is a major concern, and silicon P-i-N diode still can be modified and continue to play an important role in the application, especially in medium range of breakdown voltage.

This can be explained based on expression as shown in Equation (2). The expression for V_R in this P-i-N diode can be derived by using higher critical electric field (E_C) [11, 12] Based on Figure 1 (b) (ii), E_C is the critical electric field and W_D is depletion region thickness during reverse bias. Since P-i-N diode operates in a thickness-limited mode, which is controlled by the thickness of N- region epitaxial layer, the W_D can be referred to as the thickness of the N- epitaxial layer in i-region. The V_R can be calculated as the area of the trapezium (Figure 1 (b) (ii)) as in Equation (2).

$$V_R = \frac{1}{2}\left(E_C + E_1 \right) W_D \tag{2}$$

By using the Equation (2) for the variation in the electric field with distance:

$$E_1 = E_C - \frac{q\, N_D}{\epsilon_S}\, W_D \tag{3}$$

and substituting Equation (3) in Equation (2), the V_R for the punch through diode is obtained as in Equation (4):

$$V_R = E_C W_D - \frac{q\, N_D W_D^{\,2}}{2\,\epsilon_S} \tag{4}$$

The V_R can be affected by the variable thickness of the N- region (W_D) and the doping concentration of the N-

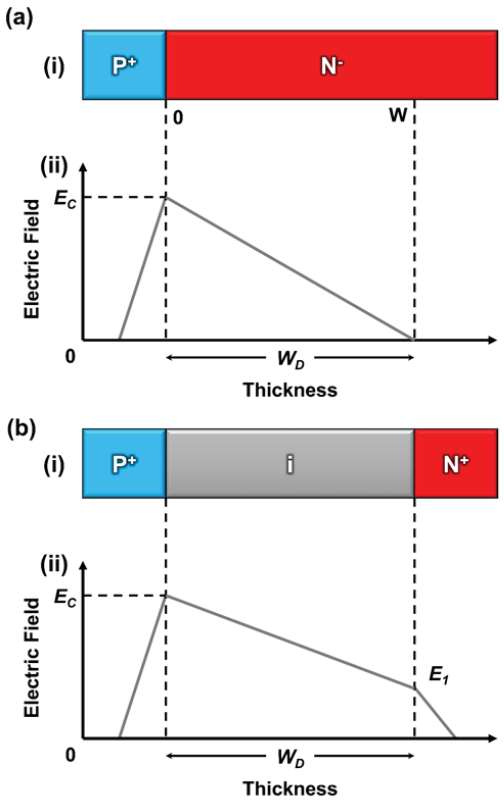


Figure 1: Comparison of ideal (a) P-N junction and (b) P-i-N diode in terms of (i) 2D structure and (ii)electrical field distribution.

epitaxial layer (N_D). The N_D can be translated into the resistivity of the N- layer [11],. The increase of the N_D results in lower resistivity.

In this paper, P-i-N diode with high resistivity N region (N- region) is used to replace the intrinsic layer. For this purpose, a commercially available 250 V P-i-N power switching diode was used to evaluate effects of N- epitaxial layer thickness (W_D) and resistivity (ρ) as the intrinsic layer effect to the P-i-N power switching diode on the performance of current-voltage (I-V) characteristic in terms of diode's V_R. The aim of this study is to have a diode that can withstand beyond 250 V for motor control, robotics and power distribution applications. The N- region is deposited on top of the wafer substrate through epitaxial process.

2 Methodology

In this work, the simulation of the P-i-N diode is performed using technology computer-aided design (TCAD) simulation software i.e. Sentaurus WorkBench, as well as the fabrication and characterization of the P-i-N diode. The P-i-N power switching diode diffuses a circular shaped boron (P+ anode junction) into an N- type epitaxial layer on a low bulk resistance N+ substrate. Another N+ diffused isolation region at the perimeter of the anode junction to reduces leakage current. The backside of the wafer is sputtered with platinum (Pt) and gold (Au). The process followed by a quick drive-in cycle for both elements, from the bulk all the way through the epitaxial layer and the P+ anode junction. Pt improves the life time cycle, reducing the reverse recovery time (t_{rr}) [13]. Au increases the epitaxial layer's t_{rr} resistance, which increases the resistance of drastic oscillation of the signal. Thus, it produces a wider P-N junction depletion region and reducing the capacitance. Figure 2 illustrates the cross-section design of the P-i-N power switching diode.

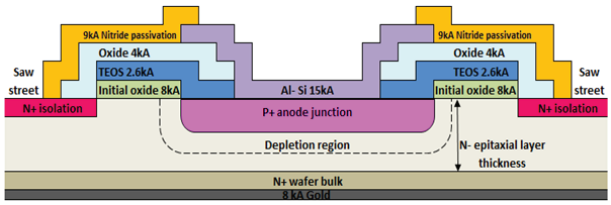


Figure 2: Cross-section structure of P-i-N power switching diode.

2.1 Numerical Simulation

The V_R of P-i-N power switching diode operates in W_D limited mode of the epitaxial layer. The first approach is to alter the W_D by adjusting the depth of the P+ anode junction through diffusion with boron as demonstrated in Figure 2. By reducing the junction diffusion drive time, a shallower anode junction is formed. With this approach, the W_D is increased [14]. However, this method has several weaknesses. The anode junction diffusion process is difficult to control, which leads to process variation. The inconsistent process temperature of diffusion furnace results in lower V_R at the edges compared to the centre of the wafers, as wafer edges tend to have a higher process temperature compared to the wafer centre [14]. Another drawback is the diffusion process is performed under a high temperature, thus caused the up diffusion from the heavily doped N+ bulk substrate. This resulted in a less favourable higher V_F [14].

The second approach is to adjust the epitaxial layer profile (W_D and ρ) of the substrate [14]. With the zero punch through structure of the P-i-N diode, as observed from the Equation (4), the W_D and N_D are dominant factors, which increase the V_R. The second approach is more favourable due to better control of wafer fabrication process.

A series of simulation and DOE is performed to show the effects of the W_D and N_D on the I-V characteristic using TCAD simulation software. The applications of TCAD simulation include technology and design rule development, as well as the extraction of compact models for manufacturability [15]. Initially, a half diode cross-section structure is designed by using SProcess. After the half diode is created, reflecting boundary conditions is applied to generate a full simulation diode model symmetrically.

For the SProcess step, a layer of phosphorus dopant (N- epitaxial) thickness is grown on top of the N+ bulk silicon substrate, which is initially doped with arsenic. The silicon substrate orientation of <100> is used. The dopant parameter is defined as @epidose@ and W_D parameter is defined as @epiThick@. With the parameters are defined in general, several W_D and doping concentrations are utilized in the simulation (Table 1) to evaluate the output response of the I-V characteristic.

Table 1: Simulation thickness and concentration dosage of N- layer.

Split	Epitaxial Layer Thickness, @epiThick@ (μm)	Epitaxial Layer Dopant Concentration, @epidose@ (cm^{-3})
a	42	1.68×10^{14}
b	42	1.58×10^{14}
c	42	1.48×10^{14}
d	42	1.36×10^{14}

e	34	1.68×10^{14}
f	34	1.58×10^{14}
g	34	1.48×10^{14}
h	34	1.36×10^{14}

The selection of the 34 µm and 42 µm thickness of W_D in simulation is due to lower and upper specification on the existing diode device epitaxial layer evaluation shown as group C in Figure 5, which will be explained in Section 2.2. The various dopant concentrations of N- epitaxial layer are selected to measure the electrical output response impact in simulation. By adjusting the phosphorus dopant concentration at the N- epitaxy layer via implantation, the ρ can be controlled, since the dopant concentration is inversely proportional with resistivity [16].

Subsequently, a 1 µm thickness of oxide layer is deposited, followed by opening of the anode area with the photolithography and etching process for electrode deposition. Next, boron is implanted with a dosage of 5×10^{15} cm^{-3}, anode junction drive in temperature and time for 1200 °C and 240 mins, respectively. After the anode junction is formed, the oxide layer is stripped off and then re-deposited with the same thickness. This re-deposited oxide layer is to react as the pattern oxide, followed by a 2 µm thickness of front metal Al layer, which act as the ohmic contact and a 1 µm thickness of Si_3N_4 nitride layer, which act as the passivation layer. All of these three layers are formed with photolithography and etching process. The final device structure is shown in Figure 3.

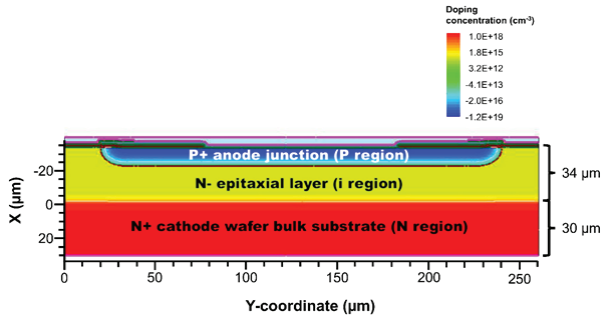


Figure 3: P-i-N diode structure with doping profile distribution.

2.2 Design of experiment and process split

Based on the simulated results, the devices are fabricated with a four corners matrix DOE to investigate the effects of W_D and ρ in order to achieve V_R above 300 V. In the fabrication process, the epitaxial layer is grown and diffused with dopant material on the wafer bulk as shown in Figure 4.

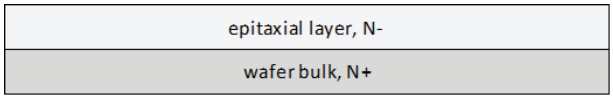


Figure 4: Wafer starting material with deposited epitaxial layer.

The DOE of the four corners matrix that includes the W_D and ρ is detailed in Table 2. As mentioned previously, the epitaxial layer dopant concentration and ρ are inter-related. The relationship between resistivity and phosphorus doping concentration has been studied for doped silicon as in [16]. Four corners matrix are groups of epitaxial layer covering the lower and upper specifications. It is used in the evaluation of the P-i-N diode performance when operating at the corners (lower or upper end) of epitaxial specifications as compared to the centre. Illustrations of total 5 groups with two level factorial DOE are shown in Figure 5 consisting of group A, B, C, D and E. The two factors (epitaxial layer thickness and resistivity) in low, centre and high condition. Design of experiments (DOE) is a systematic approach

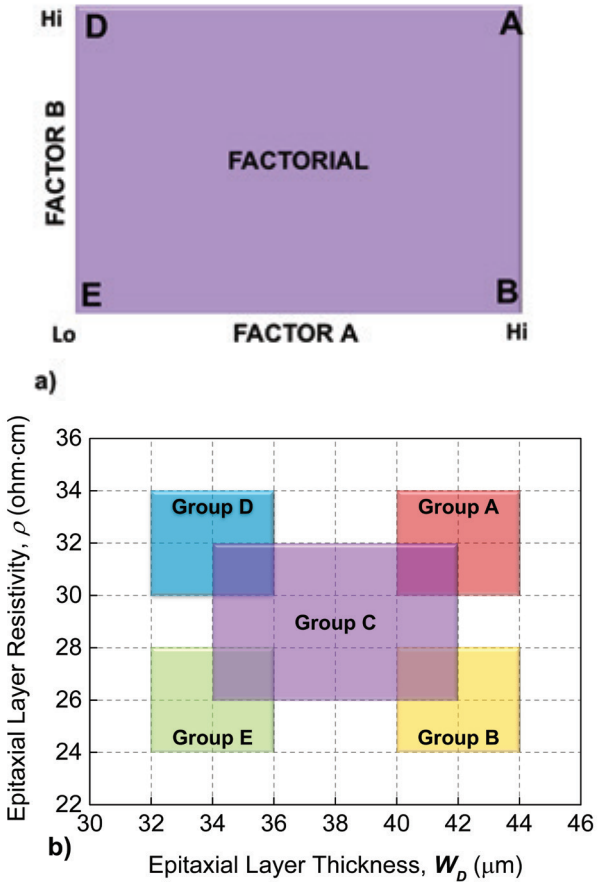


Figure 5: a) Two level factorials of DOE, Factor A and B refer to epitaxial layer thickness and epitaxial layer resistivity respectively. b) The location of four corners and centre of the evaluation samples consists of group A, B, C, D and E.

in engineering problem-solving that applies principles and techniques from the data collection stage. The output response from the data collection includes forward voltage, reverse breakdown voltage and reverse leakage current. The focus on the study is to increase the V_R during reverse bias without changing much of the V_F and I_R.

A total of 15 wafers lot are fabricated with the same P-i-N diode design at process corners with low/high W_D and low/high ρ. Afterward, the wafers are fabricated and electrically characterized. Electrical results of V_F, V_R, and reverse leakage current (I_R) are the main parameters of interest and then analysed with statistical software (for profiler study). The predicted profiler study is done to determine the dominant factor that affects the electrical performance and the optimal epitaxial profile. To ensure the repeatability of the result, each of the splits is repeated 3 times for the wafer fabrication and characterization.

3 Results and discussions

3.1 Simulation results

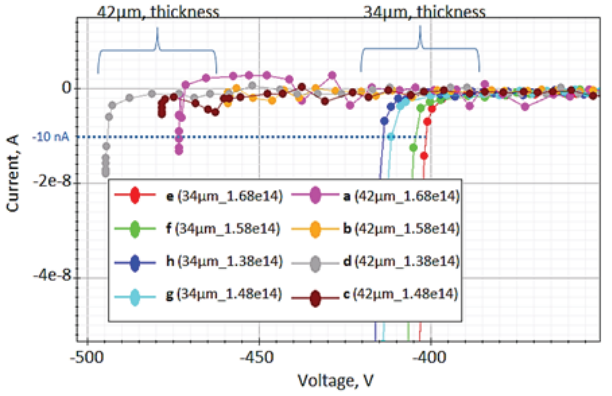
Figure 6 shows (a) reverse bias and (b) forward bias of the simulated I-V characteristics for different W_D and concentration of the N- epitaxial layer as tabulated in Table 1. In Figure 6 (a), a clear significant difference of the V_R with difference of W_D (i.e. 34 and 42 µm) is observed. At 10 nA (shown as dotted line), the 34 µm of W_D, results in lower V_R ranging from -400 V to -415 V. In contrast the 42 µm of W_D shows a higher V_R ranging from 460 V to 490 V. The increase of the W_D leads to an increment of the stored charges available and makes the diode to behave like a resistor [17]. According to Ohm's law and with the same current, the resistance is increased as a result of the increase in voltage. On the other hand, the increase of the dopant concentration N_D, from 1.38×10^{14} cm^{-3} to 1.68×10^{14} cm^{-3}, results in slight decrease of V_R. This shows that the W_D is more dominance factor affecting the V_R performance. Nevertheless, both impacts are in agreement with Equation (4) as previously explained.

Figure 6 (b) shows the forward bias results of the simulated diode. One can see that, significant impact is only related to the different W_D (i.e. 34 µm and 42 µm), while no variation can be observed for different dopant concentration. In comparison between 34 µm and 42 µm of W_D, 1) at low current of 200 mA (shown in the blue dotted line) regardless of the dopant concentration difference, V_F values of 870 mV and 880 mV, respectively. At low I_F biasing, the difference of the W_D results in a small change of V_F with the range of 10 mV difference. 2) The difference in V_F output response becomes widen

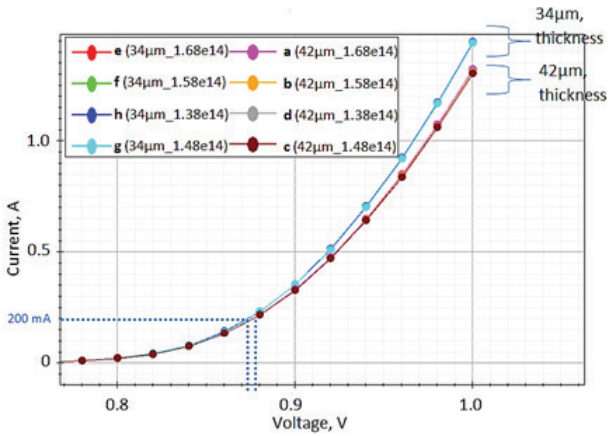
Table 2: Substrate 4 corner split table

Wafer#	Group	Description (Thickness/ Resistivity)	Target Thickness (µm)	Phosphorus dopant concentration (cm^{-3})	Conversion of dopant concentration to Resistivity (ohm·cm)	Target resistivity value (ohm·cm)	Exact Thickness value (µm)	Exact resistivity value (ohm·cm)
1	A	High / High	42	1.36×10^{14}	32.8	32	42.6	33.223
2	D	Low / High	34	1.36×10^{14}	32.8	32	34.34	30.093
3	C	Center / Center	38	1.58×10^{14}	28.2	29	37.95	28.742
4	A	High / High	42	1.36×10^{14}	32.8	32	42.6	33.223
5	D	Low / High	34	1.36×10^{14}	32.8	32	34.34	30.093
6	B	High / Low	42	1.68×10^{14}	26.6	26	42.15	26.524
7	E	Low / Low	34	1.68×10^{14}	26.6	26	33.85	25.723
8	C	Center / Center	38	1.58×10^{14}	28.2	29	37.89	28.742
9	B	High / Low	42	1.68×10^{14}	26.6	26	42.15	26.524
10	E	Low / Low	34	1.68×10^{14}	26.6	26	33.85	25.723
11	A	High / High	42	1.36×10^{14}	32.8	32	42.6	33.223
12	C	Center / Center	38	1.58×10^{14}	28.2	29	37.95	28.742
13	D	Low / High	34	1.36×10^{14}	32.8	32	34.34	30.093
14	E	Low / Low	34	1.68×10^{14}	26.6	26	33.85	25.723
15	B	High / Low	42	1.68×10^{14}	26.6	26	42.15	26.524

between various W_D with the increase of the I_F. This can be explained, when a P-i-N diode is forward biased, where holes and electrons are injected from the P and N regions into the i-region, which is represented as W_D. These charges do not recombine immediately. Instead, a finite quantity of charge always remains stored and results in a lowering of the ρ. So, the increase of I_F leads the decrease of the forward series resistance (R_S) [18]. The W_D plays a greater role to change the V_F with low resistivity.



(a)



(b)

Figure 6: I-V characteristics under (a) reverse bias and (b) forward bias for different W_D and dopant concentrations.

From the simulation, by changing the W_D and dopant concentration of the epitaxial layer, the V_R shows more significant difference compared to V_F. The reason being the P-i-N diode exhibiting reverse capacitance characteristics during reverse bias where dopant concentration and the W_D shows a more responsive curve. While forward biasing, P-i-N diode exhibits the forward series resistance characteristics where the difference of the W_D plays a greater role when the I_F is increased to a certain level [18], [19]. The phenomenon of the less responsive output on the forward bias is preferable as the focus on the study is to increase the V_R during reverse bias without changing the V_F.

With the confirmation of the theory through the TCAD simulation software, a wafer fabrication DOE has been conducted to validate the results by taking into account of the process variation and material variation.

3.2 DOE wafer results

From the DOE experimental results, in addition to V_R and V_F, and I_R are also considered. The statistical analysis, i.e. JMP profiler is used to analyse the effect of the W_D and ρ as shown in Figure 7. The line curve can be analysed by separating the two groups, which are W_D and ρ versus electrical responses. The x-axis of the chart represents the W_D, the ρ and the desirability of the responses. The curvature of the line in desirability row indicates how impactful the two factors (W_D and ρ) to the electrical output response of the device. The y-axis represents the electrical output response of V_R, V_F and I_R.

In Figure 7, W_D plays a dominant factor compared to the ρ in V_R and V_F. This is due to the V_R and V_F show more responsive curve on W_D compared to ρ. In other words, a greater gradient is observed in W_D line curve when compared to the ρ. However, the I_R change on both W_D and ρ is not significant (in nano-ampere range).

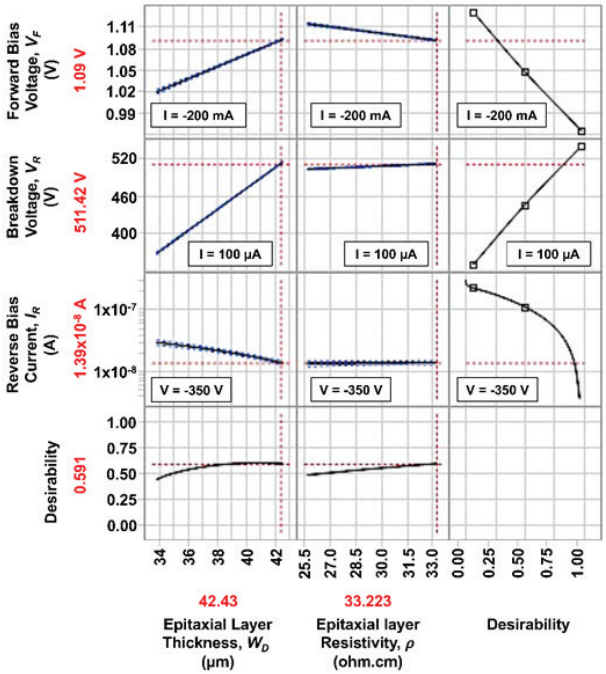


Figure 7: Statistical data on the impact of W_D and ρ on the fabricated devices.

As expected, by changing the W_D (34 µm to 42 µm), a significant difference on electrical performance for both V_F at 200 mA and V_R at 100 µA can be observed. This is related to the increase of the W_D results in the

V_R and V_F is also increased. Interesting to note that, an increase of V_F around 10 mV can be observed in Figure 7, is similar to the result obtained in simulation Figure 6 (b). With W_D increased from 34 µm to 42 µm, at 100 µA, the V_R shows almost similar response between simulations versus actual DOE. The voltage different between simulation and actual DOE is around 20 V is due to the uniformity of the boron pre deposition process.

In Figure 7, based on the statistical analysis JMP software, the V_R shows a significant improvement from 300 V to more than 500 V when replaced with W_D of 42.43 µm and the ρ of 33.22 ohm.cm.

From the DOE evaluation, both W_D and ρ in group A shows the optimum condition to achieved the desired device performance. The target W_D is 42 µm with window of 40–44 µm and the target ρ is 32 ohm·cm with window of 30–34 ohm·cm. The tolerance of ±4 µm of W_D and ±2 ohm·cm window are the narrowest tolerance, limited by process fabrication for this device. The small tolerance is preferable to reduce the process variation. With the fixed epitaxial layer substrate profile window, a total of 3 qualification lots with 5 wafers each have been fabricated in different time frames to monitor the process variation. All V_R and V_F are monitored at

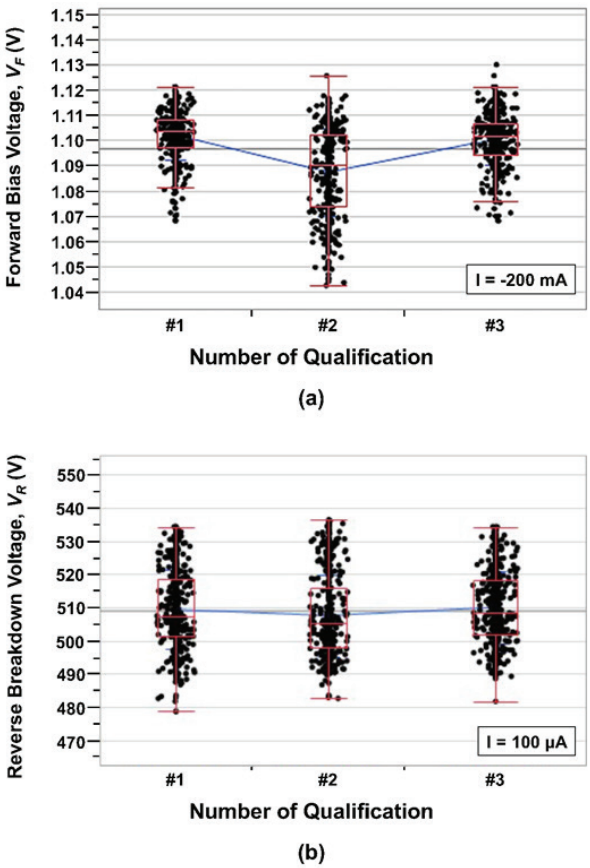


Figure 8: Qualification lot electrical distribution when (a) V_F at 200mA and (b) V_R at 100 µA.

wafer level electrical test. Based on the 3 qualification lots result shown in Figure 8, V_R and V_F electrical test result distribution are well within the specifications. The V_F distributions are less than 1.5 V and V_R distribution are above 450 V.

4 Conclusion

In summary, through the understanding of device behaviour and process TCAD simulation performance, the W_D plays a major role to increase the V_R when compared to the ρ. Further, the simulated result is validated through fabricated devices. To achieve beyond 300 V of V_R, the W_D is 42 µm and the target ρ is 32 ohm·cm.

A statistical analysis based on the electrical data was carried out to determine the best wafer substrate window. Subsequently, a validation process using 3 qualification lots is done. The V_R shows a significant improvement from 300 V to more than 500 V when replaced with the W_D of 42 µm and the epitaxial resistivity of 32 ohm·cm. The implementations of the new epitaxial specification have been successfully used to expand the product portfolio of this 300V P-i-N power switching diode that can be used in motor control, robotics and power distribution.

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