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Reliability analysis and SFG modeling of a new modified Quadratic boost DC-DC converter

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Abstract: In the present scenario, direct current boost converters play a vital role in automobiles and various industries. The direct current boost converters are designed by diverse topologies in which every topology has its benefits. The task arises in developing a converter with reduced losses, increased efficiency, robust and high gain. In this paper, a novel topology for the DC-DC conversion is proposed for high-intensity discharge lamps. The designed topology is the modified structure of the quadratic boost converter and hence named as the modified quadratic boost converter. The model, which is proposed, is more efficient with increased performance. This model is compared with an existing model, and the results are verified. The open loop small-signal analysis of the proposed topology is carried out using the switching flow graph modeling method to perform the dynamic analysis. The reliability analysis of the converter introduced is done for ensuring the lifetime operation of the converter. From reliability analysis, it is observed that the proposed topology is 14 years more reliable than the compared existing topology. It is also identified that the derived one is 6% more efficient than the compared one. A 40 W prototype, which is suitable for HID lamps, is developed to validate the theoretical results.

Keywords: MQB (Modified Quadratic Boost); voltage stress; efficiency; SFG (Switching Flow Graph); frequency domain; reliability

Zanesljivostna analiza in SFG modeliranje novega modificiranega kvadratičnega DC-DC pretvornika navzgor

Izvleček: Direktni pretvorniki navzgor danes predstavljajo pomembno vlogo v industriji. Realizirani so v različnih topologijah. V članku je predlagana nova topologija DC-DC pretvornika za uporabo v visokotlačnih sijalkah. Predlagana topologija sloni na kvadratičnem pretvorniku navzgor z izboljšanim izkoristkom in učinkovitostjo. Rezultati so preverjeni in primerjani z obstoječim modelom. Odprtozančna analiza majhnih signalov je opravljena na osnovi je opravljena z modelom grafa preklopnega poteka. Zanesljivostna analiza je pokazala, da je zanesljivostna doba predlagane topologije 14 let daljša od obstoječe topologije. Teorija je verificirana na osnovi idealnega prototipa moči 40 W, ki je primeren za napajanje HID sijalk.

Ključne besede: kvadratičen pretvornik; napetostni stres; izkoristek; SFG; frekvenčna domena; zanesljivost

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1 Introduction

In the present generation, high gain DC-DC converters find their application in various fields. Due to power crisis and shortage of electricity generations, the efficient use of the available energy in the present scenario plays a significant role [16]. In this case, DC- DC boost converters play a major role in renewable power plants. There are various topologies for the DC-DC boost converters with different drawbacks such switch voltage stress, losses in the nonlinear elements, very less voltage gain and so on. The methods to achieve high step-up, low cost, and high-efficiency DC-DC conversion constitute a significant consideration. The high-intensity discharge lamps are used in automobiles, which are powered by the batteries at low voltage. Hence, it is needed to step-up the voltage to the high level of output voltage. The operating voltage of the HID lamps is 80-90 V which cannot be achieved by conventional boost converter with 12 V supply. To achieve a highly efficient DC-DC boost conversion with reduced losses and high voltage gain, the below model is proposed with reduced number of inductors compared to the model considered for the comparison.

Various topologies had been constructed in the recent years to achieve high voltage gain for numerous applications. There are several methods to produce the high gain in DC-DC converters. Voltage multiplier cell, switched capacitor, switched inductor, voltage-lift cell, coupled inductor is integrated with the conventional DC-DC topologies to boost the voltage conversion ratio. Cockcroft and Dickson multiplier cells are used to boost the voltage of the converters. Dickson and Cockcroft multiplier cell are incorporated in the boost converter, and their performance is analyzed in [1, 2]. The gain of the converter is further increased by the adding coupled inductor to the topology, and it is reported in [3]. This leads to increase in the number of components. Boost converter integrated coupled inductors are reported in the literature [4, 5]. However, the use of multiple coupled inductors complicates the dynamic analysis of those topologies [6]. Ultra gain converters are derived by voltage lift cells which are introduced by F.L. Luo [7, 8]. However, high gain is achieved with self and relift techniques with too many components[15]. Two or more methods are integrated to attain high voltage gain and combine its advantages for better performance. The coupled inductor is combined with switched capacitor cell to derive high step-up converter, and quasi-resonant operation is employed to reduce the switching loss [9, 10]. Asymmetrical and symmetrical hybrid switched inductor converters are proposed in [11] for PV grid connected system. However, the above-mentioned topologies are derived by adding additional components to the existing converters. In this paper, we have derived a high gain converter with the simple modification in the conventional topology. The primary objective of the work is to design a DC-DC boost converter, which is more efficient in conversion with much-reduced losses, compared with an existing converter and must be suitable for meeting the requirements of high-intensity discharge lamps.

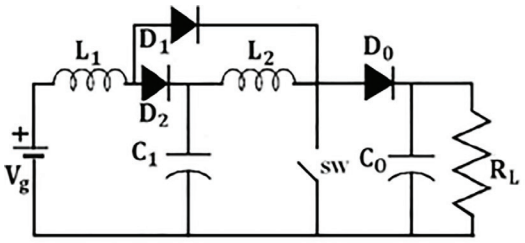
The variation in the derived topology presented in this paper is the alteration of the existing converter, i.e., Quadratic boost converter with the addition of only one capacitor and a removal of a diode [12]. The maximum stress voltage across all the components in the modified topology is found to be lower compared to the quadratic boost converter. The proposed topology is compared with quadratic boost converter and existing converter in the literature. Mostly, comparative study will be based on efficiency, voltage stress, volume, and reliability. We have compared the proposed topology with the existing topology based on reliability using FIDES guide [13]. The superiority of the proposed topology is proved based on the reliability, which is not reported in the literature until now.

The paper is organized as follows: Section 2 provides the modes of operation of the proposed topology. Section 3 gives steady-state analysis in CCM and DCM condition, the design of passive components, efficiency analysis, time domain and frequency domain analysis. The proposed topology is evaluated with the existing converters, and it is presented in section 4. Reliability study is performed on proposed topology and compared with the existing topology, and it is shown in section 5. Section 6 presents the simulation results to provide evidence to the theoretical calculation, and a prototype is raised to confirm the derived topology. Finally, the paper is terminated in section 7.

2 Structure of proposed converter

Figure 1(a) and (b) present the conventional quadratic boost converter and modified quadratic boost converter as proposed topology respectively. The modification made in the existing quadratic boost converter is the removal of one diode and addition of capacitor. The total number of devices in both the converters is same with the single switch. A number of passive components in quadratic boost converter are four, and it is five in the proposed topology. The diode count in the proposed converter is two, but it is three in the quadratic boost converter. The converter mainly comprises of two inductors, three capacitors, two diodes, resistive load, and a switch. The advantage of the modification made in the topology is discussed in section 4. Figure 2 (a) and (b) provide the mode 1 and mode 2 of the proposed topology.

(a)



(b)

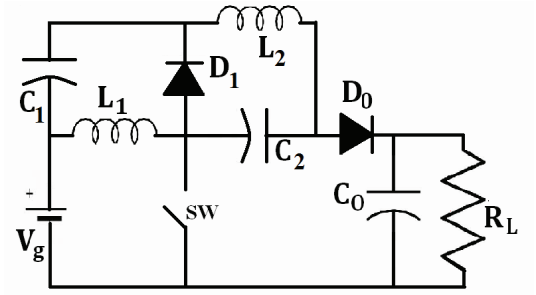


Figure 1: (a) Quadratic boost converter (b) Proposed topology

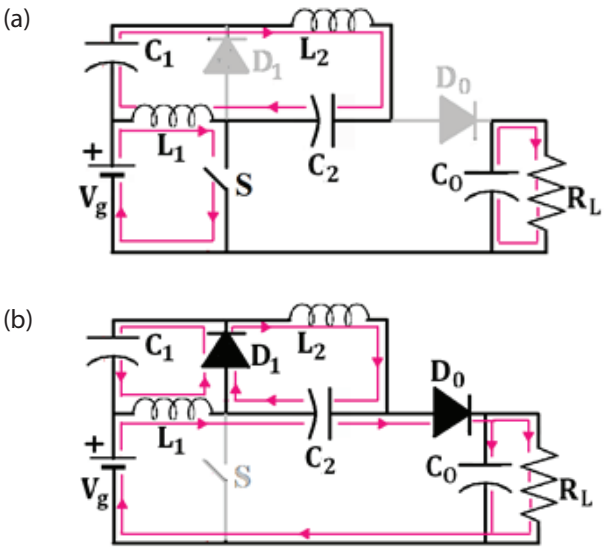


Figure 2: (a) Mode 1 (b) Mode 2

Mode 1: The states of device conduction and current path for the conducting state of the S are given in Figure 2(a). When switch SW is ON, inductor L_1 and L_2 are charged to the supply voltage V_g. Diode D_1 is reverse biased by the negative polarity of the supply voltage through the switch. Diode Do also reverse biased by the voltage across the inductor L_2. Load voltage is due to the charge in the output capacitor.

Mode 2: Figure 2(b) gives the current path when the switch S is in non-conducting state. Diode D_1 and D_O are forward biased due to the voltage of the capacitor. The inductor L_1 and L_2 started to discharge through these diodes. The output voltage is equal to the summation of the input voltage, capacitor C_1 and C_2 voltage. Figure 3 gives the current through all the passive components and diode.

3. Analysis of the proposed topology

3.1 Steady State Analysis in CCM

Voltage across the inductor L_1 and L_2 in ON and OFF mode is written as follows

$$V_{L1} = V_g \tag{1}$$

$$V_{L2} = V_g + V_{C1} - V_{C2} \tag{2}$$

$$V_{L1} = -V_{C1} \tag{3}$$

$$V_{L2} = -V_{C2} \tag{4}$$

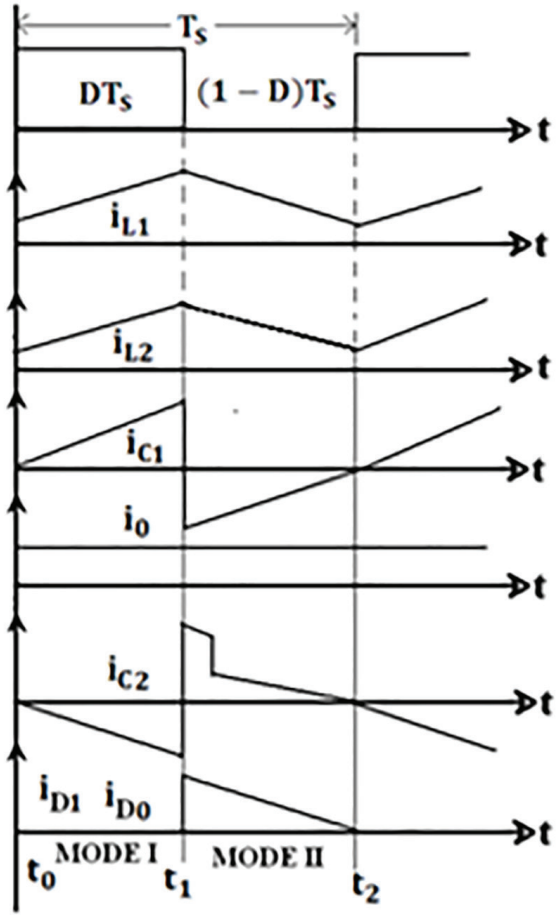


Figure 3: Current waveforms of the MQB converter

By applying volt-sec balance principle to the Equations (1)-(4), capacitor voltage C_1 and C_2 is obtained as

$$V_{C1} = V_{C2} = \frac{V_g D}{1-D} \tag{5}$$

The output voltage is given as

$$V_O = V_g + V_{C1} + V_{C2} \tag{6}$$

By simplifying the Equation (6), the voltage gain of the converter is obtained as

$$G_{VCCM} = \frac{V_O}{V_g} = \frac{1-D^2}{[1-D]^2} \tag{7}$$

Current through the capacitor C_1 and C_2 is written and by applying charge-sec balance principle, the current through the inductor L_1 and L_2 is obtained as

$$I_{L1} = \left[\frac{1+D}{1-D}\right]^2 \frac{V_g}{R_L};\ I_{L2} = \frac{1+D}{1-D}\frac{V_g}{R_L} \tag{8}$$

3.2 Boundary Conditions for Inductor L_1 and L_2

Figure 4 shows the inductor L_1 and L_2 current waveform at Discontinuous Conduction Mode (DCM) condition. The condition for inductor L_1 to operate in DCM as follows

$$I_{L1} < \frac{\Delta i_{L1}}{2} \tag{9}$$

I_{L1}= average current through the inductor L_1
Δi_{L1}= Ripple of the current through the inductor L_1

Substituting Equation (8) in (9)

$$\left[\frac{1+D}{1-D}\right]^2 \frac{V_g}{R_L} < \frac{V_g D T_S}{2L_1} \tag{10}$$

Solve the Equation (10)

$$\frac{2L_1 f_S}{R_L} < \frac{D}{G_{VCCM}{}^2} \tag{11}$$

The DCM condition for inductor L_1 is given as

for DCM $K_{L1} < K_{Crit1}$ (12)

The condition for inductor L_2 to operate in DCM as follows

$$I_{L2} < \frac{\Delta i_{L2}}{2} \tag{13}$$

I_{L2}= average current through the inductor L_2
Di_{L2} = Ripple of the current through the inductor L_2

Substituting Equation (8) in (13)

$$\frac{V_O}{R_L} < \frac{[V_g + V_{C1} - V_{C2}]DT_S}{2L_2} \tag{14}$$

Simplification leads to

$$\frac{2L_2 f_S}{R_L} < \frac{D}{G_{VCCM}} \tag{15}$$

The DCM condition for inductor L_2 is given as

for DCM $K_{L2} < K_{Crit2}$ (16)

3.3 Steady State Analysis in DCM

Applying volt-sec balance principle on inductor L_1

$$V_g D_1 - V_{C1} D_2 = 0 \tag{17}$$

Applying volt-sec balance principle on inductor L_2

$$[V_g + V_{C1} - V_{C2}]D_1 - V_{C2} D_2 = 0 \tag{18}$$

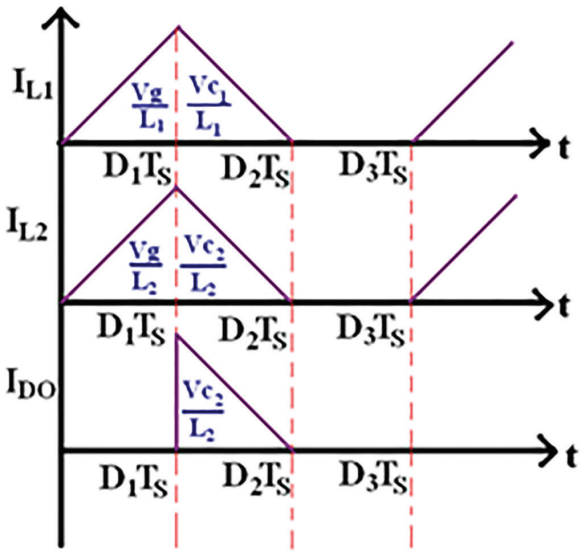


Figure 4: Inductor L_1 and L_2Current waveform at DCM

By simplifying the Equations (17) and (18), capacitor voltage is obtained as

$$\frac{V_O}{V_g} = 1 + 2\left[\frac{D_1}{D_2}\right] \tag{19}$$

Output diode DC component current must be equal to the DC load current, $I_{DO} = I_O$
The DC component of the output diode current is

$$I_{DO} = \frac{1}{T_S}\int_0^{T_S} I_{DO}(t)\,dt \tag{20}$$

According to the Figure 4, peak diode current can be obtained by multiplying the slope of the waveform with the time interval.

Simplify the integral (20) and rearrange to yield

$$\frac{V_O}{V_g} = \frac{D_1 D_2 T_S R_L}{2L_2} \tag{21}$$

Solving the Equations (19) and (21) yield the voltage conversion ratio of the proposed topology in DCM

$$G_{VDCM} = \frac{V_O}{V_g} = \frac{1 \pm \sqrt{1 + \frac{8D_1^{\,2}}{K_{L2}}}}{2} \tag{22}$$

The complete modified quadratic boost converter's conversion ratio including CCM and DCM are

$$G_V = \begin{cases} \dfrac{1-D^2}{[1-D]^2} & \ldots\ldots\ldots\ldots CCM \\ \dfrac{1 \pm \sqrt{1 + \frac{8D^2}{K_{L2}}}}{2} & \ldots\ldots\ldots\ldots DCM \end{cases} \tag{23}$$

3.4 Design of Inductor and Capacitor

Current ripple, voltage ripple, and switching frequency are required to design the passive elements of the converter. The peak-to-peak current ripple of Inductor L_1 and L_2 is given as

$$\frac{\Delta i_{L1}(DT)}{2} = \frac{V_O(1-D)D}{2(1+D)L_1 f_S} = I_{L1} \tag{24}$$

$$\frac{\Delta i_{L2}(DT)}{2} = \frac{V_O(1-D)D}{2(1+D)L_2 f_S} = I_{L2} \tag{25}$$

Using Equation (8), the design equation of Inductor L_1 and L_2 is obtained as

$$L_1 = \frac{(1-D)^2 DR_L}{2(1+D)^2 f_S};\ L_2 = \frac{(1-D)DR_L}{2(1+D)f_S} \tag{26}$$

The peak to peak voltage ripple of capacitor C_1, C_2 and C_O is calculated and rearranged to yield the design equations of the capacitor

$$C_1 = \frac{I_O D}{\Delta V_{C1} f_S};\ C_2 = \frac{I_O D}{\Delta V_{C2} f_S};\ C_0 = \frac{I_O D}{\Delta V_{CO} f_S} \tag{27}$$

3.5 Power loss and Efficiency analysis

The power losses and efficiency of the proposed topology are calculated by considering parasitic resistance, diode threshold voltage, and on-state resistance of the switch. In this calculation, R_{L1}, R_{L2} is the ESR of the inductor, R_{C1}, R_{C2} and R_{CO} are the ESR of the capacitor, R_{DS} and R_F are the on-state resistance of the switch and diode respectively. V_F is the diode threshold voltage.

RMS value of switch current:

$$I_{S(RMS)} = \begin{cases} I_{L1} + I_{L2} \ldots\ldots 0 < t < DT \\ 0 \qquad\qquad \ldots\ldots DT < t < T \end{cases} \tag{28}$$

$$I_{S(RMS)} = \sqrt{\frac{\int_0^{DT} I_{L1} + I_{L2}^{\,2} dt}{T}} = \frac{2\sqrt{D}[1+D]V_g}{R_L[1-D]^2}$$

Similarly, average and RMS currents of diodes are obtained as

$$I_{D1(avg)} = I_{D2(avg)} = I_O \tag{29}$$

$$I_{D1(RMS)} = I_{D2(RMS)} = \frac{I_O}{\sqrt{1-D}} \tag{30}$$

RMS value of capacitor current:

$$I_{C1(RMS)} = I_{C2(RMS)} = I_{C3(RMS)} = I_O\sqrt{\frac{1+D}{1-D}} \tag{31}$$

RMS values of the inductor currents are taken from Equation (8).

Total losses of the converter = $P_L + P_{SW} + P_D + P_C$

$$\begin{aligned} P_{loss} &= I_{L1}^{\,2} R_{L1} + I_{L2}^{\,2} R_{L2} + I_{S(RMS)}^{\,2} R_{DS} + \\ &+ I_{D1(avg)} V_F + I_{D1(RMS)}^{\,2} R_F + I_{D2(avg)} V_F + \\ &+ I_{D2(RMS)}^{\,2} R_F + I_{C1(RMS)}^{\,2} R_{C1} + I_{C2(RMS)}^{\,2} R_{C2} + \\ &+ I_{C3(RMS)}^{\,2} R_{C3} \end{aligned} \tag{32}$$

$$\text{Efficiency} = \eta = \frac{P_{out}}{P_{out} + P_{loss}} \tag{33}$$

3.6 Time domain and Frequency domain Analysis

3.6.1 Time domain analysis.

The important objective of investigating the time domain and frequency domain analysis of a converter is to design a control system. The desired requirement of the system can be attained by an appropriate design of control system. The converter taken for comparison combines the features of impedance source converter and quadratic boost converter [11]. This topology is derived to achieve high voltage gain. However, it can operate only with D<0.5 as positive output converter. Figure 5 gives the responses of the proposed topology and quasi Z source topology [11], which is taken for comparison. It is observed in Figure (a)-(d), the proposed topology has excellent settling time and less overshoot compared to the quasi Z source topology. The settling time of the proposed topology is just 42% of the converter taken for comparison, and the results are presented in Figure 5(c) and (d). The time domain analysis of both the converter explains the time response of the proposed converter, which takes less time for stable operation than the compared converter.

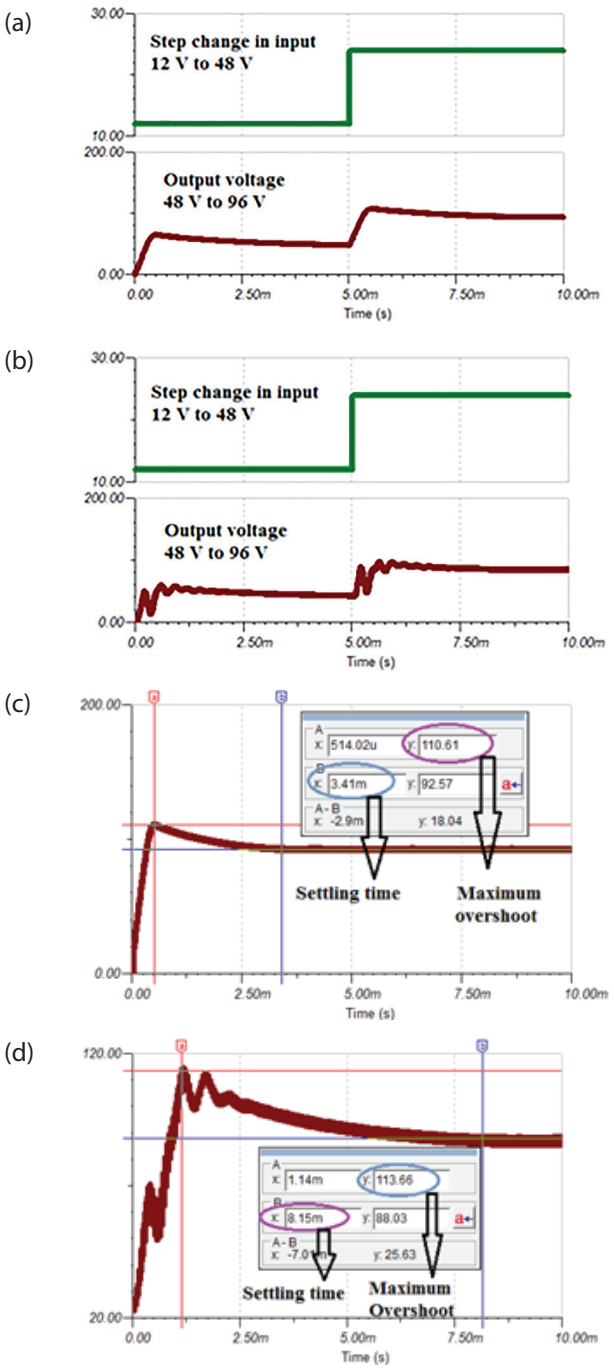


Figure 5: Time domain analysis (a) Output voltage of MQB converter for the step change in input.(b) Output voltage of Quasi Z source topology for the step change in input. (c) Settling time and maximum overshoot of MQB converter (d) Settling time and maximum overshoot of Quasi Z source topology

3.6.2 Frequency domain analysis.

To simplify the analysis, output capacitor of the converter is not considered. Order of the system is four. Figure 6 provides the signal flow graph of the MQB converter for small signal analysis.

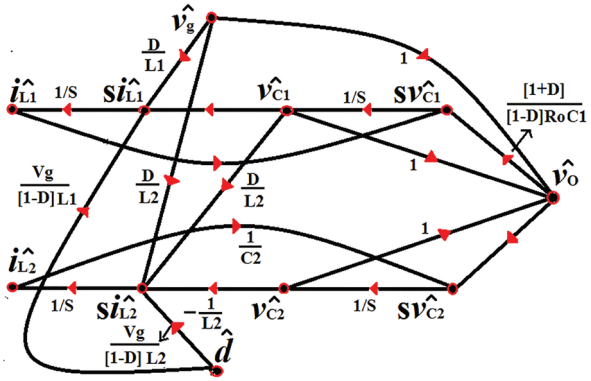


Figure 6: Small-signal analysis of MQB converter

Averaged and linearised state equations are derived using steady-state analysis to develop signal flow graph. By adding perturbation to the linearised equation, the AC equations are used to draw the signal flow graph[17]. Individual loop and non-touching loop gains are identified from the figure 6. Finally, forward path gains are traced to apply mason's gain formula to derive the transfer function.

Table 1 presents the values of the circuit parameters used for transfer function calculation to perform frequency domain analysis. Table 2 furnishes the complete frequency domain analysis of the proposed topology and the transfer functions are also provided in the table.The root locus diagram for input to output

Table 1: Circuit parameters for frequency domain analysis of the proposed topology

Po(W)	Vg(V)	Vo(V)	Ro(Ω)	fs(kHz)	L1(uH)	L2(uH)	C1(uF)	C2(uF)	Co(uF)
40	24	96	230	60	72	287	10	10	5

Table 2: Loops and their gains-SFG

Loops(L)	Loop gains	Non-touching loop gain
$L_1 = \tilde{i}_{L1} \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1} \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1}$	$I_{D2rms} = I_{DOrms} = \frac{I_O\sqrt{1-D}}{1-D}$	$L_1L_2 = \frac{-D'}{S^4L_1L_2C_1C_2}$
$L_2 = \tilde{i}_{L2} \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2}$	$L_2 = \frac{-1}{S^2L_2C_2}$	$L_1L_5 = \frac{-D'}{S^3L_1C_1C_2R_O}$
$L_3 = \tilde{v}_{C1} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2} \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2} \rightarrow \tilde{v}_O \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1}$	$L_3 = \frac{D[1+D]}{S^3L_2C_1C_2R_O[1-D]}$	$L_2L_4 = \frac{-[1+D]}{S^3L_2C_2C_1R_O[1-D]}$
$L_4 = \tilde{v}_{C1} \rightarrow \tilde{v}_O \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1}$	$L_4 = \frac{[1+D]}{SC_1R_O[1-D]}$	
$L_5 = \tilde{v}_{C2} \rightarrow \tilde{v}_O \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2}$	$L_5 = \frac{-1}{SC_2R_O}$	

Input to output transfer function

Forward paths(FP) from $\tilde{v}_g \rightarrow \tilde{v}_O$	Gain
$\tilde{v}_g \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1} \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1} \rightarrow \tilde{v}_O$	$FP_{g1} = \frac{-D}{S^2L_1C_1}$
$\tilde{v}_g \rightarrow \tilde{v}_O$	$FP_{g2} = 1$
$\tilde{v}_g \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2} \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2} \rightarrow \tilde{v}_O$	$FP_{g3} = \frac{D}{S^2L_2C_2}$
$\tilde{v}_g \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1} \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2} \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2} \rightarrow \tilde{v}_O$	$FP_{g4} = \frac{-D^2}{S^4L_1C_1L_2C_2}$

Transfer function:

$$\frac{\tilde{v}_O(s)}{\tilde{v}_g(s)} = \frac{\sum FP_{gK}\Delta_K}{\Delta} = \frac{FP_{g1}[1-L_2] + FP_{g2}[1-L_1-L_2] + FP_{g3}[1-L_1] + FP_{g4}}{1-L_1-L_2-L_3-L_4-L_5+L_1L_2+L_1L_5+L_2L_4}$$

Control to output transfer function

Forward paths(FP) from $\tilde{d} \rightarrow \tilde{v}_O$	Gain
$\tilde{d} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2} \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2} \rightarrow \tilde{v}_O$	$FP_{g1} = \frac{V_g}{S^2[1-D]L_2C_2}$
$\tilde{d} \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1} \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2} \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2} \rightarrow \tilde{v}_O$	$FP_{g2} = \frac{-V_g}{S^4[1-D]L_1C_1L_2C_2}$
$\tilde{d} \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1} \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1} \rightarrow \tilde{v}_O$	$FP_{g3} = \frac{-V_g}{S^2[1-D]L_1C_1}$

Transfer function:

$$\frac{\tilde{v}_O(s)}{\tilde{d}(s)} = \frac{\sum FP_{gK}\Delta_K}{\Delta} = \frac{FP_{g1}[1-L_1] + FP_{g2} + FP_{g3}[1-L_2]}{1-L_1-L_2-L_3-L_4-L_5+L_1L_2+L_1L_5+L_2L_4}$$

and control to output transfer function are shown in Figure 7(a) and (c) respectively. Magnitude and phase plot for both the derived transfer functions are given in Figure 7(b) and (d) . From root locus in Figure 7(a), it is observed that the input to output transfer function has two complex poles and zeros and two real poles and zeros. One real pole and zero lie in the right half of the s-plane. Similarly, the control to output transfer function has two complex poles, two complex zeros and two real poles.One real pole lies in the right half of the s-plane. The status of pole-zero locations is given in Table 3.

Table 3: Poles and zeros of the open loops transfer function

Input to output transfer function				
Poles and zeros	Values	Damping	Overshoot (%)	Frequency (rad/sec)
Poles(4)	$2.6x10^4$	-1	0	$2.6x10^4$
	$-416+1.87x10^4i$	0.0223	93.2	$1.87x10^4$
	$-416-1.87x10^4i$	0.0223	93.2	$1.87x10^4$
	$-2.25x10^4$	1	0	$2.25x10^4$
Zeros(4)	$3.12x10^4$	-1	0	$3.12x10^4$
	$-2.18x10^4i$	0	100	$2.18x10^4$
	$+2.18x10^4i$	0	100	$2.18x10^4$
	$-3.12x10^4$	1	0	$3.12x10^4$
Control to output transfer function				
Poles and zeros	Values	Damping	Overshoot (%)	Frequency (rad/sec)
Poles(4)	$2.6x10^4$	-1	0	$2.6x10^4$
	$-416+1.87x10^4i$	0.0223	93.2	$1.87x10^4$
	$-416-1.87x10^4i$	0.0223	93.2	$1.87x10^4$
	$-2.25x10^4$	1	0	$2.25x10^4$
Zeros(2)	$3.05x10^4$ $x10^4i$	0	100	$3.05x10^4$
	$-3.05x10^4$ $x10^4i$	0	100	$3.05x10^4$

By investigating the bode diagram of $\tilde{V}_{\dot{O}}(s)/\tilde{V}_{\dot{g}}(s)$, it is understood that the magnitude curve of the function starts with a gain of 7.62 dB at $1.02X10^3$ rad/sec and the magnitude curve slope becomes -40 dB/dec. The phase curve has a phase reduction of -180°, so the curve reduced from 360° to 180°. Similarly, the magnitude and phase plot continue accordingly to the values of poles and zeros. Due to the presence of zero in the right of the s-plane and low value of phase margin, the system exhibits non-minimum phase behavior. Bode plot of the duty cycle to output transfer function is similar to previous transfer function bode plot except the phase margin is 0.0237°.

4 Advantages of the proposed converter

The proposed topology is compared with the quadratic boost converter and quasi Z source topology proposed in [11]. Even though the gain of the proposed converter is less compared to the quadratic boost converter for the same duty cycle, MQB converter's performance is superior compared to other two converters taken for the same power and voltage rating. Table 4 gives all the theoretical formula derived for the proposed topology and is tabulated along with the quasi z-source and the quadratic boost converter. Figures 8(a)-(d) furnishes the comparative graphs of the MQB converter with other converter taken for comparison. Figure 8(b) endows the capacitor voltage stress for different output voltage rating. The proposed converter has very low buffer capacitor stress compared to another converter.

Switch and diode voltage stress is determined using switch utilization (SUF) and diode utilization factor (DUF)

$$\text{SUF or DUF} = \frac{P_{rated}}{\sum_{M=1}^{n} V_M I_M} \tag{34}$$

Where V_M = voltage stress across the switch or diode.

I_M = current stress through the switch or diode.

Switch and diode utilization factors are calculated using the equation (34). From the Figure 8(c), it is observed that the SUF of the MQB converter is 1.7 and 2.7 times of the quadratic boost and quasi z-source topology respectively. Similarly, from the Figure 8(d), it is detected that the DUF of the MQB converter is 1.8 and 4.7 times of the quadratic boost and quasi z-source topol-

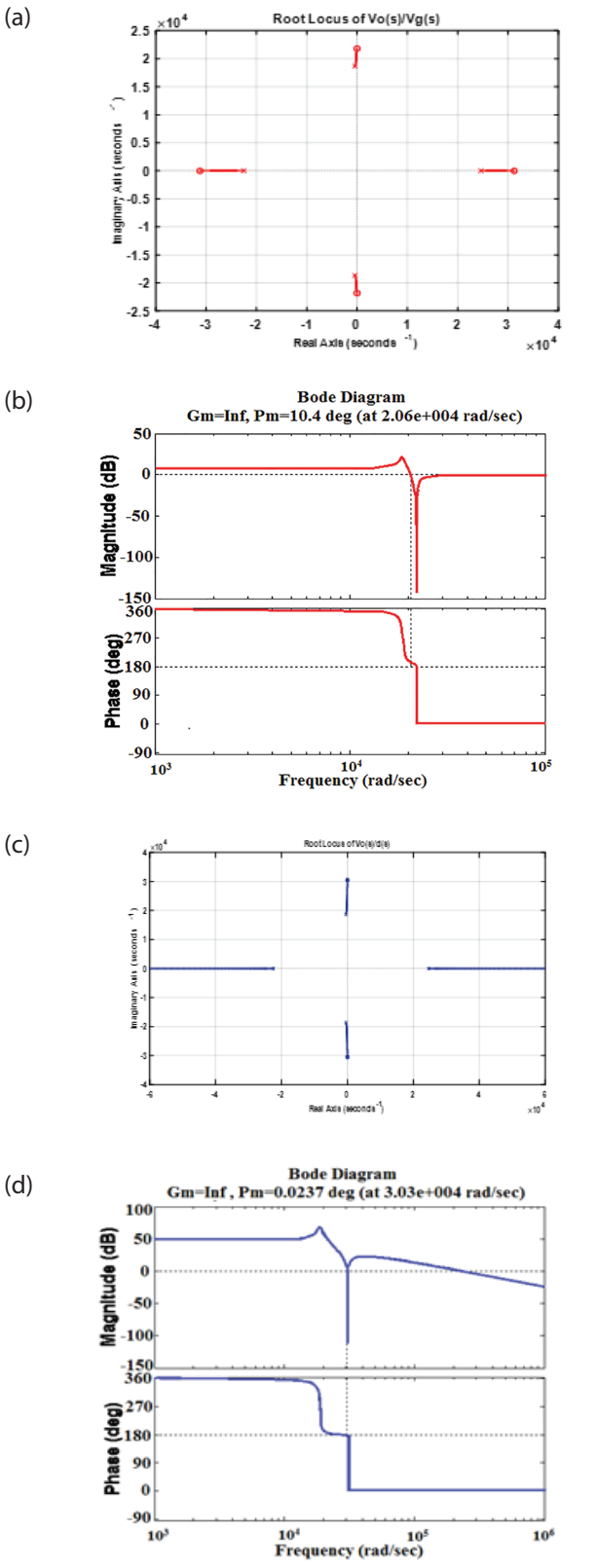


Figure 7: Frequency domain analysis (a) Root locus diagram of input to output transfer function (b) bode plot of input to output transfer function (c) Root locus diagram of control to output transfer function (d) bode plot of control to output transfer function

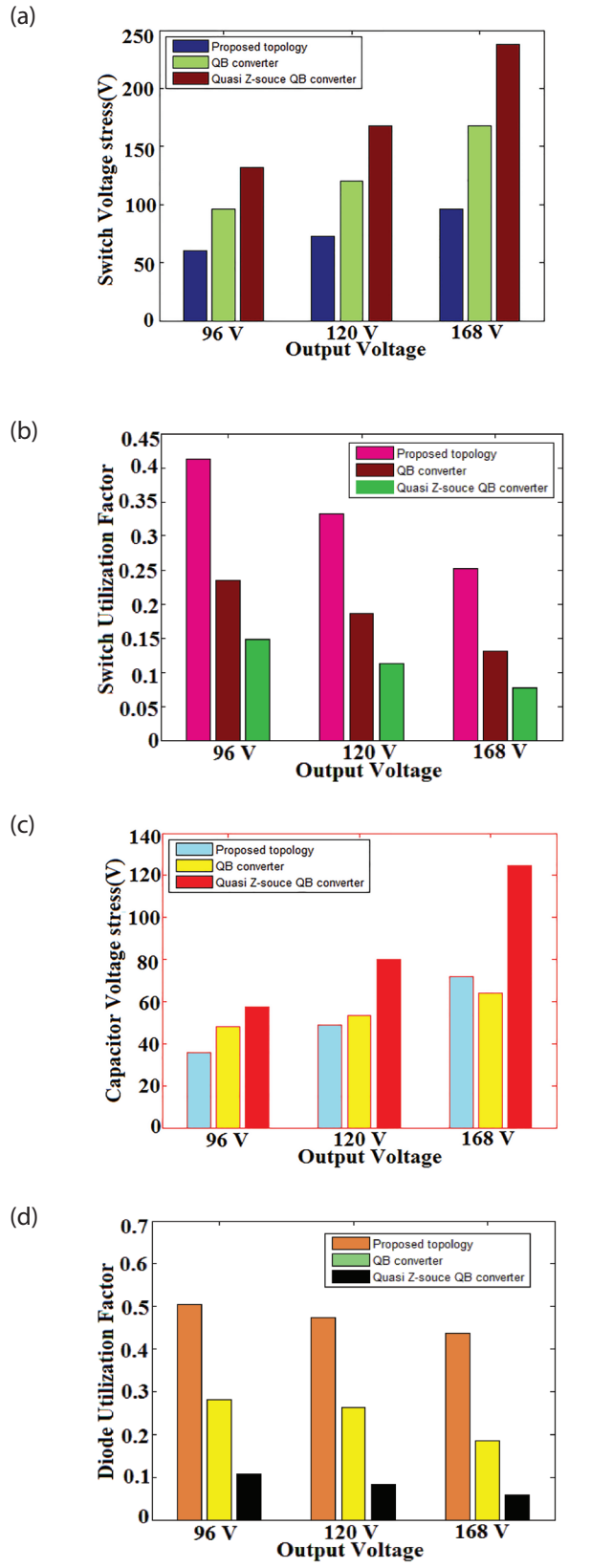


Figure 8: (a) Output voltage Vs switch voltage stress (b) Output voltage Vs capacitor voltage stress (c) Output voltage Vs switch utilization factor (d) Output voltage Vs diode utilization factor

ogy respectively. The proposed converter is also compared with the converter in [14]. It is observed that the gain of the converter in [14] is just similar to the proposed converter. The converter [14] achieves the same

Table 4: comparison of proposed converter with existing topology

Sno	Parameter	Proposed Topology	Quadratic boost converter	Quasi Z-source topology[11]
1	Voltage gain	$\frac{1-D^2}{(1-D)^2}$	$\frac{1}{[1-D]^2}$	$\frac{1}{1-2D}$
2	Inductor design	$L_1 = \frac{R_O[1-D]^2 D}{2[1+D]^2 f_S}$ $L_2 = \frac{R_O[1-D]D}{2[1+D]f_S}$	$L_1 = \frac{R_O[1-D]^4 D}{2f_S}$ $L_2 = \frac{R_O[1-D]^3 D}{2f_S}$	$L_1 = \frac{R_O[1-2D]^2 D}{2f_S}$ $L_2 = \frac{R_O[1-2D]D}{2[1-D]f_S}$ $L_3 = \frac{R_O[1-2D]}{2f_S}$
3	Switch voltage stress	$\frac{V_g}{1-D}$	V_O	$\frac{V_g[1+D]}{1-2D}$
4	Switch current stress	$\frac{2\sqrt{D}I_O}{1-D}$	$\frac{[2-D]\sqrt{D}I_O}{[1-D]^2}$	$\frac{2\sqrt{D}I_O}{1-2D}$
5	Diode current stress	$I_{D1rms} = I_{DOrms} = \frac{I_O}{\sqrt{1-D}}$	$I_{D1rms} = \frac{I_O\sqrt{D}}{[1-D]^2}$ $I_{D2rms} = I_{DOrms} = \frac{I_O\sqrt{1-D}}{1-D}$	$I_{D1rms} = I_{D3rms} = \frac{I_O\sqrt{1-D}}{1-2D}$ $I_{D1rms} = \frac{I_O\sqrt{D}}{1-2D}$
6	Capacitor Voltage stress	$V_{C1} = V_{C2} = \frac{V_g D}{1-D}$	$V_{C1} = \frac{V_g}{1-D}$	$V_{C1} = \frac{V_g}{1-D}$ $V_{C2} = \frac{V_g D}{[1-D][1-2D]}$
7	Diode voltage stress	$V_{D1} = V_{DO} = \frac{V_g}{1-D}$	$V_{D1} = V_{D2} = \frac{V_g}{1-D}$ $V_{DO} = V_O$	$V_{D1} = \frac{V_g}{1-D}$ $V_{D2} = \frac{2DV_g}{[1-D][1-2D]}$ $V_{D3} = \frac{V_g}{[1-D][1-2D]}$
8	Total device count	3-Diode;1-Switch; 2-Inductor 2-Capacitor	2-Diode;1-Switch 2-Inductor; 3-Capacitor	3-Diode;1-Switch;3-Inductor; 2-Capacitor
SUF(Switch Utilization Factor)(P_O = 40 W, V_g = 24 V, V_O = 96 V)				
9	SUF	0.412	0.235	0.148
DUF(Diode Utilization Factor)(P_O = 40 W, V_g = 24 V, V_O = 96 V)				
10	DUF	0.505	0.282	0.107

voltage conversion ratio with four capacitors whereas, with the proposed topology, it is three capacitors. The MQB converter possesses a total component count of 8 whereas the converter [14] has nine devices with 3-diodes, 4- capacitors, 2-inductors and a switch. Switch voltage stress in both the converters is observed to be same and it is measured by the equation Vg/[1-D].

5 Reliability study of the proposed converter

Reliability analysis is carried out with the help of FIDES guide [13]. Fides is a guide used for reliability computation of electronic components and structures. The reliability prediction is usually stated in FIT (number of failures for 10^9 hours). It is composed of two parts such as reliability evaluation and audit guide. It takes account of the mechanical and electrical stresses. In addition to that, it takes the complete life profile of the system. Reliability calculation helps to predict the failure rate of the converter by considering all the factor of the converter when it is integrated with the application. The reliability analysis is started by predicting the life profile of the converter used in trucks. The conditions such as operating time of the converter, the location of the application, the type of atmosphere where the converter is to be integrated, and the type of use must be tabulated which would be further used in the reliability prediction as in Table 5. In India, trucks are allowed to run only during night hours to avoid traffic. According to the traffic rules, life profile of the converter is designed.

The main objective of the reliability study is to calculate the mean time to failure (MTTF) of a converter when it is integrated into the application. The failure rates of every component that are incorporated in the converter circuit are to be calculated to find the mean time to failure. The failure rate that is calculated from the predictions are expressed in FIT (FIT = failure in 10^9 hours). The MTTF is calculated by the below equation.

$$\mathrm{MTTF} = \frac{1}{\lambda_S + \lambda_D + \lambda_C + \lambda_I} \tag{35}$$

λ is the symbol of failure rate and the general equation for calculating the failure rate is given in Equation (36). The failure rates are calculated for the capacitor, inductor, switch, and diodes.

$$\lambda = \lambda\mathrm{physical}.\ \Pi\mathrm{pm}.\ \Pi\mathrm{process} \tag{36}$$

The component junction temperature is calculated as below,

$$T_{j-comp} = T_{ambient} + R_{JA}.P_{dissipated} \tag{37}$$

In Equation (37), the power dissipation denotes the losses occurring in the diode and switch which are given in Equations (37) and (38).

$$P_{d1} = P_{dO} = \frac{V_f \times P_o}{V_o} + \frac{P_o^{\,2}}{(1-D)V_o^{\,2}}.R_f \tag{38}$$

$$P_{SW} = P_o^{\,2}\left\{\frac{4\,D\,R_{ds(on)}}{V_o^{\,2}(1-D)^2} + \frac{f_s.C_o}{(1-D)^2 I_o^{\,2}}\right\} \tag{39}$$

Table 5: Life profile of the converter

Condition		Temperature and humidity			Temperature cycling			
Phase title	Time (hrs)	On/Off	Ambient temp (˚C)	Relative humidity (%)	ΔT(˚C)	No of cycle (/ year)	Cycle duration (hrs)	Max temp during cycling (˚C)
Night/ on	3660	on	125	22	25	305	12	150
Day/ off	4380	off	35	20	10	365	12	45
Night/ off	720	off	30	30	5	60	12	35

Table 6: Specifications of the components

Component	Model no	Description
Diode	MUR510	TO-220AC [R_{JA} = 30 °c/w]
Switch	IRF 520	TO-220 [R_{JA}= 62.5 °c/w, Rds(on)= 0.23 Ω]
Capacitor	Aluminium solid electrolyte capacitor	[100V, 5A] 10-20 μF; Resr = 0.2 to 0.5 Ω
Inductor	Toroid, powered iron core wire wound inductor	17 μH, (Resr = 0.009 Ω) 303 μH (Resr = 0.091 Ω

The Table 6 shows the specifications of the components that are selected. From the stress values and the base failure rate values of the components, the failure rate value is calculated and tabulated in Table 7 along with the failure rate values of the compared quazi z source converter, which is calculated similarly.

Table 7: Failure rate values of components

Failure Rate	Proposed MQB Converter	Compared Quazi z converter
λ_S	384.04	451.1853
λ_D	2863.92	5037
λ_I	3.026	4.539
λ_C	101.304	110.4

The above failure rate values are used in the Equation (35) to calculate the mean time to failure of the converter which is given below.

For the proposed modified quadratic dc-dc boost converter,

$\lambda_S + \lambda_D + \lambda_C + \lambda_I = 3352.2787$ FIT

MTTF = 34.05 years

For the compared quadratic quazi z source converter,

$\lambda_S + \lambda_D + \lambda_C + \lambda_I = 5603.1243$ FIT

MTTF = 20.37 years

Thus from the reliability analysis, the mean time to failure is calculated. When comparing both the converters, the proposed modified quadratic boost converter can work without failure for nearly 14 year more than the compared converter due to the lesser number of component counts and reduced losses in the components. While including the controller circuit and the gate driver circuit the value might vary depending upon the methods used.

6 Simulation and experimental results

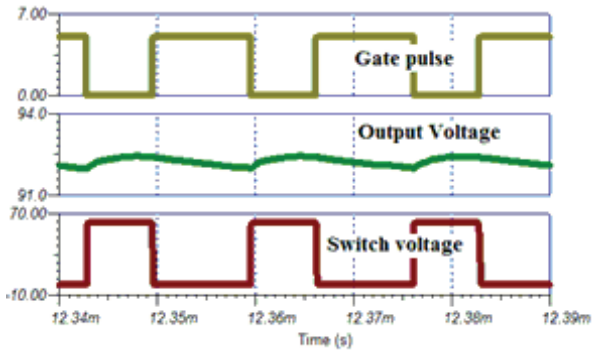
Simulation is carried out with Tina software and presented in the Figures 9(a)-(g). The proposed topology is simulated in Tina design suite TI version 9. The circuit response to the input voltage is calculated in the transient and mixed mode of Tina. In a transient analysis, the DC operating point can be calculated which is used to check with the theoretical results obtained from the steady-state analysis. By comparing the simulation results and the theoretical results, the values are more satisfactory. The voltage across the inductors and capacitors during turn ON and turn OFF period are same as that of the theoretical values. The calculated voltage gain and capacitor voltage by volt-second balance principle are more accurate to the simulation results.
(a) (b)

Figure 9(h) gives a pictorial representation of the efficiency between the converters, in the form of the graph. The efficiency analysis of converter is carried out by estimating the losses in the conversion process. The losses are mainly due to switching frequency, power diodes, passive elements such as inductor and capacitors. The output power versus the efficiency is plotted, and we infer from the graph that the converter's efficiency decreases with increase in the power ratings, but the rate of decrease in efficiency varies. The rate of decrease of the efficiency is less in proposed converter when compared to the compared converter. From the efficiency and loss analysis, it's more obvious that the proposed converter is much dominant than the compared converter.

Figure 10 shows the hardware that is developed for the converter proposed. The dsPIC controller generates a switching pulse of 5 V amplitude and 20 kHz frequency. A power supply of 230 V is given to the transformer, which is stepped down to 15 V and 40 V respectively. 15 V is given to the dsPIC controller kit, and 40 V is given to the bridge rectifier circuit. The rectifier converts the 40 V AC to 40 V DC, which is given to the converter for input supply. The 15 V AC is again stepped down to 5 V

Table 8: Components of hardware circuit

Parameters		Components	
Input voltage	40 V	Switch	IRF520
Output power	40 W	Diode	MUR510
Switching frequency	20 kHz	Inductor	400 uH, 1 mH
Output voltage	93 V	Capacitor	10 uF
Duty cycle	0.4	dsPIC Controller	dsPIC33FJ64MC802
		Gate driver circuit	IRS2110



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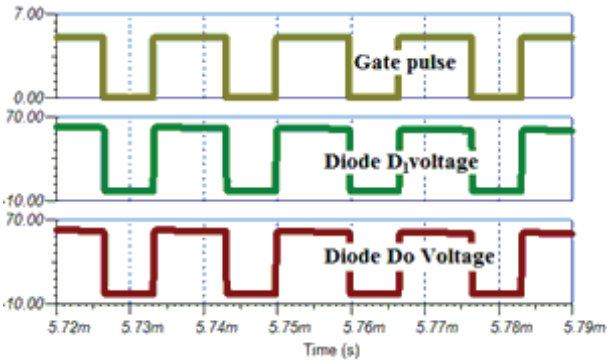

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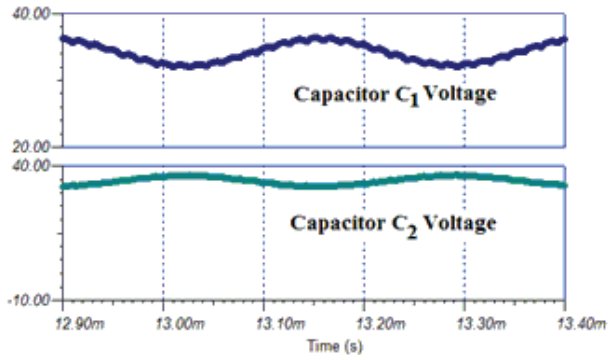

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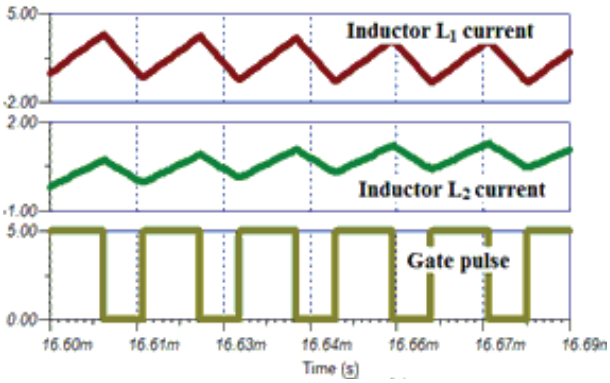

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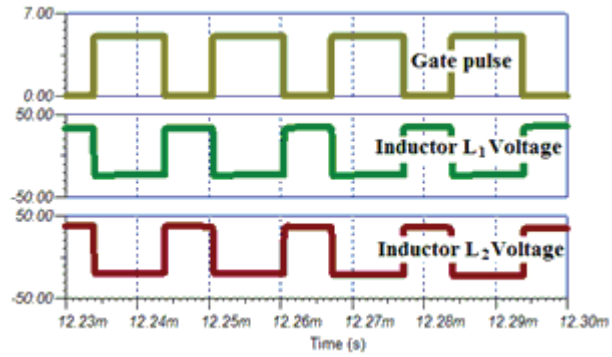

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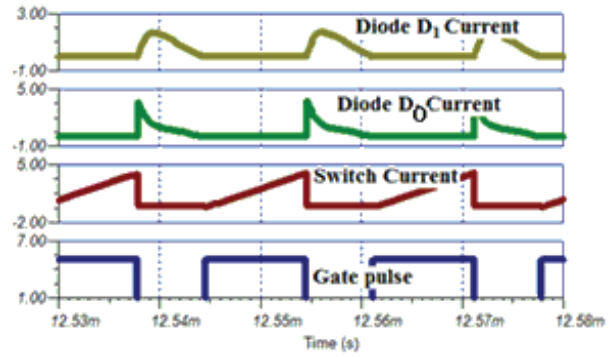

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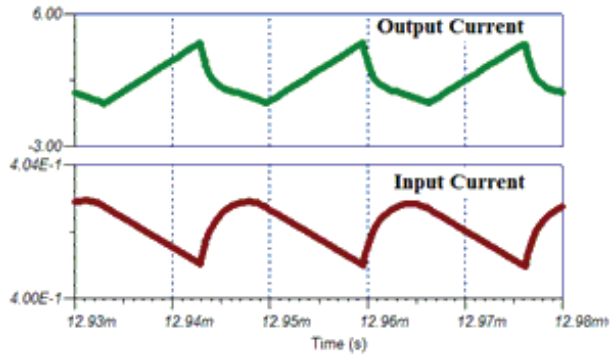
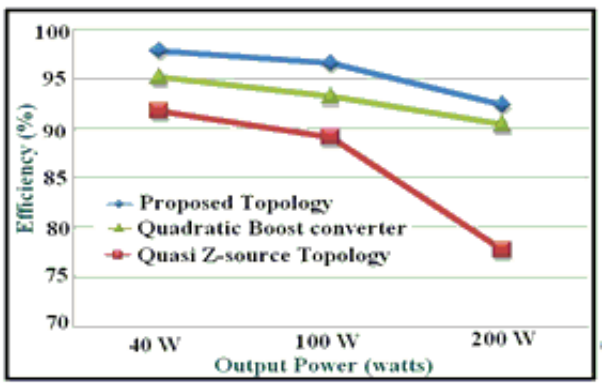


(g)



(h)

Figure 9: Simulation results (a) Output and Switch voltage (b) Diode voltages (c) Capacitor voltages (d) Inductor currents (e) Inductor voltages (f) Switch and diode currents (g) Input and output currents (h) output power Vs Efficiency.

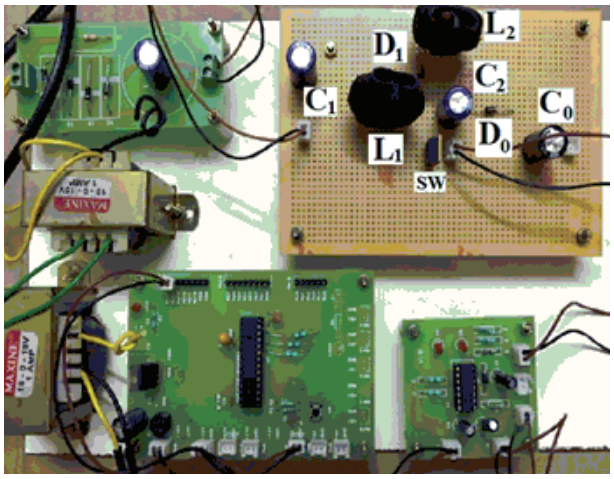


Figure 10: Photograph of the hardware

as a power supply to the controller and the gate driver circuit. Table 8 gives the components and parameters used for the hardware circuits

The Figure 11(a) shows the switching pulse waveform generated from the dsPIC controller with 0.4 duty cycle. The ON time of the switch is hence 40 % and the OFF time is remaining 60%. Thus for that duty cycle, the boost ratio is 2.33 and the output voltage for 40 V input is 90 V. The Figure 11(b) shows the input and output waveforms of the converter. The input voltage given to the converter is 40 V and the output voltage of the converter is 90 V. The channel 2 shows the output voltage and the channel 1 shows the input voltage. The voltage across the switch connected to the converter model is taken between drain and source and given in Figure 11(c). Theoretically, by $\frac{V_g}{1-D}$ the maximum switch voltage is 66 V, and it is observed that the hardware switch voltage is very close to the theoretical value. However, conventional quadratic boost converter has switch voltage stress equals to its output voltage. The proposed topology with low switch voltage stress uses low $R_{ds(on)}$ switches which reduces the cost of the component. A closer inspection shows that the hardware results validate the simulation and theoretical results. To increase the voltage gain, the coupled inductor can be incorporated. Thus, the proposed converter can be extended in the future for further increase in voltage conversion ratio.

7 Conclusion

The proposed topology for the operation of high-intensity discharge lamps has been described in this work. The same topology can be operated with PV source as an input. The converter is more suitable to

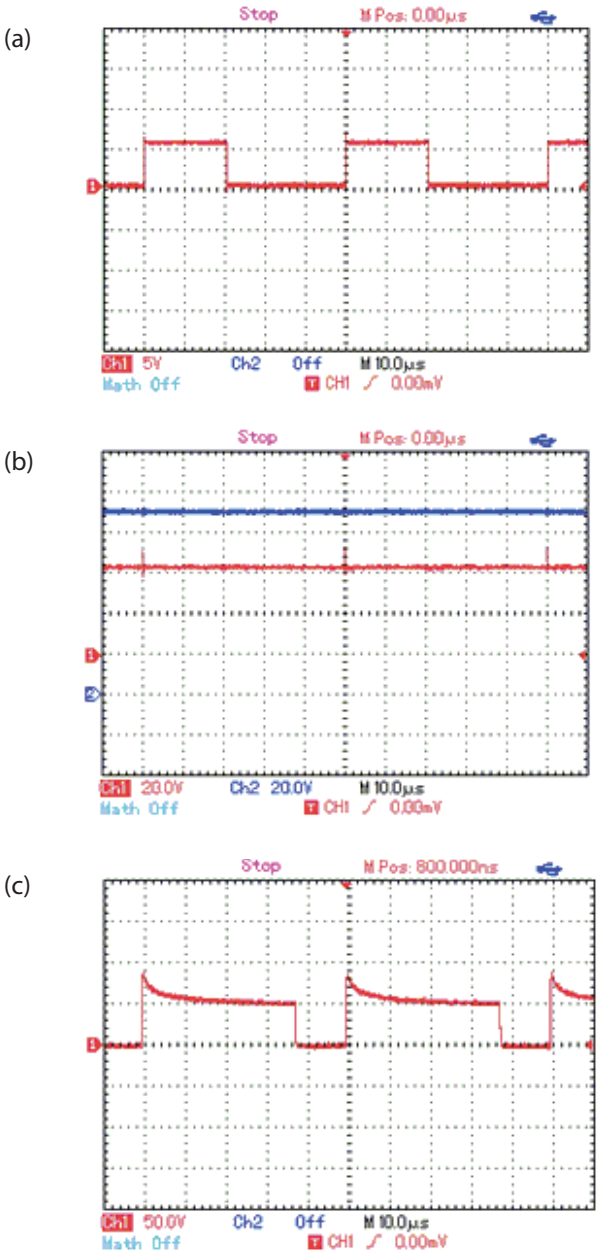


Figure 11: Experimental results (a) Gate pulse (Amp: 5 V/div; Time period: 10us/div) (b) Input and output voltage (Input voltage: Ch1: Amp: 20V/div; Time period: 10us/div; Output voltage: Ch2: Amp: 20V/div; Time period: 10us/div) (c) Voltage across the switch

be operated for lower power ratings and the efficiency decrease slightly with the increase in the power ratings. The output response with variation of input supply is studied in open loop conditions. The attractive features of the MQB converter are:

It has low buffer capacitor voltage stress.

SUF of the proposed converter is approximately 2-3 times greater than that of the compared converter.

Similarly, DUF of the MQB converter is 2-5 times higher than the converter taken for comparison. SUF and DUF of the proposed topology are very high compared to another converter. Therefore, it allows us to choose low rating semiconductor devices and which results in low cost of the devices.

The efficiency of the proposed converter is 6% higher as that of the compared converter for 40 W power rating, and the results of the output voltage and current make it more suitable for operation of the high-intensity discharge lamps.

The reliability of the MQB converter is about 15 years more reliable than the compared converter. The reliability analysis of the converter, when compared with the existing converter, shows that it is more reliable.

The hardware developed for the converter shows a satisfactory result for the voltage gain, which is found theoretically .In the future work, bidirectional version of the converter can be developed with the controller. The reliability analysis can be done for the gate driver circuit and the controller circuit so that it would give better details about the reliability analysis.

8 List of symbols and abbreviations

S	MOSFET switch
L_1, L_2	Inductor
C_1, C_2, C_O	Capacitors
R_L	Output resistor
D_1, D_O	Diodes
Vg	Input voltage
V_O	Output voltage
V_{L1}, V_{L2}	Inductor voltage
I_{L1}, I_{L2}	Inductor current
V_{C1}, V_{C2}	Capacitor voltage
D	Duty cycle
f_S	Switching frequency
G_{VCCM}	Voltage gain in CCM
G_{VDCM}	Voltage gain in DCM
Δi_{L1}, Δi_{L2}	Ripples in the inductor current
ΔV_{C1}, ΔV_{C2}	Ripples in the capacitor voltage
K_{crit1},K_{crit2}	Critical value of K at the boundary between the modes for L_1 and L_2
MQB	Modified quadratic boost
SFG	Switching flow graph
HID	High-intensity discharge
SUF	Switch utilization factor
DUF	Diode utilization factor
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
K_{cric1},K_{cric2}	Critical value decides CCM and DCM
$I_{S(RMS)}$, $I_{D(RMS)}$,	Switch and diode RMS current
$I_{D1(avg)}$, $I_{DO(avg)}$	Diode average current
$I_{L1(RMS)}$, $I_{L2(RMS)}$	Inductor RMS current
$I_{C(RMS)}$	Capacitor RMS current
P_{LOSS}	Power loss of the components
P_{out}	Output power
L_1, L_2…	Loop gains of signal flow graph
FP	Forward path in SFG
Gm	Gain margin
Pm	Phase margin
λ	Item failure rate
$\lambda_{Physical}$	Physical contribution
Π_{PM}	Part manufacturing
T_j	Component junction temperature (°C)
R_{JA}	Junction to ambient thermal resistance (°C/W)
MTTF	Mean Time to Failure

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