

Design of Priority Based Reconfigurable Router in Network on Chip

D. David Neels Ponkumar¹, V. Sushmitha², K.Saravanan³

¹Dr. Sivanthi Aditanar College of Engineering, Department of Electronics Communication Engineering, Tamil Nadu, India

²Chandy College of Engineering, Department of Electronics and Communication Engineering, Tamil Nadu, India

³SAINTGITS College of Engineering and Technology, Department of Electronics and Communication Engineering, Kerala, India

Abstract: Network on Chip (NoC) is an advanced integration design for communication networks while providing a solution to the traditional bus based System on Chip designs (SoC) too. A router is a key component which is considered as the backbone of communication in NoC. The objective of this work is to design a priority based reconfigurable router for NoC. Initially, a 4x4 Baseline router is designed and synthesised and then the channels inside the router are modified to achieve reconfiguration to improve the router's efficiency. In 4x4 Reconfigurable Router the slots are well utilized but prioritization portion is not considered. Routers are associated with switches to take data transfer decisions resulting in high power consumption. In order to overcome this problem, a new priority based reconfigurable router is designed. The design for this router is carried out using Verilog HDL and synthesised and simulated using Xilinx ISE Design Suite 14.3 and ModelSim-Altera 6.5b Software respectively. The corresponding results in terms of power, energy efficiency, area and delay are analysed and the proposed work gives better results than the conventional Baseline Router.

Keywords: Router; NoC; On Chip Power; Area; Energy Efficiency; Delay; Priority; Reconfigurable Router

Dizajn prioritetno nastavljivega usmerjevalnika v omrežju na čipu

Izvleček: Omrežje na čipu (NoC) je napredna integracija komunikacijskih omrežij z uporabo tradicionalnih sistemov na čipu na osnovi vodil (SoC). Usmerjevalnik predstavlja ključno komponento v komunikaciji preko NoC. Namen dela je razvoj prioritetno nastavljivega usmerjevalnika za NoC. V osnovi je uporabljen 4x4 usmerjevalnik, v kateremu so, za doseganje učinkovitosti, kanali naknadno razširjeni. Reže v nastavljivem usmerjevalniku so dobro uporabljene, vendar ne upoštevajo prioritete. Usmerjevalniki so povezani s stikali za prenos podatkov, ki imajo visoko porabo. Nastavljivi usmerjevalniku rešujejo problem visoke porabe. Dizajn usmerjevalnika je realiziran v Verilog HDL okolju in simuliran z Xilinx ISE Design Suite 14.3 in ModelSim-Altera 5.5b programsko opremo. Rezultati izkazujejo boljše učinkovitost, nižjo porabo in zakasnitev predlaganega usmerjevalnika.

Ključne besede: Router; NoC; On Chip Power; Area; Energy Efficiency; Delay; Priority; Reconfigurable Router

* Corresponding Author's e-mail: david26571@gmail.com

1 Introduction

The key behind the Integrated Circuit technology has been Moore's law for almost five decades. Although this is projected to slow down to doubling every 3 years in the next few years for fixed chip sizes, the exponential trend is still in force. Because of the evolution, the system level focus moves in steps. It leads to a paradigm shift through the technology maturity for a given implementation style. Past examples of such

shifts were moving from room to rack level systems (LSI-1970s) and later from rack to board level systems (VLSI-1980s). This trend allowed the introduction of Systems on-Chip (SoC) (1990s), the integration of many components such as Microprocessors and Custom IPs in a single chip. Hence the integration of many processing elements along with the memory cores in a single chip [1, 2] was introduced. In turn it created a communication overhead that traditional bus-based architec-

tures cannot handle for a number of reasons. In order to solve these problems, NoC (Network on Chip) [3, 4] is a good paradigm. NoC is an integrated network that uses routers to allow the communication among those blocks. It uses networking theory methods for on chip communications where the blocks exchange information on a chip [5].

2 Network on chip

NoC technology is a new approach to communication that [6, 7] enables not only more efficient interconnects but also more efficient design and verification processes for modern SoCs. NoC is an approach in signalling the needs of the signal to various communication protocols by reducing the complexity of the chips interconnects. The communication through the NoC is performed by Processing Elements (PEs) through the network fabric composed of switches or routers [8] through physical channels. A typical NoC based MPSoC is composed of a number of PEs such as CPUs, custom IPs, DSPs and Storage elements (Embedded Memory Blocks).

3 Proposed design

The proposed architecture is a Priority based Reconfigurable Router for NoC. The architecture constitutes of a Reconfigurable Router with four channels and a Priority based Scheduler, a Buffer and an Arbiter Unit. Under this section, we will see the design of a Reconfigurable Router alongside the buffer and arbiter unit.

3.1 Router design

Router architectures have dominated the early NoC researches [9] and the first NoC design proposed the

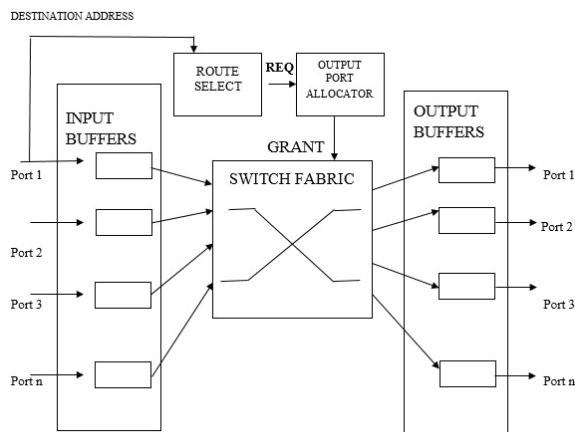


Figure1: NoC Router Block Diagram

use of simplistic routers with deterministic routing algorithms in terms of RTL design. Since, the router [10] is a component that is to be used in every future versions of the system, its architecture options may be either revised or coexist in the same architecture (heterogeneous NoCs [11]), it should be designed as a reusable IP block [12].

The basic block diagram of a NoC Router is shown in figure 1 and its major components are listed below.

- The input/output buffers that temporarily store flits.
- The output port allocation logic which selects the output port for each flit/packet.
- The switch fabric which makes the physical connection from input to output port.
- The control logic that is responsible for overall synchronization.

3.2 Buffer

Buffers are the greatest power consumers [13, 14]. Thus, efficient buffer design is critical for achieving good performance/area/power trade-off. To minimize the implementation cost, the on-chip network has to be implemented with little area overhead. Thus, unlike off chip networks which feature large memories, NoCs typically use small registers for buffering. Major advantage of using registers over large memories is the significant reduction of the address decoding/encoding latency and the access latency [15]. The FIFO scheduler which has to be fit inside the Router is designed. There are 4 FIFOs used in the design of this router. Each FIFO used here is of 9 bits wide and 16 bits depth. The FIFO operates on the system clock and the reset operation is synchronized with an active-low reset. Sizing of buffers in worst case scenario will have to compromise routing area and power consumption while improving the throughput. If depth is small, latency is more leading to a compromise in QoS.

Above figure shows the internal design of a FIFO Buffer module of our proposed design. It has two major units namely Data Path unit and Control unit. Control unit receives control signals as Credit_ in as In_request and Out_request. It has sub modules such as FSM, Counter and Decoder. Minimum buffer dimensions requirements (width and depth) are functions of switching modes, packet size, flit size and expected traffics. One of the vital goals in designing NOCs is to minimize the buffer size by incorporating a trade off between latency and throughput performance degradations.

Upon arrival of the packet at the input port, it is stored in the FIFO Buffer flit by flit during every clock cycle provided that there is availability of free space. Simulta-

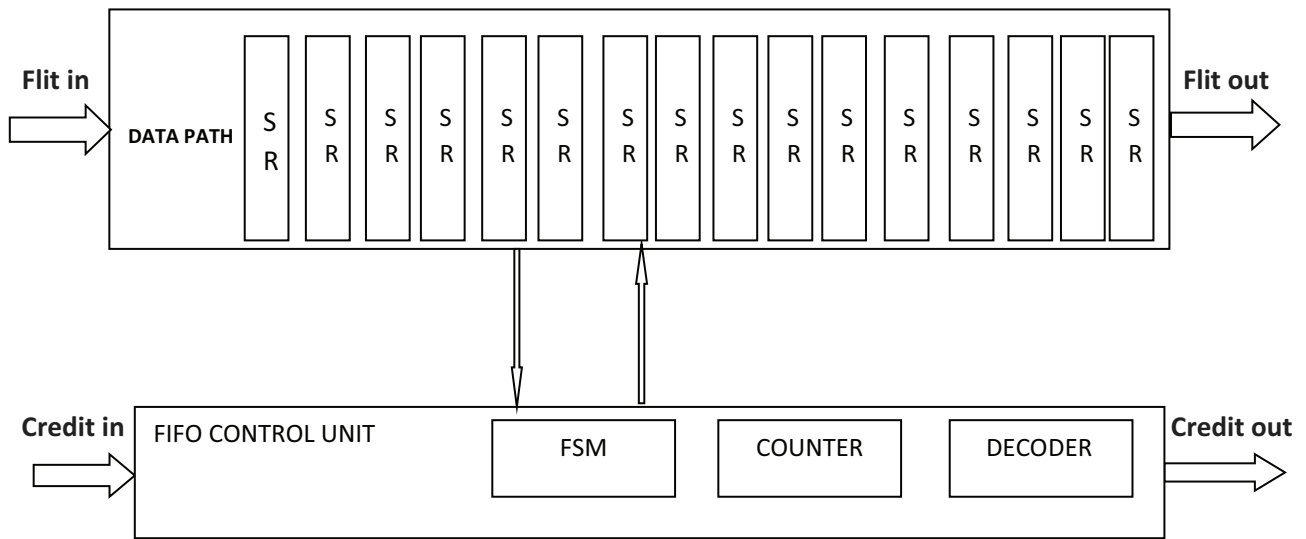


Figure 2: Internal design of an FIFO Buffer module

neously, FIFO Buffer will be evacuated until the output port finds free space. The evacuation stops when the control signal `credit_in` entering the arbiter becomes invalid indicating non availability of free space. However the storage in the current buffer will continue. Now, the control signal `credit_out` representing this port will be sent as back pressure to the adjacent source node when the FIFO Buffer becomes almost full. As soon as the first flit reaches the first location (Shift Register SR) of FIFO which is connected directly to the router, the header flit will notify arbiter about the arrival of the flit/ packet in the port and provide destination address to the Direction Decoder to calculate the direction.

Using the mechanism, eight buffer locations is sufficient enough to get the minimum latency in the absence of blocking. However, the buffer size has to be made parameterizable and chosen as 16 to make a fair understanding and reallocation to four different channels to accommodate the reconfiguration process during contention and to make a fair comparison with other designs. Hence, by doing systematic Design Space Exploration (DSE), the depth of buffers is zeroed in as 16 bits for our design.

Write Operation:

- Signal data is sampled at the rising edge of the clock when `write_enable` is high.
- Write operation takes place only when FIFO is not full to avoid overrun condition.

Read operation:

- The data is read from `data_out` at rising edge of the clock, when `read_enable` is high.
- Read operation takes place only when the FIFO is not empty in order to avoid under run condition.

3.3 Arbiter unit

Finite State Machine (FSM) in general is simply another name for sequential circuits. Finite refers to the fact that the number of states the circuit can take during finite. A synchronous clocked FSM changes state only when a triggering edge occurs on the clock signal. It provides the selection process of selecting the operation to be carried out by the router. The FSM controller here is used to display the work to be done by the router [12]. In general, a synchronous circuit is a digital circuit in which the changes in the state of memory elements are synchronized by a clock signal. In a sequential digital logic circuit, data is stored in simple memory devices termed as the latches.

A synchronizer is a digital circuit that converts an asynchronous signal into the recipient clock domain without causing any stability issues. This module provides synchronization between router Finite State Machine and router FIFO modules. Thus, it provides fruitful communication between all the four input ports and output ports. The register module is designed using four internal registers in order to hold a header byte, FIFO full state byte, internal parity byte and packet parity byte. All the available registers are latched on the rising edge of the clock.

3.4 Reconfigurable router

If an NoC router has a larger FIFO buffer, the network will have higher throughput [16] and smaller latency as there will be fewer flits stagnant on the network. Since, each communication will have its peculiarities, sizing the FIFO for the worst case communication sce-

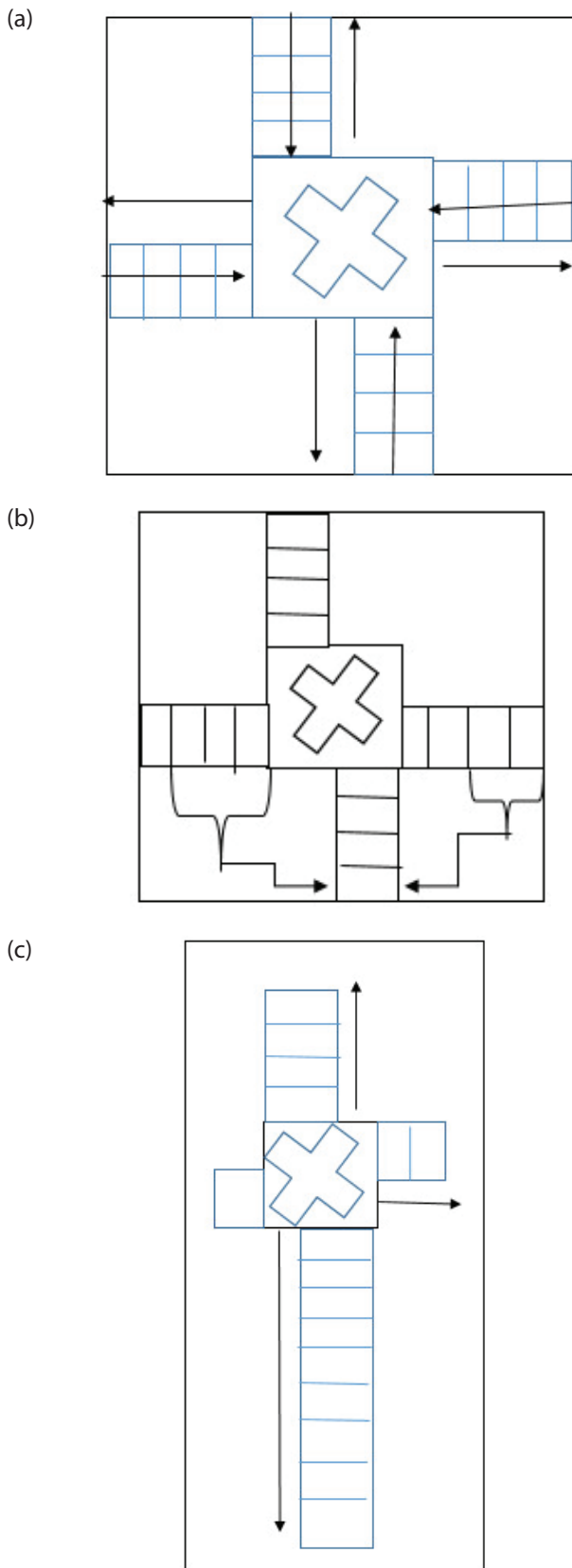


Figure3: a) Router Design with depth 4; b) Need for Reconfiguration; c) Reconfiguration of the Buffer to attend the Need

nario will compromise not only the routing area, but power [17] as well. However, if the router has a small FIFO depth, the latency will be larger and the quality of service (QoS) can be compromised. The solution is to have a heterogeneous router, [18] in which each channel can have a different buffer size. In this situation, if a channel has a communication rate smaller than its neighbour, it may lend some of its buffer slots that are not being used as explained clearly in stages in the figure 3. In figure 3.a all the channels are designed with a depth of 4 slots. The south channel is filled with 9 slots by borrowing three free slots from west and two free slots from east, along with its own four slots as shown in figure 3.b. Thus, the final reconfiguration of south channel with depth 9 is shown in figure 3.c. In a different communication pattern, the roles may be reversed or changed at run time, without a redesign step [19]. When the traffic is less there will be no waiting time and reconfiguration process leading to no impact in latency based on buffer depth. Our proposed idea is to design a router having 4 channels namely East Channel, West Channel, South Channel and North Channel. All four channels have separate buffer slots along with FSM and Registers as 4x4 Baseline Router. It is followed by the modification of the channels inside the router in a way to achieve reconfiguration. Reconfiguration in a router works according to the needed bandwidth in the channel. Initially, the buffer depth of all channels is decided during design. In our design, the buffer depth is fixed for 16. If the east channel is filled with the data it can be transferred to its neighbouring channel when it uses less number of slots. For storing the huge data, the data loss can be avoided by this process known as reconfigurable mechanism.

The design of east channel with the novel reconfiguration mechanism is shown in the figure 4. Priority, [20] a crucial part in networking was not considered in our primary design. Routers are associated with switches to take data transmission decisions resulting in higher power consumption [21]. In order to overcome this problem of higher power consumption, a new prior-

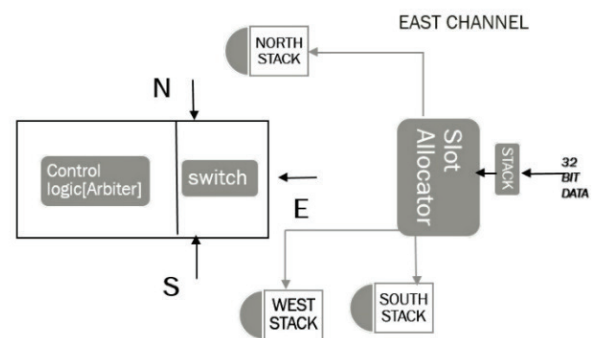


Figure 4: Proposed Design of Reconfigurable East Channel

Device	On-Chip Power (W)	Used	Available	Utilization (%)	Supply Summary	Total	Dynamic	Quiescent			
Family	Spartan-6e	Clocks	0.003	1	---	Source	Voltage	Current (A)	Current (A)		
Part	xc6s100e	Logic	0.000	476	1920	25	Vccint	1.200	0.011	0.003	0.008
Package	cp132	Signals	0.000	878	---	---	Vccaux	2.500	0.008	0.000	0.008
Temp Grade	Commercial	I/Os	0.001	43	83	52	Vccv25	2.500	0.002	0.000	0.002
Process	Typical	Leakage	0.034	---	---	---	Supply Power (W)	Total	Dynamic	Quiescent	
Speed Grade	4	Total	0.037	---	---	---	0.037	0.004	0.034		

2. Summary
2.1. On-Chip Power Summary

On-Chip Power Summary				
On-Chip	Power (mW)	Used	Available	Utilization (%)
Clocks	2.62	1	---	---
Logic	0.14	476	1920	25
Signals	0.39	878	---	---
I/Os	0.56	43	83	52
Static Power	33.70	---	---	---
Total	37.41	---	---	---

Figure 5: Power results of 4x4 Baseline Router

ity based reconfigurable router is designed. Here, the priority is assigned at the slot allocator stage which is incorporated in the router.

During typical router operation, an incoming flit is first successfully received and possibly stored in the input queue. Second, the output port request for the incoming flit is determined based on the flit destination address according to the routing algorithm. Third, the output port allocator receives the flit [22, 23] requests and allocates the output ports according to priority. Finally, as soon as a flit is granted a port it is routed through the switch fabric to the granted output port to reach the neighbouring router or destination node.

Timing constraint: Default path analysis
Total number of paths / destination ports: 3 / 3

Delay: 9.012ns (Levels of Logic = 4)
Source: resetn (PAD)
Destination: vld_out_1 (PAD)

Data Path: resetn to vld_out_1

Cell:in->out	fanout	Gate	Delay	Net	Logical Name (Net Name)
IBUF:I->O	17	1.218	1.226	resetn_IBUF	(resetn_IBUF)
LUT2:I0->O	130	0.704	1.468	fifo[2].f/_or00001	(fifo[2].f/_or0000)
LUT4:I0->O	1	0.704	0.420	s1/vld_out_21	(vld_out_2_OBUF)
OBUF:I->O	3.272			vld_out_2_OBUF	(vld_out_2)
Total		9.012ns	(5.898ns logic, 3.114ns route)		(65.4% logic, 34.6% route)

Figure 6: Timing results of 4x4 Baseline Router

4 Results and discussion

The design of 4x4 Baseline Router is done using Verilog in Xilinx ISE software. The design is simulated using ModelSim. The on chip power consumption is found to be 37.41mW as shown in figure 5. The timing report in figure 6 shows that the synthesis of the design takes a delay of about 9.012ns.

For the efficient utilization of slots in the 4x4 Baseline Router, the need of reconfiguration of the slots in the channel is identified. The Reconfiguration of slots is done according to the bandwidth necessity of the channel. For example, if the south channel is overflowing with the data it can be transferred to its neighbouring channel if it uses the less number of slots. For assigning the four directions four channels are used in reconfiguration router. The register inside the east channel is provided with push and pop as input signal to perform the read and write operation respectively. Moreover,



Figure7: Simulation Waveform showing the functionality of 4x4 Reconfigurable Router

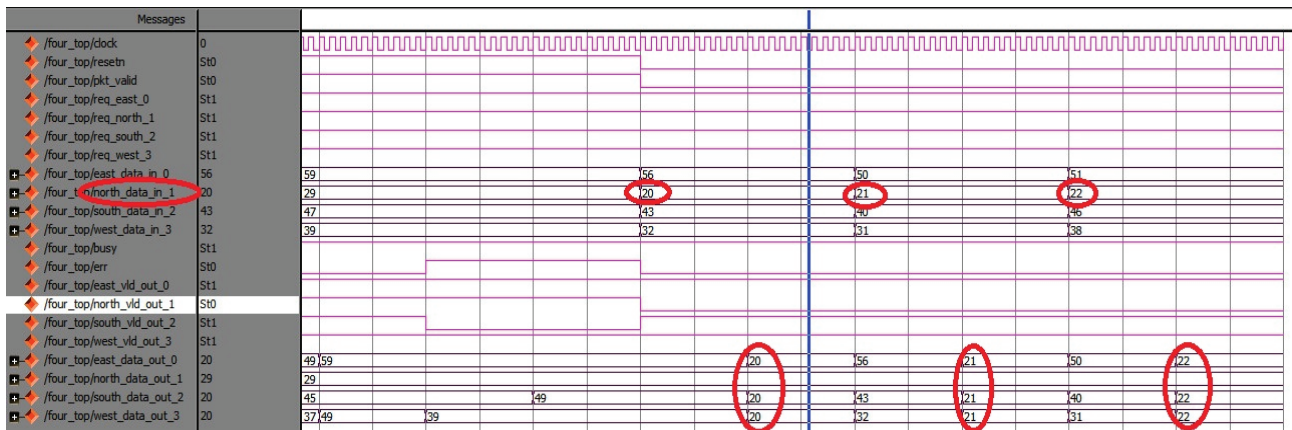


Figure 8: 4x4 Priority based Reconfigurable router

the output of the register is provided with full, empty, half, almost full and almost empty indications to showcase the availability of traffic. From that, the availability of free space of a channel can be inferred. Similarly, the entire data transfer which takes place inside all four channels is analysed separately. Once the push operation is done, the data out will fill the output channel manifesting the full signal indication as high. From the various full and empty indications, the need for reconfiguration is validated.

The function of 4x4 Reconfigurable Router is obtained from the simulation results as in figure 7. It shows that the data input of west 77 & 74, are not able to be stored in corresponding west output port due to scarcity of memory slot in south. We can visualize that these two data 77 & 74 are stored in north's and south's empty slots respectively. Thus, the concept of reconfiguration is achieved in the simulations. Also, the on chip power consumption is found to be 33.66mW, which is 38% reduction than the Baseline router. The timing delay is

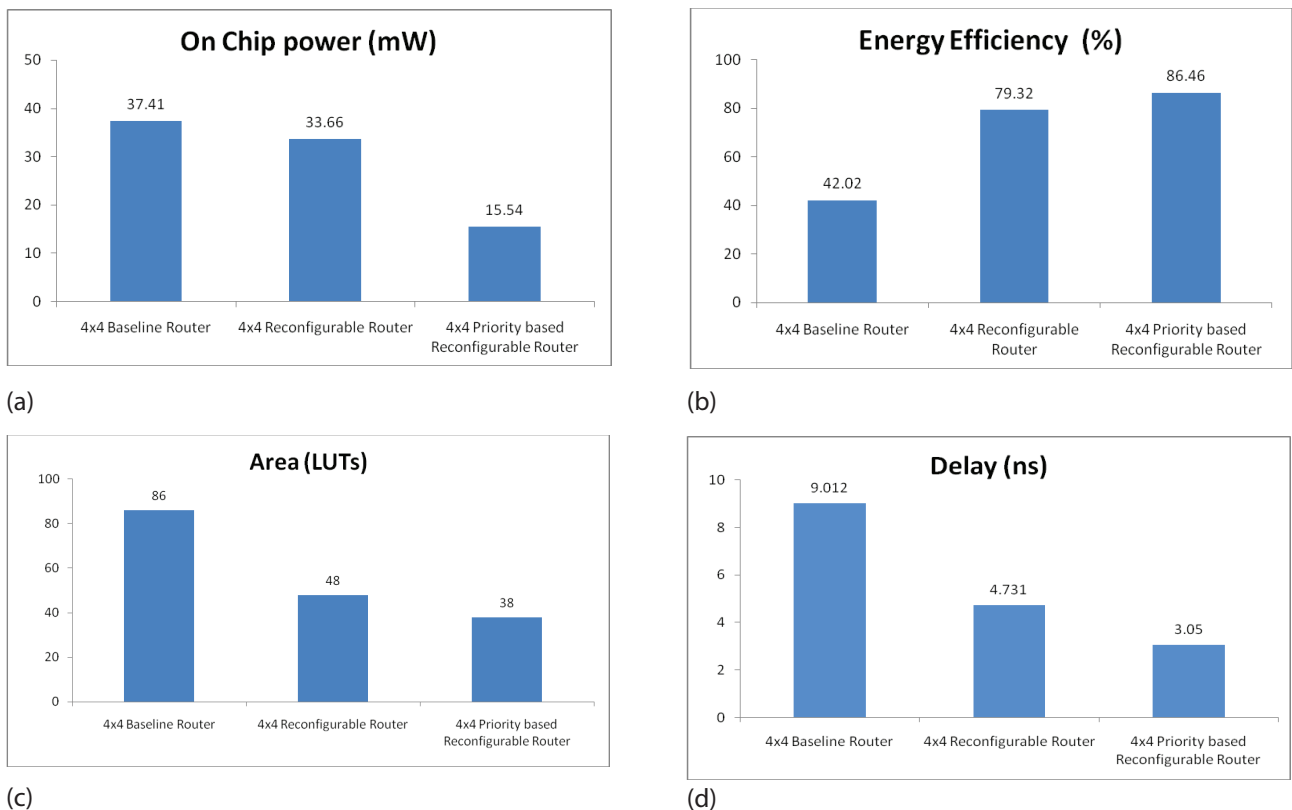


Figure 9: Comparison of performance for various routers with proposed Priority based Reconfigurable router
 a) On Chip Power; b) Energy Efficiency; c) Delay; d) Area in LUTs

also found to be 4.731ns leading to a further reduction of delay too.

The function of 4x4 Priority based Reconfigurable router is obtained from the simulation results as shown in figure 8, the data input of north 20,21 & 22 are not able to store in corresponding north output port due to the scarcity of memory in north channel. So the data 20, 21 & 22 are stored in east's, west's and south's empty slots respectively. The concept of priority based reconfiguration is achieved in the sense of accessing the data inputs of any of the channels from any of the slots. The 4x4 Priority based Reconfigurable Router on chip power consumption is found to be much lesser at 15.54mW, which is 44% reduction in comparison with 4x4 Baseline router, and where as it has a further 36% reduction in delay at 3.050ns.

The figure 9 shows the overall comparison results of the designed Routers. From that, it is found that the designed Priority based Reconfigurable Router consumes less power with a reduction of 58.5% than the 4x4 Baseline router. The number of (Look Up Tables) LUTs in 4x4 Priority based Reconfigurable Router is reduced from 86 to 38, leading to an optimized router architecture of reduced area and power consumption. When implementing the proposed design on spartan3e FPGA, the delay among the configurable logic blocks is reduced from 9.012ns to 3.05ns. Thus, this design leads to a high efficiency router too. The utilization of the available energy is also significantly improved. The maximized energy efficiency is 86.46% as it has improved from 42.02 %.

5 Conclusion

The Baseline Router is designed using the FIFO, FSM, Synchronizers and Registers with single input channel and three output channels. Then, the channels are extended in all four directions as 4x4 Baseline Router. The design entry of this router is done using Verilog. Their corresponding test fixtures are synthesized and implementation design is obtained using Xilinx ISE Design Suite 14.3. Those on chip supply power consumptions are obtained using XPower Analyzer. The functionality verification of the router is obtained in the form of simulation waveform results from ModelSim -Altera 6.5b. By analysis, it is found that reconfiguration of these buffer slots will lead to the reduction in power consumption in router configuration. Also, the efficient utilization of slots in the 4x4 Baseline Router will improve its performance. So, the channels of the 4x4 Baseline router's channels are modified to achieve reconfiguration. The on chip power consumption and delay of the 4x4 Reconfigurable Router is found to be reduced to 33.66mW which is 44% reduction from the Baseline Router.

In 4x4 Reconfigurable Router the slots are utilized but priority, a crucial part in networking was not considered. Routers are associated with switches to take data transmission decisions resulting in higher power consumption. In order to overcome this problem of higher power consumption a new priority based reconfigurable router is designed and found that the power consumption is reduced by 58.5% while delay is reduced to 3.05 ns. The number of LUTs is reduced to 38. The utilization of the available energy is also significantly improved. The maximized energy efficiency is 86.46% as it has improved from 42.02 %. Thus, this design has led to a high efficiency router too. Designing of Multiple priority Traffic class Router [24] can be considered for future works.

6 References

1. A.Hemani, A.Jantsch, S.Kumar, A.Postula, J.Oberg, M.Milberg and D.Lindqvist, (2000), "Network on chip: Architecture for billion transistor era". In Proceeding of the IEEE Nor chip conference. <https://doi.org/10.1109/ISVLSI.2002.1016885>
2. Park, Dongkook, et al.(2007) "Design of a dynamic priority-based fast path architecture for on-chip interconnects." 15th Annual IEEE Symposium on High-Performance Interconnects (HOTI 2007), IEEE Computer Society, 2007, Proceedings, 15 - 20. <https://doi.org/10.1109/HOTI.2007.1>
3. Ogras, U. Y., Marculescu, R., Gyu Lee, H., Choudhary, P., Marculescu, D., Kaufman, M., & Nelson, P. (2007). "Challenges and Promising Results in NoC Prototyping Using FPGAs". IEEE Micro, 27(5), 86–95. <https://doi.org/10.1145/1255456.1255460>.
4. Kiasari, Abbas Eslami, Zhonghai Lu, and Axel Jantsch, (2012), "An analytical latency model for networks-on-chip." IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume No: 21 Issue No: 1, 113-123. <https://doi.org/10.1109/TVLSI.2011.2178620>.
5. Gaurav Verma, Harsh Agarwal, Shreya Singh, Shaheem Nighat Khanam, Prateek kumar Gupta and Vishal Jain,(2016), "Design and implementation of router for NOC on FPGA", International Journal of Future Generation communication and networking Vol.9.No.12(2016),pp.263-272 <https://doi.org/10.14257/ijfgcn.2016.9.12.24>
6. Oveis-Gharan, M., & Khan, G. N. (2018). "Flexible Reconfigurable On-chip Networks for Multi-core SoCs". Proceedings of the 9th International Symposium on Highly-Efficient Accelerators and Reconfigurable Technologies - HEART 2018. <https://doi.org/10.1145/3241793.3241813>
7. Kakoei, Mohammad Reza, Valeria Bertacco, and Luca Benini, (2011), "ReliNoC: Reliable network

- for priority-based on-chip communication." Design, Automation & Test in Europe. IEEE, 2011. <https://doi.org/10.1.1.281.3548>.
8. Kumar, S., Jantsch, A., Soinenen, J.-P., Forsell, M., Millberg, M., Oberg, J., Hemani, A. (n.d.).(2002), "A network on chip architecture and design methodology", Proceedings IEEE Computer Society Annual Symposium on VLSI. New Paradigms for VLSI Systems Design. ISVLSI 2002. <https://doi.org/10-7695-1486-3>
 9. Concatto, C., Matos, D., Carro, L., Kastensmidt, F., Susin, A., & Kreutz, M. (2009), "NoC Optimization Using a Reconfigurable Router", IEEE Computer Society Annual Symposium on VLSI. <https://doi.org/10.1109/ISVLSI.2009.7>
 10. Pau, R., & Manjikian, N. (2008), "High-level specification and logic implementation of single-chip multiprocessor systems based on a configurable router" Canadian Conference on Electrical and Computer Engineering, 2008 <https://doi.org/10.1109/CCECE.2008.4564695>
 11. Ben-Itzhak, Y., Cidon, I., Kolodny, A., Shabun, M., & Shmuel, N. (2015), "Heterogeneous NoC Router Architecture". IEEE Transactions on Parallel and Distributed Systems, 26(9), 2479–2492. <https://doi.org/10.1109/TPDS.2014.2351816>
 12. Chan, Cheng-Hao, Kun-Lin Tsai, Feipei Lai, and Shun-Hung Tsai (2011), "A priority based output arbiter for NoC router." 2011 IEEE International Symposium of Circuits and Systems (ISCAS). IEEE, 1928 – 1931. <https://doi.org/10.1109/ISCAS.2011.5937966>.
 13. Debore Matos, Caroline Concatto, Luigi Carro, Fernanda Kastensmidt and Maccio Kreutz, (2015), "Highly efficient Reconfigurable Routers in Network-on-Chip". IEEE Transaction on Very Large Scale Integration (VLSI) Systems <https://doi.org/10.1109/VLSISOC.2009.6041348>
 14. Kashif, Hany, and Hiren Patel, (2016), "Buffer space allocation for real-time priority-aware networks." 2016 IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS). <https://doi.org/10.1109/RTAS.2016.7461324>.
 15. Deepak S, Divyaprabha, M Z Kurian (2015), "Design and Verification Of Network-On-Chip Router Architecture". International Journal of Advanced Computational Engineering and Networking, ISSN: 2320-2106, Volume-3, Issue9. <https://doi.org/10.2106/ijacen.2320.3.15.9.1>
 16. Amit Bhanwala, Mayank Kumar and Yogendera Kumar (2015), "FPGA based Design of Low Power Reconfigurable Router for Network on Chip (NoC)". International Conference on Computing, Communication and Automation 2015, IEEE 1320. <https://doi.org/10.1109/CCAA.2015.7148581>
 17. Nirmaladevi, K., & Sundararajan, J. (2017). Low power NoC architecture based dynamic reconfigurable system Cluster Computing. https://doi.org/10.1007/s_10586-017-1413-3
 18. Mostafa S. Sayeda, Ahmed Shalabya, Mohamed El-Sayeda, Victor Goulart, (2012), "Flexible router architecture for network-on-chip". Computers and Mathematics with Applications 64 1301–1310 at SciVerse Science Direct <https://doi.org/10.1016/j.camwa.2012.03.074>
 19. Zhang, Z., Greiner, A., & Taktak, S. (2008). "A reconfigurable routing algorithm for a fault-tolerant 2D-Mesh Network-on-Chip". Proceedings of the 45th Annual Conference on Design Automation - DAC '08. <https://doi.org/10.1145/1391469.1391584>
 20. Nguyen, H. K., & Tran, X.-T. (2018), "A novel priority-driven arbiter for the router in reconfigurable Network-on-Chips". International Conference on IC Design & Technology (ICICDT). <https://doi.org/10.1109/ICICDT.2018.8399747>
 21. Meenu Anna George, Aravindhan and Lakshminarayanan (2017), "Design of five port priority based router with port selection logic for noc". ICTACT Journal On Microelectronics, Volume: 02, Issue: 04 <https://doi.org/10.21917/ijme.2017.0051>
 22. Li, X., Duraisamy, K., Baylon, J., Majumder, T., Wei, G., Bogdan, P., Pande, P. (2017), "A Reconfigurable Wireless NoC for Large Scale Microbiome Community Analysis" IEEE Transactions on Computers, 66(10), 1653–1666. <https://doi.org/10.1109/TC.2017.2706278>
 23. Sinduri, M. N., Nagaraja Kumar, (2013), "Design and Implementation of Reconfigurable Router Architecture for Dynamic NoC's". IJESC Volume No: 1 Issue No: 10 ISSN: 2250 - 1371 Paper IJESC116. <https://doi.org/10.1371/ijesc.2250.10.13.1.3>
 24. Mandal, Sumit K., Raid Ayoub, Michael Kishinevsky, Umit Y. Ogras, "Analytical Performance Models for NoCs with Multiple Priority Traffic Classes." ACM Transactions on Embedded Computing Systems, Volume 18, Issue 5s, <https://doi.org/10.1145/3358176>.



Copyright © 2019 by the Authors. This is an open access article distributed under the Creative Commons Attribution (CC BY) License (<https://creativecommons.org/licenses/by/4.0/>), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Arrived: 18. 06. 20119

Accepted: 06. 01. 2020