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Electronically Adjustable Capacitance Multiplier Circuit with a Single Voltage Differencing Gain Amplifier (VDGA)

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Abstract: In this work, we propose a resistorless realization of a simple electronically adjustable capacitance multiplier circuit using a single voltage differencing gain amplifier (VDGA) as an active building block. The circuit utilizes one VDGA and only one capacitor in a simple circuit configuration. The proposed capacitance multiplier circuit can be tuned electronically with the adjustment of the transconductance gains of the VDGA. To emphasis the applicability of the proposed circuit, a second-order RC low-pass filter is constructed as an application example. PSPICE simulations are performed to verify the theory.

Keywords: Voltage Differencing Gain Amplifier (VDGA); capacitance multiplier; electronically adjustable; active circuits

Elektronsko nastavljiv kapacitivni množilnik z enojnim napetostnim diferencialnim ojačevalnikom (VDGA)

Izvleček: V članku je predstavljen enostaven elektronsko nastavljiv kapacitiven množilnik z diferencialnim ojačevalnikom (VDGA) brez uporabe uporov. Vezje vključuje en VDGA in le en kondenzator. Predlagan kapacitivni množilnik je elektronsko nastavljiv s pomočjo spreminjanja transkonduktančnega ojačenja VDGA. Kot primer uporabe je predstavljen nizkopasovni RC filter drugega reda. Teoretični zaključki so preverjeni s PSPICE simulacijami.

Ključne besede: Napetostni diferencialni ojačevalnik (VDGA); kapacitiven množilnik; elektronska nastavljivost; aktivna vezja

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1 Introduction

Integrable high-valued capacitances are necessary and often used in several analog integrated applications, such as sensor interfacing circuits, monolithic phase-locked loops, sample-and-hold data systems, and implantable biomedical systems [1-3]. However in fully integrated circuit design, the fabrication of the large-valued capacitors is an essential problem, due to their large occupation of fractional die areas for standard silicon-based technology [4-5]. A possible solution is the implementation of high capacitance values from smaller ones by the use of a capacitance multiplication technique. This justifies the development, in the last few decades, of various circuit techniques to implement grounded and floating capacitance multiplier circuits with some active elements like second-generation current conveyors (CCIIs) [6-11], current feedback operational amplifiers (CFOAs) [12-13], operational transconductance amplifiers (OTAs) [14-15], current follower transconductance amplifiers (CFTAs) [16], current differencing transconductance amplifiers (CDTAs) [17], current backward transconductance amplifiers (CBTAs) [18], differential voltage current conveyors (DVCCs) [19], DVCC-transconduct-

ance amplifiers (DVCCTAs) [20], and voltage differencing buffered amplifiers (VDBAs) [21].

Circuits from [8-16], [18-19], [21] employ at least two active components. The active element-based capacitance multipliers proposed in [6], [8-10], [12-13], [17-21] are designed with two or more passive elements. These would need relatively high power dissipation and large silicon area on the chip. In the literature [8-9], [14-15], the capacitance multiplier realizations with different active components have been proposed. Moreover, the available active capacitance multipliers in [6-10], [12-13], [19], [21] are not programmable.

This paper proposes a voltage differencing gain amplifier (VDGA)-based capacitance multiplier circuit. The circuit is realized with only one VDGA together with one floating capacitor. No need for strict component-matching conditions is required. The equivalent capacitor value is electronically tunable by changing the ratio of the VDGA transonductances. The effects of the VDGA non-idealities are also discussed and evaluated. To confirm the analytical calculation, the simulation results with TSMC 0.25-µm CMOS technology are reported.

2 Description of the VDGA

The VDGA, whose circuit symbol is represented in Fig.1, is a recently reported active building block introduced in [22]. In ideal operation, the behavior of the VDGA element can be characterized by the matrix equation:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_{mA} & -g_{mA} & 0 & 0 \\ 0 & 0 & g_{mB} & 0 \\ 0 & 0 & \beta & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ v_x \end{bmatrix}, \quad (1)$$

where g_{mA} and g_{mB} denote the transconductance gains and β represents the voltage gain of the VDGA. Internal structure of the VDGA based on MOS transistors is depicted in Fig.2 [22]. The circuit comprises by three floating current sources (FCSs) M_{1A}-M_{9A}, M_{1B}-M_{9B} and M_{1C}-M_{9C}. Each of them realizes independent tunable transconductance gain g_{mk}, ($k = A, B$ and C). The value of g_{mk} can be determined by: [23]

$$g_{mk} \cong \left(\frac{g_{1k} g_{2k}}{g_{1k} + g_{2k}} \right) + \left(\frac{g_{3k} g_{4k}}{g_{3k} + g_{4k}} \right), \quad (2)$$

where

$$g_{ik} = \sqrt{K I_{Bk}}, \text{ for } i = 1,2,3,4. \quad (3)$$

In equation (3), K is the transconductance parameter of the transsitor and I_{Bk} is an external DC bias current. It is worth mentioning that the transconductance g_{mk} is tuned electronically by changing the bias current I_{Bk}. The FCS M_{1A}-M_{4A} allows for having the differential-input voltage to current converter by $i_z = g_{mA}(v_p - v_n)$, while the FCS M_{1B}-M_{4B} performs the transconductance amplifier action between the z and x terminals (i.e. $i_x = g_{mB} v_z$). Furthermore, a pair of FCSs M_{1B}-M_{4B} and M_{1C}-M_{4C} allows us to obtain a current-controlled voltage amplifier behavior ($v_w = \beta v_z$) with the voltage transfer gain equal to $\beta = g_{mB}/g_{mC}$. Of course, the gain β can be adjusted simple by setting the g_{mB} to g_{mC} ratio.

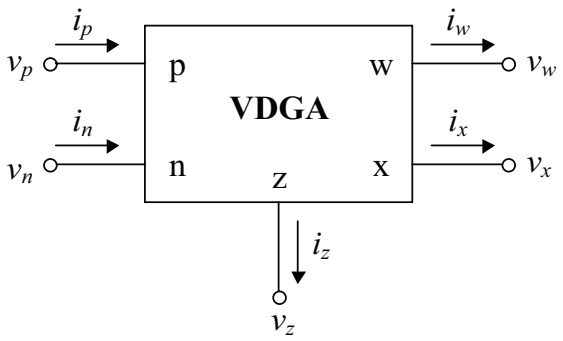

Figure 1: Schematic symbol of the VDGA.

3 Proposed capacitance multiplier circuit

The proposed topology of the capacitance multiplier with a single VDGA is shown in Fig.3. It consists of only one VDGA and one floating capacitor. Although the floating capacitor is required, it can be implemented using metal-oxide-metal (MOM) double poly (poly1-poly2) or metal-insulator-metal (MIM) capacitor process [24]. Considering the VDGA port relation (1), the input impedance of the proposed capacitance multiplier circuit is

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} = \frac{1}{sC_{eq}} = \frac{1}{sC\left(1 + \frac{g_{mA}}{g_{mC}}\right)}, \quad (4)$$

where the simulated equivalent capacitance C_{eq} is equal to:

$$C_{eq} = C\left(1 + \frac{g_{mA}}{g_{mC}}\right). \quad (5)$$

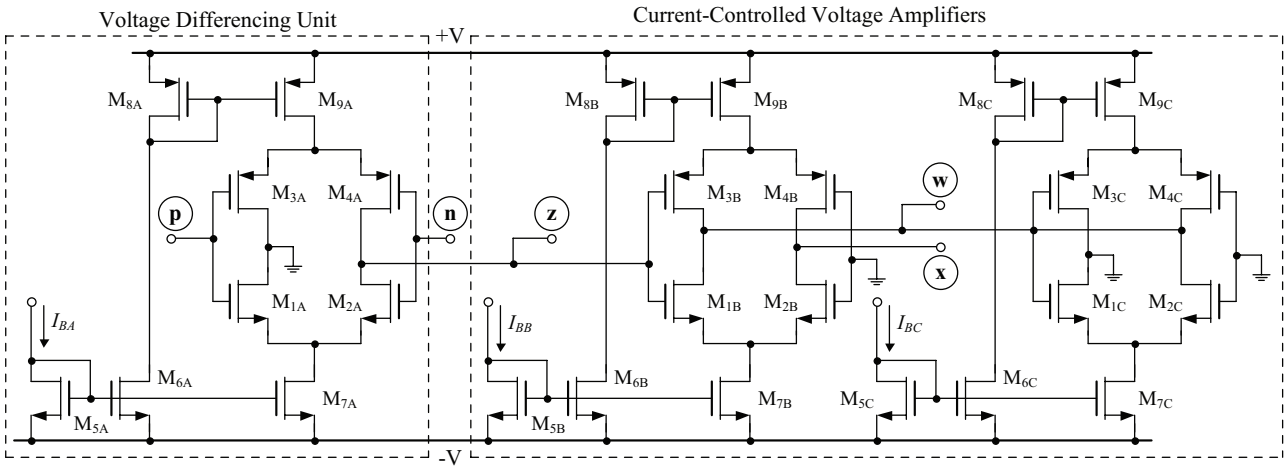

Figure 2: CMOS implementation of the VDGA circuit obtained from the one in [22].

It is clear that the proposed circuit in Fig.3 implements a variable capacitance multiplier with a capacitance multiplication factor given by:

$$K = 1 + \frac{g_{mA}}{g_{mC}}. \tag{6}$$

With this expression, the capacitance multiplication factor *K* is scaled electronically by setting the transconductance ratio g_{mA}/g_{mC}.

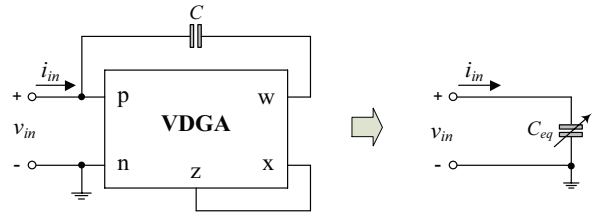

Figure 3: Proposed capacitance multiplier circuit and its equivalent circuit.

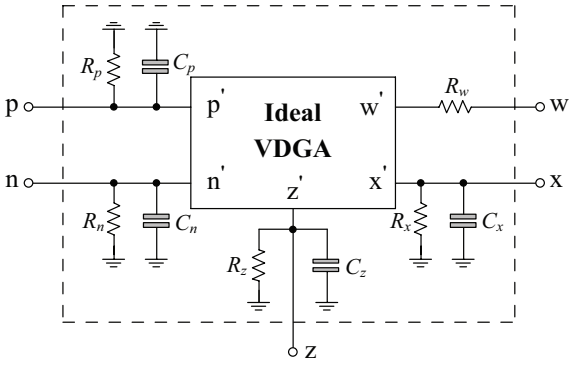

Figure 4: Non-ideal behavior model of the VDGA with terminal parasitics.

4 Analysis of non-ideal behavior

Deviations from the ideal circuit performance are mainly due to the voltage and current transfer inaccuracies and the parasitics of the VDGA. The non-ideal transfer gains of an actual VDGA are expressed as:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha_A g_{mA} & -\alpha_A g_{mA} & 0 & 0 \\ 0 & 0 & \alpha_B g_{mB} & 0 \\ 0 & 0 & \delta\beta & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ v_x \end{bmatrix}, \tag{7}$$

where α_A and α_B are the non-ideal transconductance gains and δ is the non-ideal voltage transfer gain. If these non-ideal transfer gains are considered, then the non-ideal input impedance can be rewritten as:

$$Z_{in}(s) = \frac{1}{sC\left(1 + \dfrac{\delta\alpha_A g_{mA}}{\alpha_B g_{mC}}\right)}. \tag{8}$$

In this case, the equivalent capacitance value changes to:

$$C_{eq} = C\left(1 + \frac{\delta\alpha_A g_{mA}}{\alpha_B g_{mC}}\right). \tag{9}$$

Another non-ideality is introduced by the parasitic impedances at VDGA terminals (Fig.4). Parasitic resistances R_p, R_n, R_z, R_x and the parasitic capacitances C_p, C_n, C_z, C_x are connected between the high-impedance terminals (p, n, z and x) and ground. Series parasitic resistance R_w is associated with the w-terminal. If these parasitic impedances are taken into consideration, the non-ideal

performance of the proposed circuit in Fig.3 can then be evaluated as follows.

If only the p-terminal parasitic impedances are considered, the equivalent capacitance is obtained as:

$$C_{eq} = \left(C + C_p + \frac{1}{R_p} \right) K \quad . \tag{10}$$

Similarly, if only the z- and x-terminal parasitic impedances are taken into account, the equivalent capacitance can be computed as:

$$C_{eq} = C \left\{ 1 + \frac{g_{mA}}{g_{mB}} \left[\frac{1}{1 - \left(\frac{1}{g_{mB} R_{zx}} \right) (1 + sR_{zx} C_{zx})} \right] \right\} \quad , \tag{11}$$

where $R_{zx} = R_z // R_x$ and $C_{zx} = C_z + C_x$.
If only the effect of R_w is considered, the equivalent capacitance is :

$$C_{eq} = CK \left(\frac{1}{1 + sR_w C} \right) \quad . \tag{12}$$

By considering equation (10)-(12), it can be seen that the various parasitics exhibited at different terminals of the VDGA will affect the high-frequency behavior of the proposed circuit. However, from equation (10), the influence of the p-terminal parasitic impedances on the simulated capacitance can be reduced sufficiently under the assumption that $R_p >> 1$, and by choosing the external capacitor such that $C >> C_p$. We also observe from equation (11) and (12) that the presence of parasitic impedances at terminals z, x and w introduces two extra poles, which reduces the useful bandwidth of the proposed circuit. Therefore, the circuit behaves as a capacitor for frequencies:

$$f << \min \left\{ \frac{1}{2\pi R_{zx} C_{zx}}, \frac{1}{2\pi R_w C} \right\} \quad . \tag{13}$$

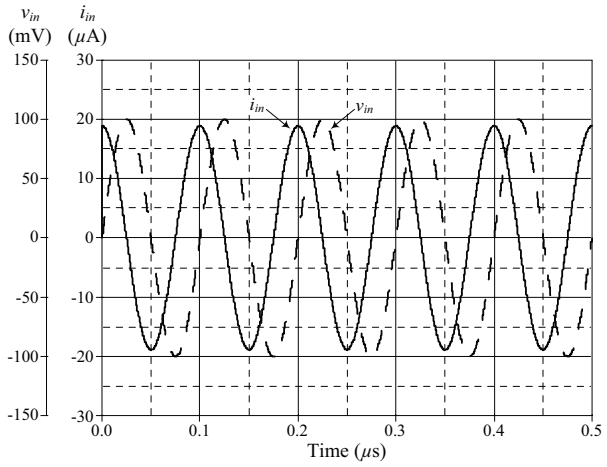

Figure 5: Simulated transient responses for v_{in} and i_{in} of Fig.3.

5 Simulation results and application

The behavior of the proposed circuit in Fig.3 has been simulated with PSPICE using the transistor model parameters of a 0.25-μm TSMC CMOS process. Transistor dimensions are given in Table 1 and symmetrical supply voltages are +V = -V = 1 V.

Table 1: Transistor aspect ratios of CMOS VDGA in Fig.2.

Transistor	W (μm)	L (μm)
M_{1k} - M_{2k}	22	0.25
M_{3k} - M_{4k}	24	0.25
M_{5k}	5	0.25
M_{6k} - M_{7k}	4.5	0.25
M_{8k} - M_{9k}	5.8	0.25

The proposed capacitance multiplier circuit depicted by Fig.3 was simulated with the following component values: $I_{BA} = I_{BB}$ = 100 μA ($g_{mA} = g_{mB}$ = 1 mA/V), I_{BC} = 4 μA (g_{mC} = 0.2 mA/V) and C = 50 pF, which results in C_{eq} = 0.3 nF. The quiescent power consumption of the circuit was 1.09 mW. In Fig.5, the simulated transient waveforms for v_{in} and i_{in} with a frequency of 10 MHz are given, wherein the phase difference has been found to be 89°. Fig.6 also represents the simulated frequency responses for Z_{in}, compared with that of an ideal capacitor response. It is observed from Fig.6 that the simulation results are in very close agreement with the theoretically predicted response far beyond 10 MHz. In addition to illustrate a variation of the C_{eq} value versus

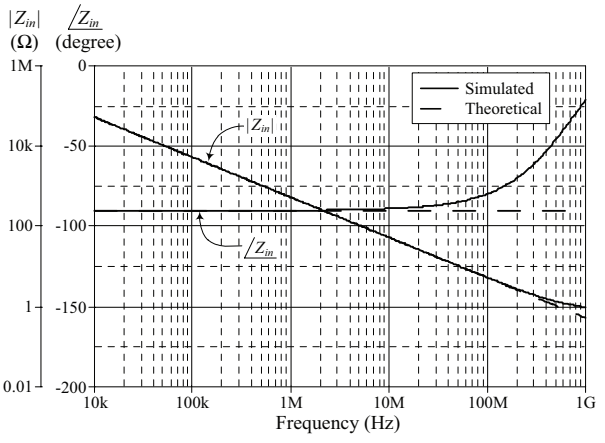

Figure 6: Simulated frequency responses for Z_{in} of Fig.3.

the capacitance multiplication factor, the impedance magnitude responses with different values of g_{mA} are depicted in Fig.7. The results are plotted for the circuit parameters listed in Table 2.

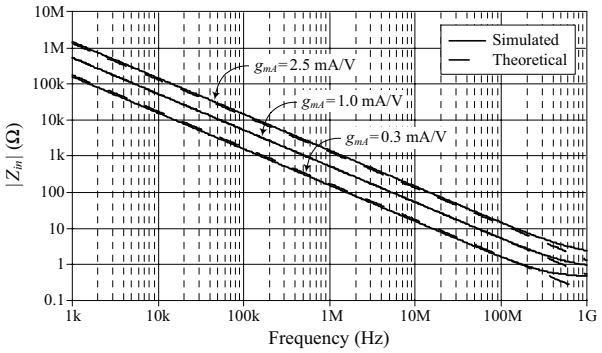

Figure 7: Magnitude-frequency responses of Z_{in} with tuning I_{BA}.

Table 2: Detailed circuit component settings for Fig.7, where C = 50 pF.

g_{mA} (mA/V)	I_{BA} (μA)	g_{mB} (mA/V)	I_{BB} (μA)	g_{mC} (mA/V)	I_{BC} (μA)	C_{eq} (nF)	K
8	0.3	1	100	0.2	4	0.13	2.6
100	1.0	1	100	0.2	4	0.30	6.0
580	2.5	1	100	0.2	4	0.67	13.5

An illustrative application of the proposed capacitance multiplier circuit in Fig.3 is the realization of a second-order RC low-pass filter depicted by Fig.8. The cut-off frequency point is determined by: $f_c = 1/2\pi(R_1R_2C_{eq1}C_{eq2})^{1/2}$. In this realization, the capacitors C_{eq1} and C_{eq2} are realized with the proposed capacitance multiplier circuit in Fig.3. The simulations of the illustrative low-pass filter have been performed by keeping $R_1 = R_2 = 1$ kΩ, and varying the values of $C_{eq} = C_{eq1} = C_{eq2}$. Fig.9 shows the simulated voltage-gain responses for C_{eq} = 0.13 nF, 0.30 nF and 0.67 nF, where detailed C_{eq} settings are the same as those given in Table 2. The results indicate that the value of f_c is: 1.37 MHz, 0.53 MHz and 0.23 MHz, respectively for different sets of C_{eq} values.

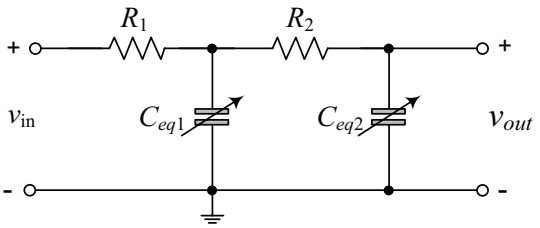

Figure 8: Second-order RC low-pass filter.

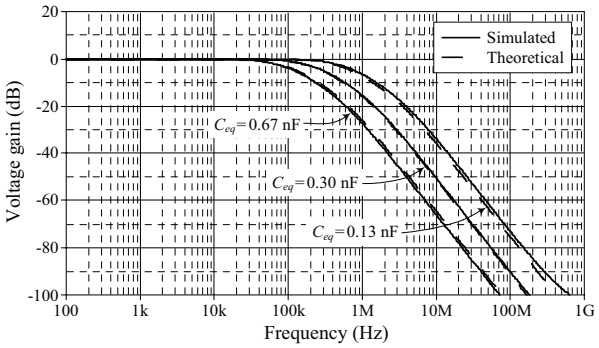

Figure 9: Simulated frequency responses of the filter in Fig.8 with tuning C_{eq}.

6 Conclusions

In this work, a simple realization of an adjustable grounded capacitance multiplier is introduced. The configuration uses only one VDGA as an active element and one floating capacitor as a passive element. The capacitance multiplication factor is electronically tunable by the ratio of the VDGA's transconductance gains. The effects of the VDGA non-idealities including voltage and current transfer errors and parasitic elements on the realized capacitor are investigated. The feasibility of the proposed capacitance multiplier is demonstrated on a second-order RC low-pass filter. Simulation results employing TSMC 0.25-μm CMOS process parameters are provided to verify the theoretical analysis.

7 Acknowledgments

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8 Conflict of interest

The authors confirm that this article content has no conflict of interest.

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