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CMOS series-shunt single-pole double-throw transmit/ receive switch and low noise amplifier design for internet of things based radio frequency identification devices

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Abstract: The incompatibility between current radio frequency identification (RFID) standards has led to the need for universal and wireless fidelity (Wi-Fi) compatible RFID for internet of things (IoT) applications. Such a universal RFID requires a single pole double throw (SPDT) switch and a low noise amplifier (LNA) to direct and amplify the received raw signal by the antenna. The SPDT suffers from low isolation, high insertion loss and low power handling capacity whereas the LNA suffers from smaller gain, bulky die area, lesser quality (Q) factor, limited tuning flexibility etc. because of passive inductor usage in current generation of devices. In this research, complementary metal oxide semiconductor (CMOS) based inductorless SPDT and LNA designs are proposed. The SPDT adopts a series-shunt topology along with parallel resonant circuits and resistive body floating in order to achieve improved insertion loss and isolation performance whereas the LNA design is implemented with the gyrator concept in which the frequency selective tank circuit is formed with an active inductor accompanied by the buffer circuits. The post-layout simulation results, utilizing 90 nm CMOS process of cadence virtuoso, exhibit that our SPDT design accomplishes 0.83 dB insertion loss, a 45.3 dB isolation, and a 11.3 dBm power-handling capacity whereas the LNA achieves a peak gain of 33 dB, bandwidth of 30 MHz and NF of 6.6 dB at 2.45 GHz center frequency. Both the SPDT and LNA have very compact layout which are 0.003 mm^2 and 127.7 μm^2, respectively. Such SPDT and LNA design will boost the widespread adaptation of Wi-Fi-compatible IoT RFID technology.

Keywords: active inductor; Complementary Metal Oxide Semiconductor (CMOS); internet of things (IoT); low noise amplifier (LNA); Radio frequency identification (RFID); single pole double throw (SPDT) switch

Enopolno menjalno oddajno/sprejemno CMOS uporovno stikalo in nizkošumen ojačevalnik za internet stvari identifikacijske elemente na radijski frekvenci

Izvleček: Nekompatibilnost trenutnih RFID standardov je pripeljala do uporabe Wi-Fi kompatibilnega RFID za internet stvari. Takšen univerzalen RFID zahteva uporabo enopolnega menjalnega stikala (SPDT) in nizkošumnega ojačevalnika (LNA) za usmerjanje in ojačenje sprejetega surovega signala. STPD ima nizko izolativnost, visoke vrinjene izgube in nizko zmogljivost prenosa moči, LNA pa majhno ojačenje, velikost , nižji faktor kvalitete in omejeno zmogljivost nastavljanja. V tem delu sta predlagana SPDT in LNA na osnovi CMOS brez uporabe tuljave. Topologija SPDT uporablja seriske upore v povezavi z vzporednim resonančnim vezje, in plavajočim uporovnim jedrom. LNA uporablja žiratorski koncept, pri katerem je frekvenčno nastavljivo vezje izvedeno z aktivno tuljavo in spremljajočim vezjem. Rezultati kažejo, da SPDT izkazuje 0.83 dB vrinjenih izgub, 45.3 dB izolativnost, in 11.3 dBm energijsko kapaciteto, LNA pa izkazuje ojačenje 33 dB, pasovno širino 30 MHz in NF 6.6 dB pri 2.45 GHz. Oba sta izvedena v kompaktnem dizajnu in omogočata povečano uporabo Wi-Fi kompatibilne RFID tehnologije v internetu stvari.

Ključne besede: aktivna tuljava; CMOS; internet stvari; RFID; enopolno menjalno stikalo

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1 Introduction

The widespread usage of smartphones and smart sensors today has transformed the network into a connected web of smart devices and intelligent services which introduces the concept of IoT. RFID is currently a very reliable wireless communication standard that stores and remotely retrieves the information. RFID has a great potential to be used as IoT devices for many useful applications. The technology comprises of mainly transponders and readers. The transponders store information about its identification along with some additional information which is, generally, transferred to the reader on request. In RFID communication, a reader receives data from transponders wirelessly in High Frequency to microwave frequency band which is decided by the nature of the application. Among all concurrent identification technologies, RFID exhibits many advantages. As a consequence, RFID technology is being deployed for many commercial and home applications since few decades and is anticipated to be available for more advanced applications in near future. The continuous downscaling of CMOS technology made it easy for the radio frequency integrated circuits (RFIC) designers to fabricate fully integrated, low-power and compact RFID [1-2].

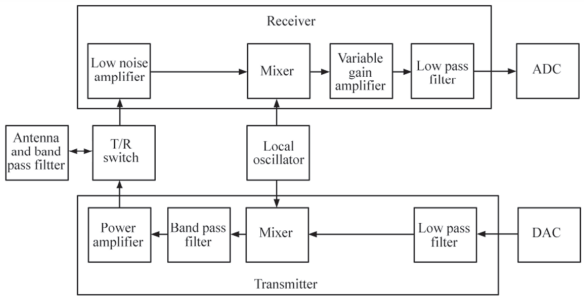

Figure 1: The IoT RFID front end blocks.

In the current generation of RFID communication, the reader is the most exclusive module. Regardless of the versatile opportunities, RFID is yet to overcome the obstruction of reader specific solutions and higher cost for widespread IoT application. In order to abolish the vendor specific unwanted operational cost, a state-of-the-art RFID communication system, by adopting IEEE 802.11b protocol, has been advised in which the wireless network interface cards can be a replacement of the typical RFID reader using future IPV6 concept [2-3]. Therefore, it is expected that a universal RFID communication will be available at very cheap price for widespread IoT application. Fig. 1 illustrates the standard constituents of a transceiver front-end for IoT RFID consisting of a transmitter frontend, a receiver frontend and a common SPDT antenna switch along with a local oscillator for proper information exchange. A power amplifier (PA), band pass and low pass filters, and an up-conversion mixer constitute the transmitter front-end. On the other hand, an LNA, a down conversion mixer, a variable gain amplifier (VGA) and a low pass filter (LPF) build up the receiver frontend. All the modules must be properly matched for the best possible data transmission and reception.

It is obvious that SPDT antenna switch and LNA are the significant modules of every RFID transceiver as it deals with varying low power raw analog signal. An SPDT switch makes it possible for a transceiver to share a common antenna for both transmission and reception process. This design of this switch is quite complicated as it need to handle both high and low power signal. The researchers have tried different combinations of circuit design strategies in order to optimize the CMOS SPDT structure and performance such as: optimized transistor, MOS biasing, stacking transistors, impedance transformation, adjusting substrate impedance [4-10]. However, the trade-off among different performance indicators including isolation, insertion loss, linearity, power handling capacity are application specific and have scope to improve the trade-off for IoT based RFID.

For typical LNA architecture, the frequency selective tank (LC) circuit forms the heart of the LNA. Inductors are always essential components of analogue front-end of typical RF devices for widespread exciting applications [11-16]. Usually, amplifiers and filters, operated in RF regime, utilize on-chip inductors. But inductors in silicon substrates suffer from the parasitic losses which in turn bring down the RF device performance. Additionally, the concerns like die size, lower Q factor, limited tuning flexibility etc. make RFIC designers think alternative to the onchip inductor [17].

In order to conquer the shortcomings, MOS based active inductors are introduced. These active inductors have the privilege of proper tuning in order to compensate the process-voltage-temperature (PVT) variation effects. Moreover, they can offer higher inductance value and better quality factor at only 10% of the die compared to its on-chip equivalent [17]. Consequently, even rapid advancements in integrated circuit technologies cannot keep the passive inductors in the preferred list of RFIC designers.

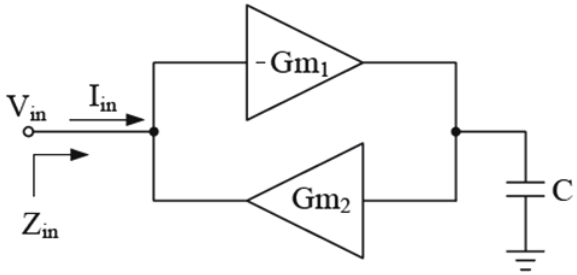

Figure 2: The concept of a typical gyrator.

The concept of the active inductor is a consequence of the gyrator-capacitor model [18-19] as shown in Fig. 2. The gyrator is a two-port circuitry which is composed of a pair of transconductors interconnected in negative feedback in order to reproduce the inductor transfer function. The transconductors designed with NMOSs results in the simple active inductor circuit [19]. Nevertheless, such a composition usually brings some unwanted issues including small inductance, low Q factor, and limited tuning flexibility. In order to compensate these issues, several design ideas have been incorporated as illustrated in the literature [20-27]. Thus, in this proposal, a fully integrated inductorless SPDT and low noise amplifier have been designed and validated by post-layout simulation in 90 nm CMOS technology for 2.4 GHz ISM band IoT based RFID.

2 Design Strategy

2.1 SPDT Design

There are four basic SPDT design topologies which are Series, Series-Shunt, Differential and Asymmetric. Among these, the series-shunt topology is considered the best based on good trade-off between performance and size [5]. Therefore, the proposed series-shunt SPDT, as shown in Fig. 3, consists of transistors (M1, M2) responsible for switching and transistors (M3 and M4) responsible for directing the unwanted leakage signal to the ground. The conduction of these transistors are controlled by the control signals (Vc, Vc´). While the transmitter is active, M1 conducts the signal from the (TX) port to the antenna (ANT) port and M4 drains any leakage approaching the receiver (RX) port to ground in spite of impedance imposed by the combination of non-conducting transistor M2 and active inductor. This improves the isolation of the SPDT with negligibly degraded insertion loss. In addition, the problem of low power handling capacity of the SPDT has been taken care of by utilizing the resistive body floated CMOS structure.

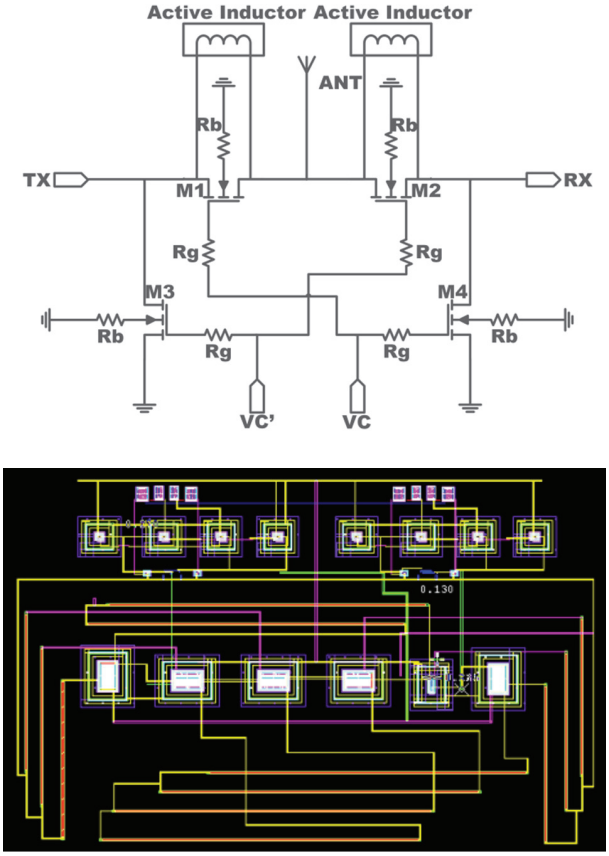

Figure 3: The design concept of SPDT: M1, M2 (100/0.13), M3, M4 (40/0.0.13), Rb, Rg = 10 KΩ. The dimension of the SPDT die is only 0.003 mm^2.

At lower frequency bands, Isolation offered by a typical SPDT is acceptable because of the high impedance of the non-conducting transistors which begins to low down as the signal frequency increases as a result of the leakage through the stray capacitances of the non-conducting transistor. But a selective inductance across this stray capacitance can impose a very high impendence by forming resonant circuit for certain frequency band. This design makes the SPDT offer frequency selective high isolation performance. With the aim of forming such a frequency selective circuit for SPDT, an on-chip inductor was proposed by Feng et al. (2010) [28]. As the lower Q value and larger chip size are the major concerns of on-chip inductors, an optimized active inductor, shown in Fig. 4 [27], has been employed in this SPDT design so that the optimal performance trade-off can be achieved.

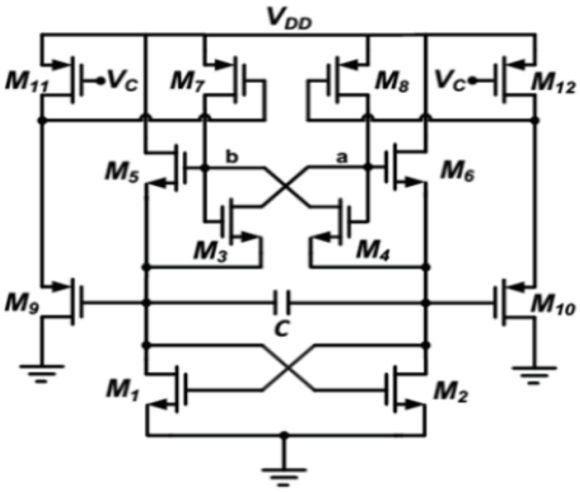

Figure 4: Active inductor for parallel resonant circuit: M1-M6 (0.35/0.13), M7, M8 (20/0.13), M9-M12 (0.35/0.13).

2.2 LNA Design

The proposed schematic of the LNA comprises of three major parts which are: input and output buffer and an active inductor based frequency selective tank circuit. Here, the active inductor utilizes the feature of very low admittance at the resonant-frequency to be used as a frequency selective circuit. Fig. 5 illustrates the schematic of the active inductor circuit used for the proposed LNA. In this active inductor, M_1 and M_2 act as a non-inverting transconductor (g_{M1}) with the input voltage at V_1 and output current at V_3. M_3 is an inverting transconductor ($-g_{M2}$) with the input voltage at V_3 and output current at V_1. Hence, $-g_{M2}$ and g_{M1} form the gyrator which in turn form an inductor at node 1 along with the parasitic capacitor C1 at node 3. This active inductor circuit can be represented as an equivalent RLC circuit as well.

The values of the equivalent inductance, resistance and capacitance are evaluated by:

$$L_{eq} = \frac{C_3}{g_{m1}g_{m2}g_{m3}} \approx \frac{C_3}{0.5g_{m1}g_{m3}} \tag{1}$$

$$r_{loss} = \frac{g_3}{0.5g_{m1}g_{m3}} \tag{2}$$

$$C_p = C_1 \tag{3}$$

$$R_p = \frac{1}{g_1} \tag{4}$$

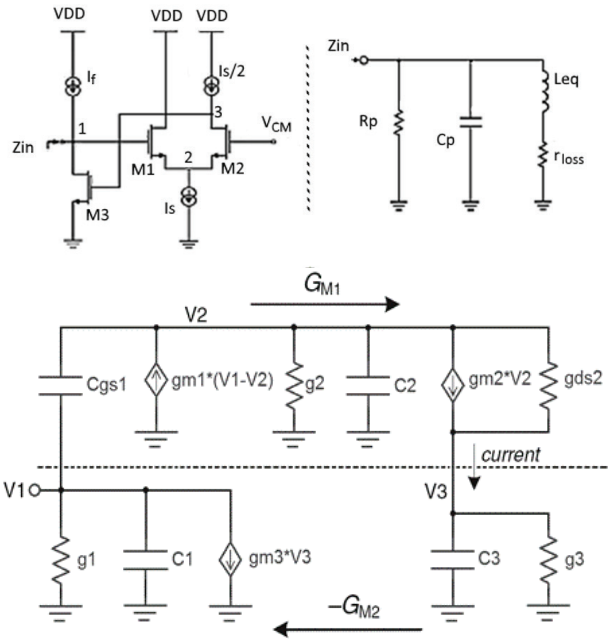

Figure 5: The active inductor and its equivalent circuit proposed for LNA.

The value of the resonant frequency is, therefore:

$$\omega = \sqrt{\frac{0.5g_{m1}g_{m3}}{C_1C_3}} = \frac{1}{\sqrt{L_{eq}C_1}} \tag{5}$$

In the case of passive inductor, the prime noise contribution comes from the internal damping resistance. But in the case of CMOS based emulated active inductor, the main impact is because of the thermal noise modelling in CMOS channel. For the noise analysis of the active inductor, let us consider that it is terminated with a resistance, Rp, the value of which is greater than (1/gm1) and also neglecting the flicker noise of the transistors used, the spot noise figure for Gm cell can be approximately expressed as:

$$NF = 1 + \frac{\gamma}{g_{m2}R_S} + \gamma g_{m1}R_S + \frac{(1+g_{m2}R_S)^2}{g_{m2}{}^2R_SR_P} \tag{6}$$

Where R_S is the source impedance and γ is some constant that depends on the thermal noise behaviour of a given fabrication process. The second term of the NF represents the noise added by M2 and a high ensuring matching conditions can make this term negligible. The third part characterizes the noise hosted by M1 and its transconductance need to be kept small to contribute a lower total

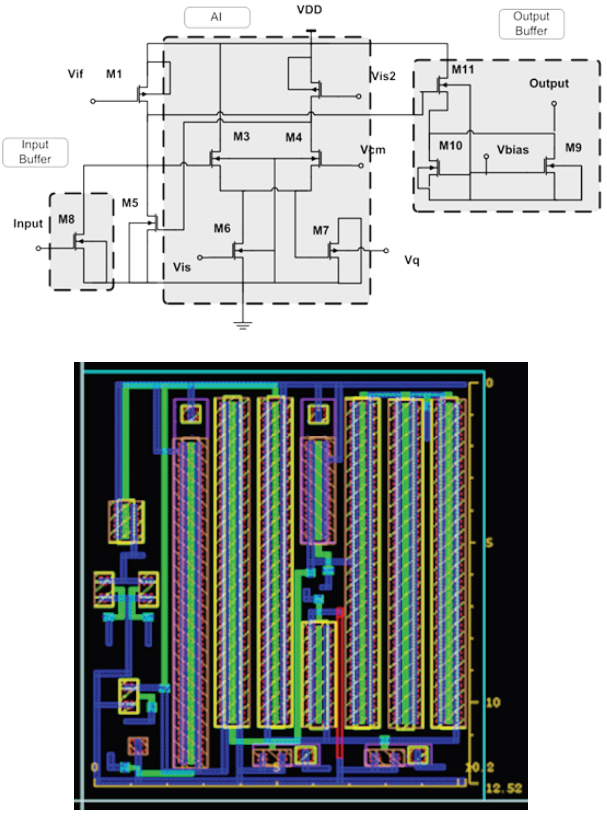

Figure 6: LNA schematic and layout design: M1, M3, M4 (10/0.13), M2 (30/0.13), M5, M6 (3/0.13), M7 - M10 (0.12/0.36), M11 (1/0.36), V_{IF}, $V_{is/2}$, V_{is} = 0.85 V, V_q = 0.7 V, V_{cm} = 0.7 V, VDD = 1.5 V. The die area of the LNA layout is only 127.704 μm².

noise. The fourth term characterizes the noise added by the load. For a high gm2 value, this term becomes nearly identical to R_S/R_P. Hence, increasing the load R_P has the effect of reduced noise contributed by the load.

The architecture of the inductorless nano-CMOS LNA including its biasing and tuning arrangements is shown in Fig. 6. The signal, extracted from the antenna, is fed to the input buffer and is extracted from the output buffer. The active inductor provides all the amplifications and noise minimization at 2.4 GHz band. In this LNA, the voltage biasing V_{IP}, $V_{is/2}$, V_{is}, V_q, V_{cm} contribute to the tuning of centre frequency, noise figure and frequency response. From the small signal equivalent circuit of the LNA, it is obvious that the maximization of the transconductances of M2, M3 and M4 improves the noise performance. But this corresponds to the increase in the parasitic capacitances which lower down the bandwidth and gain. Moreover, the transconductances of M5 and M6 have very small effect on performance as those serve as current followers. So, in order to set the best possible tradeoff, these transconductances have been tuned by trial and error basis.

3 Results and Discussions

The inductorless SPDT and LNA are designed and simulated by 90 nm CMOS process in Analog Design Environment (ADE) of cadence virtuoso. In this study, the performance of the SPDT and LNA is assessed by the post-layout simulation results at standard temperature of 300° K.

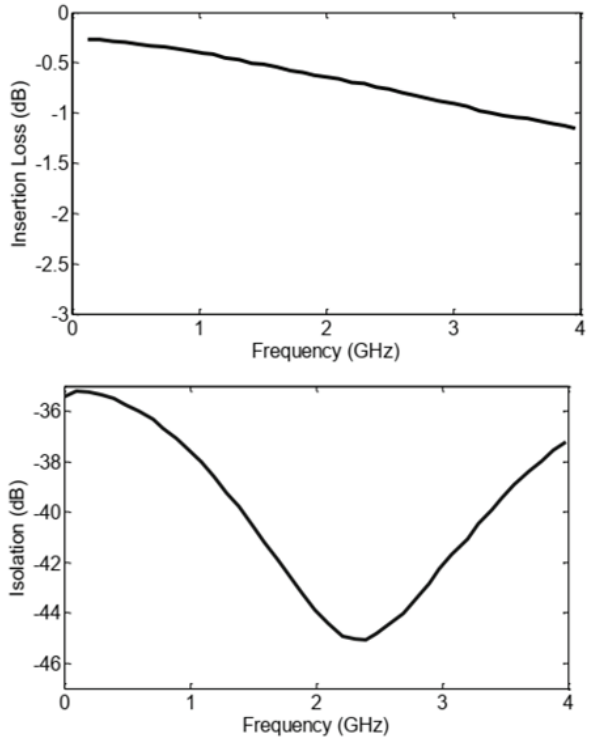

Figure 7: The insertion loss and the isolation of the SPDT.

3.1 SPDT Performance Analysis

Fig. 7 shows the insertion loss and the isolation of the SPDT as a function of the input signal frequency. At higher frequencies, the insertion loss is increased because of the effect of parasitic junction capacitances of the MOSs. The isolation of the switch is a maximum at the 2.4GHz set by the parallel resonant circuit, As the operating frequency shifts in both ways, the leakage causes the degradation of the isolation. The insertion loss and isolation of the SPDT at resonance are 0.83dB and 45.3dB respectively,

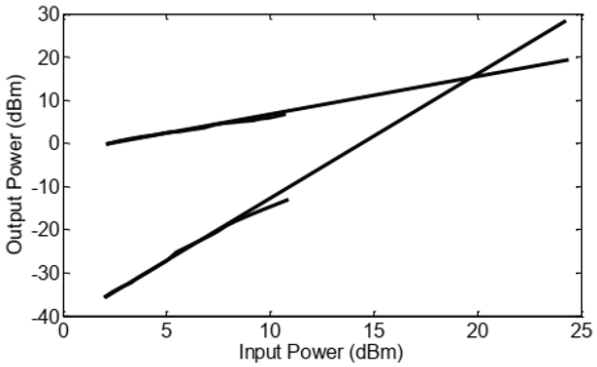

Figure 8: The P1dB and the IP3 of the SPDT.

Fig. 8 shows the power handling capacity and linearity of the SPDT. The P1dB point of this spdt is 11.3 dBm whereas the ip3 point is 19.60 dBm. Above this input power, the MOS body diodes experience break down which allow leakage of the signal to the ground. In the Monte-Carlo analysis for 50 samples, as illustrated in Fig. 9, the insertion loss was found between 0.88 dB and 0.82 dB, while the isolation was between 44.0 dB and 45.5 dB. The performance parameters of the SPDT were less dispersive and steady.

The performance parameters of this SPDT has been listed in Table 1 for comparing to the other recently reported switches. The diode connected transistor pair and suppressing the channel forming signal helped Chen and Lin (2014) to elevate IIP3 and input P1dB of the SPDT to 22.4dBm P1dB and 33 dBm IIP3, respectively [6]. But the isolation and die area were still not satisfactory. Proper impedance matching implementation by Tan et al. (2012) to design a high-power differential switch resulted in lower isolation compared to other designs [7]. Liu et al (2012) with his asymmetrical transistor based design succeeded to achieve lower IL and high P1dB but the core layout area was quite big

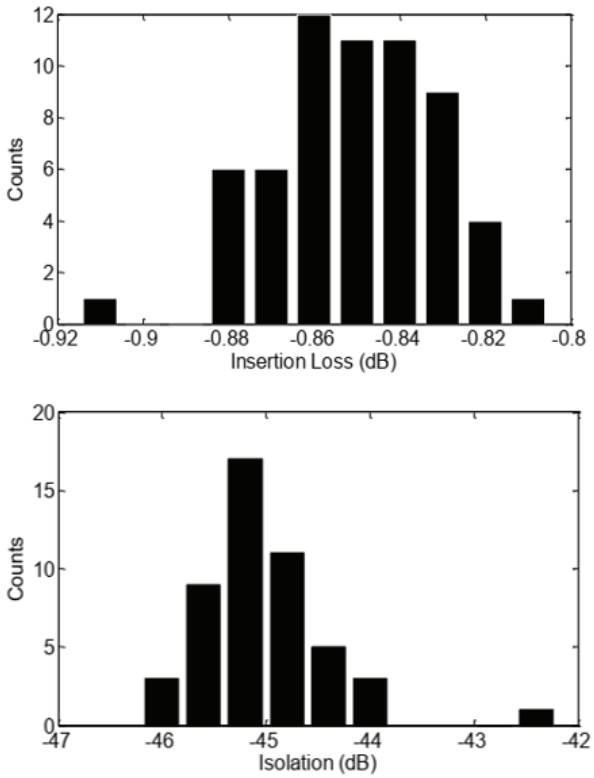

Figure 9: The Monte-Carlo analysis of insertion loss and isolation of the SPDT.

[8]. Body floated transistors with proper impedance matching resulted in 40 dB isolation switch design by Nga et al. (2016) but at the cost of bulky chip and higher IL [9]. The asymmetric SPDT utilizing ac-floating and dc-bias, designed by Chen and Gan (2017), achieved moderate P1dB but other parameters including chip area were quite undesired [10]. However, compared to these design, our SPDT realized the highest isolation and lowest die area due to the implementation of frequency dependent impedance imposed by parallel resonant circuit at 2.4 GHz band. All other parameters are reasonable and meets the 2.4 GHz prerequisites implying that our design demonstrates a good performance tradeoff for 2.4 GHz IoT applications.

Table 1: Summary of the SPDT performance comparison

Reference	CMOS Technology	IL (dB)	ISO (dB)	P1dB (dBm)	Chip Size (mm^2)
[8] (2012)	0.18 µm	0.62	33	29.2	0.125
[7] (2012)	32 nm	1.3	32	34	-
[6] (2014)	0.18 µm	0.72	24.5	22.4	0.037
[9] (2016)	65 nm	0.96	40	-	0.143
[10] (2017)	0.18 µm	1.16	20.8	20.5	0.26
This work	90 nm	0.83	45.3	11.3	0.03

3.2 LNA Performance Analysis

From the AC analysis, as shown in Fig. 10, it is observed that the proposed LNA circuit has a high gain of 33 dB with 30 MHz pass-band at the center resonant frequency of 2.45 GHz. Besides, the noise analysis of the LNA exhibits a noise figure of only 6.6 dB at its center frequency. The peak reverse isolation of the LNA is -33.1 dB at 2.4 GHz as shown in Fig. 11. The total power dissipation for this amplification operation, including the biasing and buffer circuits, equals the only 1.08 mW from a 1.5 V power supply which is very competitive compared to other contemporary researches. Moreover, the power handling capacity and third order linearity have been evaluated as given in Fig. 12 which are also very competitive. For statistical analysis, Monte-Carlo analysis has been conducted and it shows a stable performance of this LNA where the gain varied between 32.8 dB to 33.3 dB and NF varied between 6.4 dB to 6.8 dB for 50 samples as evident from Fig. 13.

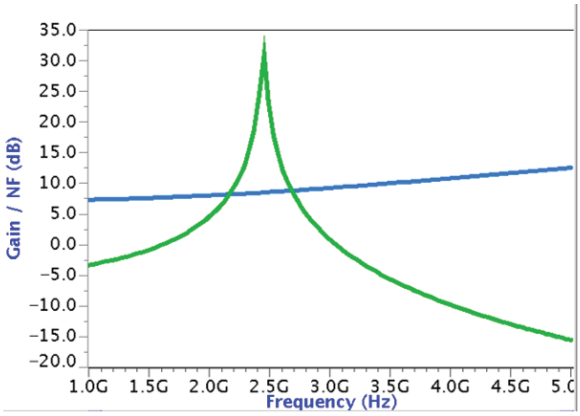

Figure 10: The AC and NF analysis of the LNA.

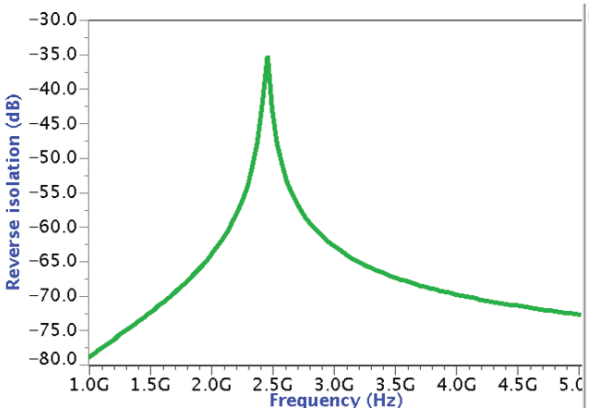

Figure 11: The reverse isolation analysis of the proposed LNA circuit.

Table 2 illustrates the performance comparison of the low noise amplifier with other recent researches. It is clear

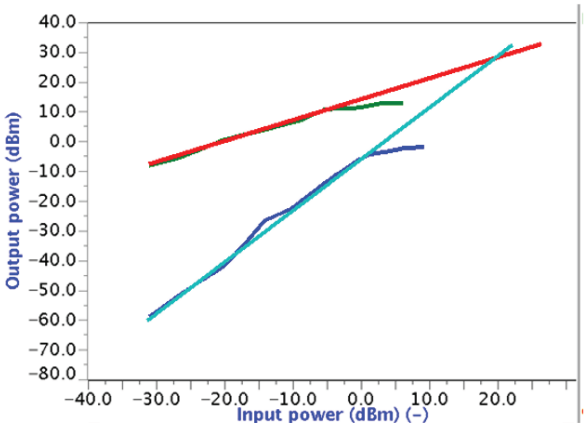

Figure 12: The linearity analysis of the proposed LNA circuit.

from the comparison that the inductorless LNA has the smallest die area which is only 127.704 μm^2. This is mainly due to the adaptation of small size transistors as well as avoidance of bulky passive constituents like capacitors, resistors etc. Moreover, the highest gain of 33 dB will facilitate the receiver frontend to amplify the weak intercepted signal by the antenna because of proper selection of transconductances. However, this work suffers from relatively higher noise figure of 6.6 dB at 2.4 Ghz frequency due to the simple common gate topology used for the amplification and also for using smaller sized transistors. Other parameters, including power dissipation and bandwidth, are also very competitive and support the requirements of 2.4 GHz RFID receiver specifications. Such a fully integrated inductorless LNA will be a handy block for low power compact readerless RFID for IoT applications operated at 2.4 GHz ISM band.

4 Conclusions

The widespread utilization of IoT, nowadays, urges the researchers to fabricate low power and portable de-

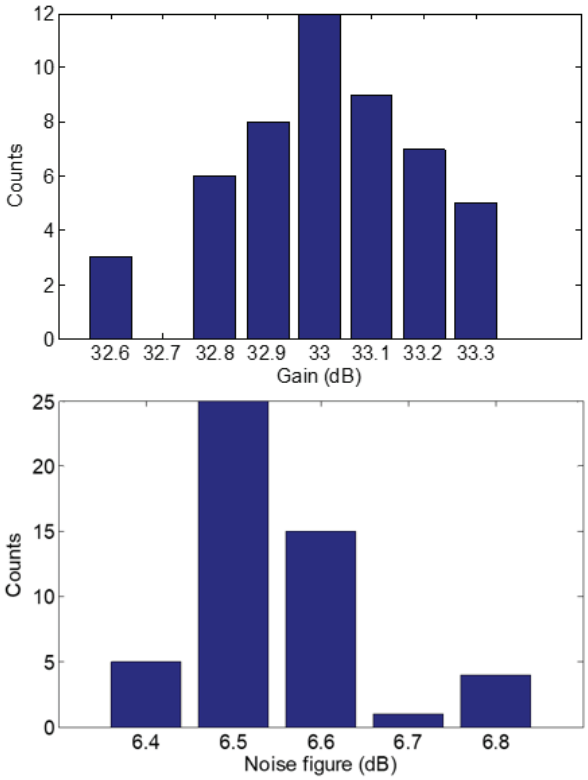

Figure 13: The Monte-Carlo analysis of gain and noise figure of the LNA circuit.

vices. The overall performance of the IoT devices depends on its frontend performance; specially on SPDT and LNA. In this research, the proposed inductorless nano-CMOS SPDT and LNA for 2.4 GHz RFID for IoT application were designed and assessed through the post-layout simulation by using Cadence. The results confirm that the design presented experiences a better performance tradeoff along with smaller power consumption and very compact die area compared to other concurrent researches after meeting all the requirements for 2.4 GHz RF communication. Such high-performance SPDT and LNA will certainly improve the

Table 2: Summary of the LNA performance comparison

Specifications	[22] (2016)	[20] (2017)	[24] (2017)	[21] (2018)	[25] (2019)	This work
Technology	130 nm CMOS	180 nm CMOS	180 nm CMOS	130 nm CMOS	65 nm CMOS	90 nm CMOS
fc (GHz)	2.45	2.5	3-5	2.4	0.5–7	2.45
Gain (dB)	12.3	16.9	12.7	20.7	16.8	33
Power dissipation (mW)	0.4	9.5	8.4	24.9	11.3	1.08
Supply voltage(V)	1.0	1.8	1.8	1.2	1.2	1.5
BW (MHz)	0.1-2.2 GHz	0.1-1.45 GHz	3.43 GHz	550	6.5 GHz	30
NF (dB)	4.9-6	2.5	3.2	2.1	2.87-3.77	6.6
Active Die area (mm^2)	0.0052	0.075	-	0.84	0.044	0.000127

performance of Wi-Fi compatible low power compact RFID as IoT devices.

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6 Conflict of Interest

The authors declare no conflict of interest. Besides, the funding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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