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Modeling of Static Negative Bias Temperature Stressing in p-channel VDMOSFETs using Least Square Method

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Abstract: Negative bias temperature instability (NBTI) is a phenomenon commonly observed in p-channel metal-oxide semiconductor (MOS) devices simultaneously exposed to elevated temperature and negative gate voltage. This paper studies threshold voltage shift under static stress associated with the NBT stress induced buildup of both interface traps and oxide trapped charge in the commercial p-channel power VDMOSFETs IRF9520, with the goal to design an electrical model. Change of threshold voltage follow power law t^n, where parameter n is different depending on the stressing phase and stressing conditions. Two modeling circuits are proposed and modeling circuit elements values are analyzed. Values of modeling circuits elements are calculated using least square method approximation conducted on obtained experimental results. Modeling results of both circuits are compared with the measured results and then further discussed.

Keywords: NBTI; VDMOSFET; electrical circuit; modeling; least square method;

Modeliranje statičnega stresa temperature zaradi negativne napetosti v p-kanalnem VDMOSFETu z metodo najmanjših kvadratov

Izvleček: Temperaturna nestabilnost pri negativni napetosti (NBTI) je fenomen p kanalnih metal-oksid polprevodnikov, ki so hkrati izpostavljeni povišani temperaturi in negativni napetosti. V študiji je opazovana sprememba pragovne napetosti komercialnega VDMOSFET tranzistorja IRF9520 pri NBT stresu in pojav naboja v spojnih in oksidnih pasteh z namenom razvoja električnega modela. Sprememba pragovne napetosti sledi zakonu moči t^n, kjer je n odvisen of faze in oblike stresa. Predlagana sta dva modela, pri čemer so vrednosti elementov izračunani z metodo najmanjših kvadratov na osnovi izmerjenih vrednosti. Modelni rezultati so primerjani z meritvami.

Ključne besede: NBTI; VDMOSFET; električno vezje; modeliranje; metoda najmanjših kvadratov

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1 Introduction

As the device dimensions in CMOS technologies have been continuously scaled down, a phenomenon called Negative Bias Temperature Instability (NBTI) has gained in importance as one of the most important degradation mechanisms. Degradation of transistor parameter values due to NBTI has emerged as a major reliability concern in current and future technology generations, especially in p-channel MOSFETs [1-3]. During the stress period, the transistor parameters slowly deviate from the nominal value. Longer the stress period, higher is the impact of NBTI on transistor parameters. NBTI

effects are manifested as the changes in device threshold voltage (V_T), transconductance (g_m) and drain current (I_D), and have been observed mostly in p-channel MOSFETs operated under negative gate oxide fields in the range 2 - 6 MV/cm at temperatures around 100 °C or higher [1-5]. Change in these parameters is dependent on the stress parameters (time, temperature, gate voltage). Considering the effects of NBTI related degradation on device electrical parameters, NBT stress-induced threshold voltage shift (ΔV_T) seems to be the most critical one [6, 7].

Despite notable scale down in the device dimensions, ultra-thick gate oxide reliability studies are still of significance because of broad use of MOS technology. Taking this into consideration, our earlier papers were dealing with NBTI in p-channel power vertical double diffused MOS (VDMOS) transistors [6, 8-13]. Their reliability has been investigated under various stress conditions, such as irradiation, high electric field, NBTI, NBTI under low magnetic field, and NBTI and irradiation [13-16]. NBTI is critical for normal operation of power MOSFETs since they are routinely operated at high current and voltage levels, which lead to both increased gate oxide fields and self-heating, thus favor NBTI.

First thorough explanation of processes on negative bias temperature instabilities was made by Jeppson and Svensson [17]. Even though more than 40 years have passed since then, many mechanisms of NBTI are not very well understood yet. In the last decade, many different working groups are addressing NBTI effects, with accent on both description and modeling of voltage threshold shifts [19, 20]. Swami presented a model for nano MOSFET for FinFET technologies [20], while Aleksandrov reported a model that is based on a reaction-diffusion principle [21]. Still, an appropriate electrical model to describe instabilities corresponding to different stressing conditions is lacking [22]. A model by Danković is RC based model and describes both static and pulsed NBT stressing [23]. However, further mathematical improvements are needed in order to overcome time-bounded flaws of the model, and to make use of the dependencies between temperatures and bias values. Ma presented a model that attempts to explore these dependencies [24], although they aren't analyzed on the accelerated NBT stressing conditions. Maricau used similar approach of RC based model [25], but it analyses short stressing periods, while this paper focuses on modeling of the effects caused by longer stressing periods.

The use of this type modeling is to create a model that can be mathematically calculated in order to incorporate the model into SPICE. That will enable the designers to consider these instabilities of the circuit during the design phase.

The primary part of this study is to propose an equivalent electrical circuit for modeling of ΔV_T based on experimental data using least square method. In the section 2, experimental setup and results will be briefly described and discussed. Section 3 deals with the modeling approach, and evaluates the model and gives comparison between measured and modeled results.

2 Experimental setup

Used devices for this research are commercial p-channel power VDMOSFETs IRF9520 with initial threshold voltage of V_{T0} = -3.6 V [26]. Devices are built in standard silicon-gate technology with 100 nm thick gate oxide and packed in plastic TO-220 packages.

To properly investigate NBTI in p-channel power VD-MOS transistors in which gate oxides thickness are 100 nm, special stress voltages are needed. These voltages need to be several times larger than typical operating voltage of these transistors (more than – 40 V). To ensure these specific signals, it is needed to develop an additional separate circuit that provides appropriate higher stress voltages for stressing. In years during the research, we have developed a system that automates both NBT stress and measurement on p-channel power VDMOS transistors [12].

System consists of high voltage stress circuit and of low voltage measurement circuit that are controlled with software-controlled switches. Stressing circuit includes an external amplifier between the stress voltage source unit and the device under test (DUT). The transfer I–V characteristics were measured at the drain voltage value of 100 mV, so the device was kept in the linear region of operation. Gate voltage was swept from −2 to −4.75 V, with −50 mV step. Designed system allows full range measurement of transfer I-V characteristics, that is used to extract threshold voltage using second derivative method [27]. This measurement method has previously been used by several research groups [9-13, 15, 16].

Several sets of p-channel devices were tested under different conditions. Devices were subjected to stress for 24 hours during which 36 interim measurements were performed. Two different negative voltages were applied to gate (- 45 V and - 50 V) while source and drain terminals were grounded. Experiments were done at two different temperatures (150 °C and 175 °C) and values of threshold voltage shifts are obtained. Our ear-

lier experiments included testing devices under many different conditions in terms of both gate voltage and temperature [9-13]. Experimental results are given in Figure 1. For the comprehensiveness of the proposed model, only four combinations of stress conditions are shown.

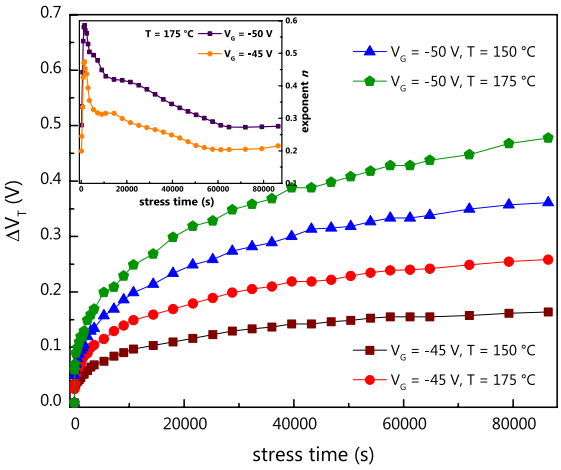


Figure 1: Threshold voltage shifts caused by static NBT stress with value of parameter *n* during stressing.

NBT stress under static conditions results in notable threshold voltages shifts. These changes become more pronounced at higher stress voltages and temperatures, which is in line with other investigations [18, 22, 28, 29]. A lot of results, including ours indicate that ΔV_T saturates with increase in stress time [4, 6, 11].

NBT stress causes threshold voltage shifts with widely different rate in different time periods [28, 29]. Evolution of ΔV_T through time is presented in Figure 1 Inserted graphic, and given with power law (t^n). During this evolution, distinct phases can be distinguished [4, 13, 30]. For every phase, the value of parameter *n* is different. Through each of the phases, parameter *n* is as close as constant (not exactly constant, but in the very limited range). During our earlier researches that involved extensive NBT stress [4, 6, 8, 9-13], in the case of long-term experiments, three different phases are detected in evolution of *n* [6]. Starting phase, where $n = 0.4$. In this phase, *n* is highly dependent on the stressing temperature and bias [4, 6]. Second phase, where *n* drops to $n = 0.25$, and is almost independent on stressing conditions. Third, final phase, where *n* in again dependent on the stressing conditions and steadily declines to $n = 0.14$, continuing to saturation. Similar results are obtained for all stressing temperatures in the experiments. All of the results are suggesting similar development of the parameter *n* [6, 13, 31]. So, it can be concluded that parameter *n* is overall higher at the start phase of the stressing, but tends to saturate in later phases of stressing.

Described progress of the parameter *n* is caused by originated oxide trapped charge and interface traps, which directly influence the changes in the threshold voltage during NBT stress [4]. These occurrences are product of numerous electrochemical processes and reactions concerning oxide and interface defects, holes and other and species related to hydrogen. Depending on the stressing conditions and the number of defects, these reactions can occur in either forward or reverse direction. Since reversed reactions are characteristic for recovery of the degradation that occurs during pulsed stressing, in the case of static stress, forward reactions are dominant [4]. Starting phase of stressing, which explain creation of interface traps is explained with the reaction:

$$Si_3 \equiv Si - H \leftrightarrow Si_3 \equiv Si^{\bullet} + H^{\bullet} \tag{1}$$

The released hydrogen atoms ($H^{\bullet}$) are highly reactive, and they also can dissociate the *SiH* bonds at the interface or in the oxide near the interface. These reactions lead to creation of additional interface traps or positively charged oxide defects.

$$Si_3 \equiv Si - H + H^{\bullet} \leftrightarrow Si_3 \equiv Si^{\bullet} + H_2 \tag{2}$$

$$O_3 \equiv Si - H + H^{\bullet} + h^{+} \leftrightarrow O_3 \equiv Si^{+} + H_2 \tag{3}$$

Released unstable hydrogen atoms react with the holes to form ions.

$$H^{\bullet} + h^{+} \rightarrow H^{+} \tag{4}$$

However, hydrogen ions also dissociate *SiH* bonds in the oxide near the interface leading to creation of positively charged oxide defects.

$$O_3 \equiv Si - H + H^{+} \leftrightarrow O_3 \equiv Si^{+} + H_2 \tag{5}$$

Oxide trapped charge and interface traps buildup described in the given reactions is notably enhanced in the early phase while concentration of *SiH* trap precursors is still high. As the stress time increases, the number of both positively charged defects and interface traps is getting higher. However, probability for reverse reaction (passivation processes) occurring rises as well.

The H_2 molecules released in reactions (2), (3) and (5) diffuse deeper into oxide and can be cracked at positively charged oxide traps:

$$O_3 \equiv Si^{+} + H_2 \rightarrow O_3 \equiv Si - H^{+} + H^{\bullet} \tag{6}$$

As a product of reaction (6), $H^{\bullet}$ is released. It can take part in either forward reaction or reverse reaction, thereby rounding the chain of reaction. Increased amount of reverse reaction occurences lead to change in the slope of a function interpreting parameter *n*. Key step for appropriate modeling is to tackle the change of parameter *n* in phases, in order to follow the evolution of ΔV_T.

3 Modeling approach

Analytical models for NBT stressing have been researched throughout the years [19-25, 32-37]. This model assumes continuous stress on the PMOS devices. Model is built to follow ΔV_T during stress time. Since the change of ΔV_T is given with the power law (t^n), a capacitor *C* charged through resistor *R* is chosen for the central element of the modeling circuit. Capacitor charging equation is given with:

$$V_C = V_S\left(1-e^{-\frac{t}{\tau}}\right) \tag{7}$$

Capacitor is chosen because the capacitor voltage is given in exponential form, which is a type of the power law, needed for ΔV_T modeling. So, the capacitor voltage, V_C models ΔV_T. In given modeling circuit, rise of the capacitor voltage should correspond to the rise of the ΔV_T, so that in any moment t_1, V_C should be as much as accurate as ΔV_T. To accomplish that, specific controlled charging rate of the capacitor must be achieved. Value of time constant, τ, must be calculated first, and then values of capacitance of capacitor *C* and resistance of the resistor *R* must be fitted. Value of V_S is acquired using stretch exponential (SE) equations [3, 6] and listed in Table 1. The SE fit predicts that value of ΔV_T will saturate after extended stressing and it estimates the saturation value. Increased stressing time leads to better estimation of the saturation value, as can be seen for parameter *n*. Stretch exponential equation is given with:

$$\Delta V_T(t) = \Delta V_{Tmax}\,\Delta\left[1-e^{-\left(\frac{t}{\tau_0}\right)^{\beta}}\right] \tag{8}$$

In the equation (8), β, τ_0 and ΔV_{Tmax} are fitting parameters. Parameter β is defined as a distribution width, and τ_o represents a characteristic time constant of the distribution. Parameter ΔV_{Tmax} is a value of ΔV_T saturation [6, 42]. Value of V_S is actually value of ΔV_{Tmax} given in equation 8. Through this value, dependence of the modeling results on bias and temperature values is given. Therefore, for different stressing conditions, value of V_S is different as well. Although at first this looks as a serious limitation, based on our earlier studies, it is possible to estimate the interdependence of time, voltage, temperature and ΔV_T of investigated VDMOSFETs using the results obtained by accelerated NBT stressing [39, 40].

To do modeling based on experimental data, it is needed to find a function that describes experimental data sets, and then to calculate modeling circuit element values based on a fitting function parameter. Most appropriate method for this fitting is Least Square Method (LSM) [41]. LSM is one of the most widely used method to find or estimate the numerical values of the parameters.

Table 1: Values of V_S for different stressing conditions calculated by SE equations.

Stressing Temperature [°C]	Stressing Voltage [V]	Value of V_S [V]
150	- 45	0.182
	-50	0.395
175	- 45	0.312
	-50	0.513

It can also be used to fit a function to a set of data and to characterize the statistical properties of the estimates [42-44]. LSM is a mathematical method for finding the best-fitting curve to a given set of points by minimizing the sum of the squares of the offsets of the points from the curve. Basic principle of the LSM implies that a set of *I* pairs of data points given with (x_1, y_1), (x_2, y_2), … (x_I, y_I) is used to find a function that describes dependence of *y* from independent variables *x*. A curve that is created from the experimentally measured data points can be presented in the generic power form given as:

$$y^* = A \cdot t^B \tag{9}$$

In equation (9), y^* represent modeled function, while *A* and *B* are free fitting parameters. This form of the modeling function is the most suitable one since the parameter t^n that should be relevant with modeled data also has power evolution. Parameters *A* and *B* specify the slope of the modeling function and determine the regression line. LSM defines the estimate of these parameters as the value which minimizes the sum of squares between the measurement (*y*) and the model (y^*) which leads to expression:

$$\varepsilon = \sum_i \left(y_i - y_i^*\right)^2 = \sum_i \left(y_i - \left(A \cdot t^B\right)\right)^2 \tag{10}$$

In the equation (10), ε stands for error which is a value to be minimized. The most suitable way to calculate parameters *A* and *B* is to introduce matrix notation in the following way:

$$\vec{a} = \begin{bmatrix} A \\ B \end{bmatrix} \tag{11}$$

$$X = \begin{bmatrix} 1 & x_1 \\ 1 & x_2 \\ 1 & x_3 \\ \vdots & \vdots \\ 1 & x_i \end{bmatrix} \tag{12}$$

$$G = \begin{bmatrix} \ln f(x_1) \\ \ln f(x_2) \\ \ln f(x_3) \\ \vdots \\ \ln f(x_i) \end{bmatrix} \tag{13}$$

Vector $\vec{a}$ consists of the parameters that need to be calculated. Matrix *X* is created from the time points when the measurements were done, while the matrix *G* consists of logarithm of values being measured in the time points. Calculation of a vector $\vec{a}$ is given with the equation:

$$\vec{a} = \left(X^T X\right)^{-1} X^T \cdot G \tag{14}$$

After performing matrix calculus for different stressing conditions, parameters A and B are calculated and given in the Table 2.

Table 2: Calculated parameters *A* and B for different NBTS conditions.

Stressing Temperature [°C]	Stressing Voltage [V]	Parameter A	Parameter B
150	-45	0.00772	0.27032
	-50	0.01254	0.29692
175	-45	0.00798	0.31088
	-50	0.01453	0.30617

After acquiring fitting parameters, A and B, it is needed to equalize equation (9) with the equation that describes capacitor charging (7). Even though it is mathematically simpler to use exponential form with least square approximation, negative exponent in the capacitor charging formula reverses the convexity of the function. Reversed convexity can introduce a lot of mathematical problems, delivering inadequate poor modeling results. After solving equations, variable τ is calculated. However, even after that calculation is concluded, problem of calculating precise resistance *R* and capacitance *C* that compose τ still remains. For modeling purpose, value of capacitance is set to 1 mF. Basic modeling circuit is given in Figure 2.

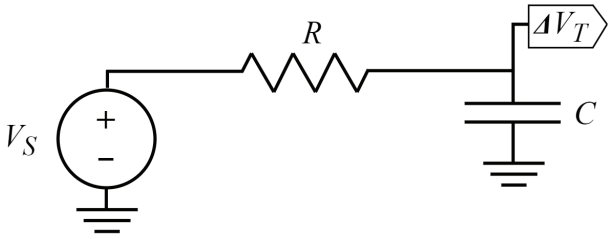


Figure 2: Basic RC circuit for ΔV_T modeling.

Since the variety of the time constants can be found in the progress of the ΔV_T, modeling with only one specific RC connection could lead to considerable dissent in the particular parts of the curve. Parameters *A* and *B* are calculated for the full period of stressing time.

The concept of improved modeling is to present the experimental curve as the product of multiple parts. These parts are to be determined by the phases of parameter *n* evolution, in favor of increasing of the accuracy of the model. To conduct this improvement, additions to the modeling circuit must be made. To follow evolution of ΔV_T, charging rate of the capacitor is to be different in different time intervals. A method for enabling charging rate diversity is to increase the number of RC connections. With the range of different time constants, capacitor voltage can adapt more precisely to ΔV_T. Adding switches and enabling only specific RC connections in determined time periods leads to capacitor voltage being additionally determined. Greater number of RC connections can be achieved in multiple ways, either by increasing number of resistors that are charging one capacitor, either by increasing number of capacitors that are charged through one resistor or either by increasing number of both resistors and capacitors. Since the principle of this modeling is that capacitor voltage models ΔV_T, number of capacitors is set to one. This way, complicate procedure of summing of capacitor voltages that corresponds to ΔV_T in different time periods is avoided, while concept is sustained. With only one capacitor, only way to increase number of RC connections is with increasing number of resistors.

With the goal to link phases of degradation with number of RC connections, modeling circuit is expanded with two additional resistors and switches. Expanded circuit is given in Figure 3.

In the starting moment, both switches, S_1 and S_2 are closed. Capacitor *C* is charged through all of three resistors. Since the resistors are connected in parallel, equivalent resistance is lower than the resistance of the

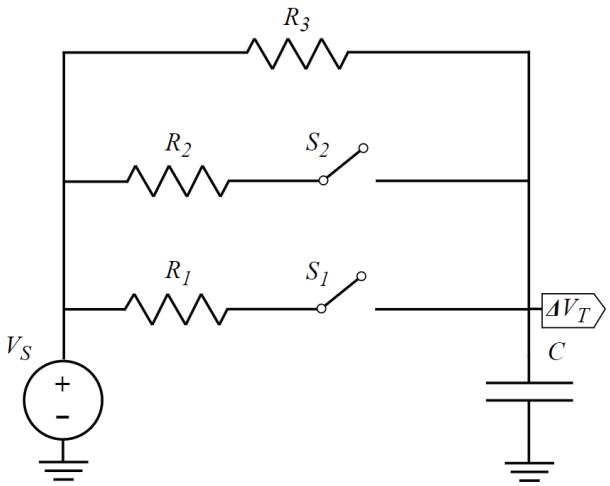


Figure 3: Expanded circuit for modeling of static stress.

resistor with lowest resistance. Growth of ΔV_T is largest in starting phase of stressing, so the capacitor C is charged through lowest resistance, which is in line with model expectations. After starting phase, switch S_1 opens, so that capacitor C continues to charge through parallel resistance of resistors R_2 and R_3 only.

To provide suitable results and follow properly ΔV_T, it is important that $R_3 > R_2 > R_1$. That way, equivalent resistance of resistors R_2 and R_3 is greater than the equivalent resistance of all three resistors. After opening switch S_1, capacitor is charged through higher resistance than before opening the switch, leading to slower capacitor charging and lower slope of the charging curve.

Higher charging resistance leads to even slower charging, which is, once again, in line with the model expectations, and describes development of ΔV_T during stressing. To find appropriate values of resistance LSM is used again. This time, every phase is approximated separately, LSM is applied 12 more times, leading to parameters A_1, A_2, A_3 and B_1, B_2 and B_3. According to these parameters and in consideration with equivalent resistance equations, resistance of resistors R_1, R_2 and R_3 are calculated. Results of different stressing conditions are given in the Table 3. Error of the estimated parameter is calculated using R-squared method and is between 0.95043 and 0.98268 for modeling with basic circuit and between 0.98764 and 0.99262 for modeling with expanded circuit. Modeled results using expanded modeling circuit are given in Figure 4 and 5.

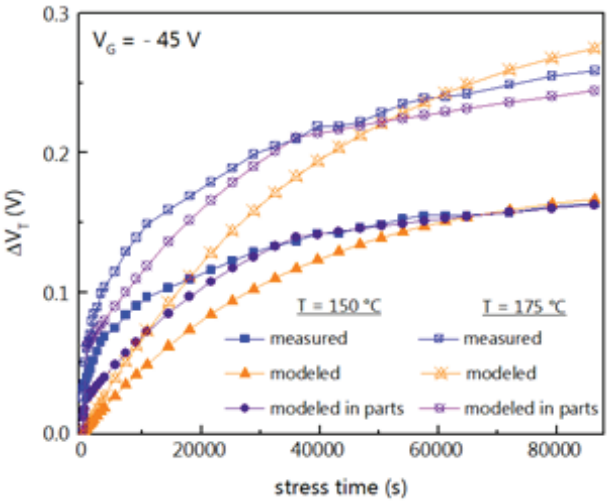


Figure 4: Values of ΔV_T obtained by measuring and with modeling for T = 150 ˚C and for T = 175 ˚C where V_G = -45 V.

Results given in the Figure 4 and Figure 5 show that modeling error is considerably reduced if the modeling is done with taking in mind phase division of the pa-

Table 3: Values od parameters A_1 – A_3, B_1 – B_3 and resistances R_1 – R_3 for different stressing conditions.

Stressing Temperature [°C]	150		175	
Stressing Voltage [V]	-45	-50	-45	-50
Phase 1 (0 < t < 600 s)				
A1	0.02191	0.02191	0.00544	0.00475
B1	0.08548	0.20024	0.38145	0.53067
R1 [MΩ]	10.1215	2.9499	2.9304	3.2873
Phase 2 (600 s < t < 36000 s)				
A2	0.00504	0.00926	0.00793	0.01092
B2	0.31566	0.32872	0.31336	0.33571
R2 [MΩ]	46.7246	71.4286	56.5297	82.6446
Phase 3 (36000 s < t < 86400 s)				
A3	0.01731	0.02279	0.01754	0.01857
B3	0.19832	0.24382	0.23718	0.28539
R3 [MΩ]	87.8942	58.7951	128.9552	53.6646

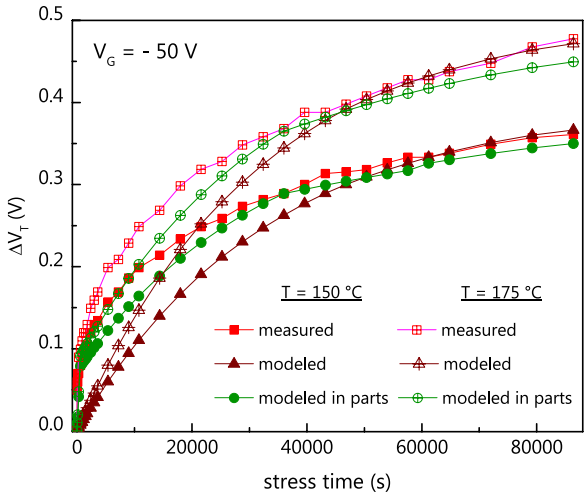
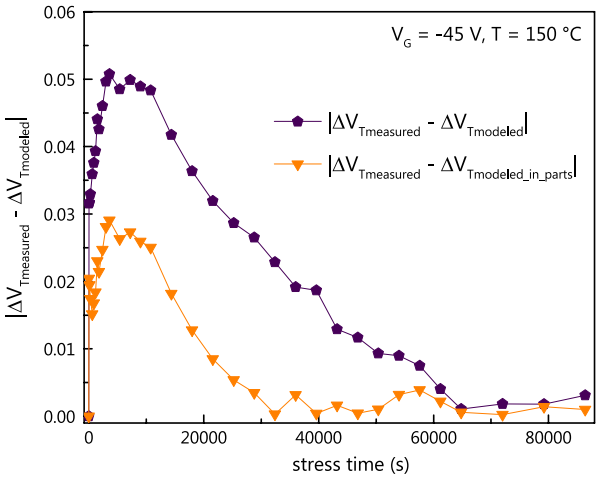


Figure 5: Values of ΔV_T obtained by measuring and with modeling for T = 150 ˚C and for T = 175 ˚C where V_G = -50 V.

rameter *n* evolution. This is notable especially during the second phase of ΔV_T development. Since the third phase occurs after approximately 10 hours of stressing [6, 38], during the experiment, samples are subdued to this phase the longest. When approximating full range of experimental data, LSM adapts parameters better for the longest lasting phase, and thereby, creating a slightly greater mismatch for the rest of the data. With this type of phase division, modeling error is more than twice decreased, as can be seen in Figure 6.

Figure 6: Difference in absolute errors of proposed modeling approaches for T = 150 ˚C and V_G = -45 V.



Results given in Figure 6 show that modeling error has very similar form to the evolution of the parameter *n*, given in the Figure 1 (inserted graphic), which is fundamental signature of NBTI. With additional resistors and switches, used in the expanded modeling circuit, slope of the curve that shows modeling error is decreased (peak of the error is reduced by half, and error is reduced even more in the other parts of the curve). This result is in line with the modeling approach. Further expansion of the circuit (adding more RC connections, and splitting degradation phases into more phases that are shorter, would impact in even more decreased slope).

However, even with further increase in number of resistors, in the specific shorter time interval, time constant will be uniform. To design even more accurate model, number of RC connections is to depend not only on stressing time or phase, but on the actual numbers of individual defects in the circuit itself [29]. With increasing the number of defects, number of RC connections rises, thereby increases the overall sum of the voltages that comprise ΔV_T.

4 Conclusions

Impacts of static negative bias temperature stressing in p-channel power VDMOSFETs IRF9520 have been reported. An equivalent electrical circuit is designed in order to model the behavior of ΔV_T. Mathematical method of least square approximation is described and conducted to determine and to acquire parameters for values of modeling circuit elements. Phase division of parameter *n* evolution during modeling leads to better overall results in terms of accuracy and precision, regardless of stressing conditions. Future steps of work include improving the model with adapting it to the modeling of pulsed stress as well, since p-channel power VDMOSFETs are widely used in switching circuits because of their good switching characteristics.

5 Acknowledgments

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6 Conflict of Interest

The author declares no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results

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