A Low-Voltage Current Mirror for Transconductance Amplifiers

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Abstract: In this study, a low-voltage current mirror to use in differential pairs as an active load is introduced. The proposed current mirror which can operate at ±0.5 V has high output impedance and low input impedance. The proposed structure employs the principle of voltage level-shifting for PMOS transistors. The voltage level-shifting operation has been achieved by using the bulk voltage at this structure. Spice simulations also justify this current mirror's outstanding performance with a bandwidth of 11 GHz using an external capacitor at an input current of 200 μA.

Keywords: PMOS level shifter; low-voltage; current mirror; current-mode; differential pair; bulk voltage

Nizkonapetostno tokovno zrcalo za transkonduktančne ojačevalnike

Izvleček: Članek predstavlja nizkonapetostno zrcalo za uporabo kot aktivno breme v diferencialnih parih. Predlagano zrcalo obratuje pri napetosti ±0.5 V in ima visoko vhodno nizko izhodno impedanco. Struktura uporablja princip premikanja napetostnega nivoja pri PMOS tranzistorjih. Odlična učinkovitost je bila pokazana tudi s SPICE simulacijami pri pasovni širini 11 GHz, z uporabo zunanjega kondenzatorja pri vhodnem toku 200 μA.

Ključne besede: PMOS premikanja nivoja; nizka napetost; tokovno zrcalo; tokovni način; diferencialen par

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1 Introduction

Nowadays, integrated circuit design has concentrated on a circuit with low-voltage operation, low-power dissipation, wide bandwidth and minimum area requirements. A growing need has emerged associated with low-voltage analog circuit design. The demand for circuits operating at low voltage has increased due to the need for low power dissipation. The low-voltage and low-power designs have increased operation time between the battery recharging cycle and have utilized a smaller or lighter-weight battery. Numerous low voltage applications have been proposed earlier [1,2]. Considering several technologies such as bipolar junction transistor (BJT), metal-oxide-semiconductor (MOS) and bipolar complementary MOS (BiCMOS), the CMOS technology has played a crucial role in the development of low power circuit for diverse applications.

The current mirror has been known as a circuit having two terminals whose output current is independent of the output voltage and depends only on the input current. These circuits copying the current carry out a significant function for active elements such as Op-Amp, OTA, current conveyor etc. The low-voltage current mirror has been used in a lot of active elements designed with low-power. The performance parameters of current mirrors like active elements parameters contain linearity, power dissipation, minimum supply voltage requirement, input and output resistance in these applications. At the same time, many active elements include differential pairs designed using PMOS current mirror as an active load [3-6]. The low-voltage operation of the active elements has been restricted because these current mirrors have high input voltage. A low voltage level shifter-based current mirror has been presented in Ref. [7] for current sensor application. Ac-

cording to this study, the bandwidth of the circuit was a few tens of MHz. Though this current mirror can be used in low voltage design, the level shifter approach has been designed using only the NMOS current mirror. The threshold voltage of the PMOS transistor is always higher than that of the NMOS. Thus, the circuit presented in Ref. [7] cannot be obtained using a PMOS transistor. However, this case has been resolved by using the proposed circuit.

In the present study, a low-voltage PMOS current mirror employing voltage level-shifting principle has been introduced. The voltage level-shifting operation has been achieved by using bulk voltage in this structure. The circuit utilizes a voltage level shifter at the input port to achieve the high input voltage swing capability. Thus, it can operate with low power supply voltage and low input /low output voltage requirements. Additionally, the proposed structure as an active load has been used in the transconductance amplifier.

2 Conventional PMOS current mirror

A conventional PMOS current mirror (CM) circuit is shown in Figure 1. Transistor M_1 has been used as a diode and the input current copied to output has been compelled to pump by the input voltage.
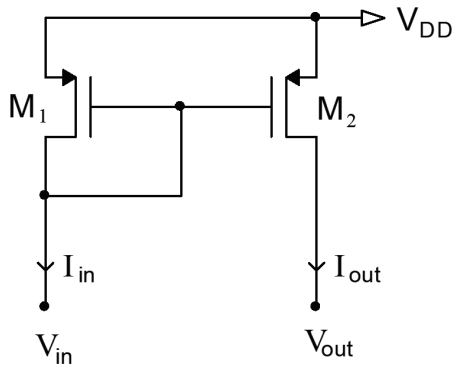

Figure 1: A conventional PMOS current mirror.

Transistor M_1 shown in Figure 1, operates in saturation mode. Besides, the input impedance of the CM depends on the transconductance (g_m) of the M_1. The input voltage of the circuit can be written as below:

$$V_{in} = V_{DD} - \sqrt{\frac{2I_{in}}{k_p \left(\frac{W_1}{L_1} \right)}} - V_{THP} \qquad (1)$$

where $k_p = \mu_p C_{ox}$ is the conduction factor, V_{THP} is the threshold voltage for PMOS transistor, V_{DD} represents the supply voltage. Also, W and L are the effective transistor width and length. The output voltage requirement of the CM can be given as

$$V_{out,max} \approx V_{DD} - V_{DS2,sat} \qquad (2)$$

where $V_{DS,sat}$ is drain-to-source voltage for relevant transistors in the saturation region. One of the drawbacks of the conventional PMOS CM is that input voltage is always greater than the threshold voltage, being a crucial parameter for low-voltage application. The other disadvantage is the low output impedance. Therefore, using this structure is inconvenient in the low voltage. By using the proposed approach, these challenges have been met.

3 PMOS level-shifter current mirror

Figure 2 indicates the PMOS level-shifted current mirror (PMOS LSCM) circuit for low-voltage applications [8]. Transistors M_1 and M_2 are operated in the saturated region ($V_{SD} > V_{SG} - V_{THP}$) in this circuit. Where V_{SD} and V_{SG} are the source-drain voltage and the source-gate voltage for M_1 and M_2, respectively. Additionally, V_{THP} is the threshold voltage for M_1 and M_2. Nevertheless, the most convenient mode is the operation of M_3 in sub-threshold region ($V_{GS3} < V_{THN}$). Where V_{GS3} is the gate-source voltage for M_3 and V_{THN} is the threshold voltage for M_3. Also, M_1 operates in sub-threshold region for low input currents and saturation region for high input currents [9,10].
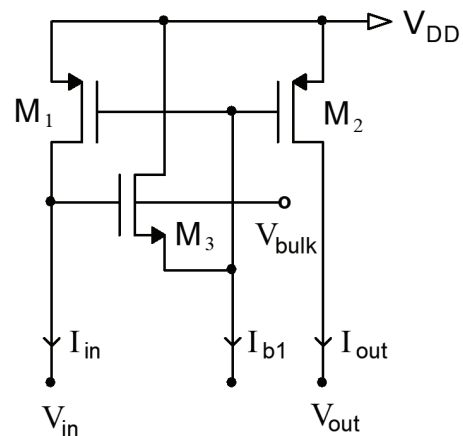

Figure 2: PMOS level-shifter current mirror.

Threshold voltage can be defined by [11]

$$V_{THN} = V_{THO} + \gamma \left(\sqrt{2|\varphi_F| - V_{BS}} - \sqrt{2|\varphi_F|} \right) \qquad (3)$$

where V_{THN} is the threshold voltage for M_3, V_{THO} is the zero-V_{BS} value of the threshold voltage, ϕ_F is the surface
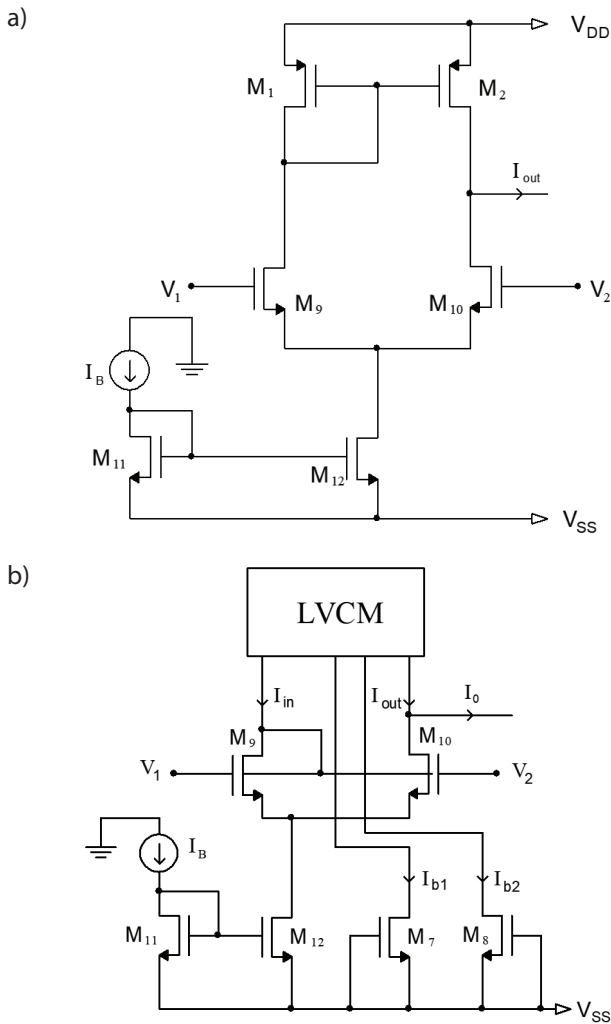
inversion potential of silicon, γ is the body effect parameter and V_{BS} (V_{bulk}-V_S) is the bulk-source voltage. V_{BS} represents the bulk-source voltage for M_3. As shown in Figure 2, transistor M_3 has been used for shifting the voltage level at the drain terminal of M_1. The high value of the biasing current forces M_3 to operate in the saturation region. According to these results, the relation between the voltages can be written as below

$$V_{in} = V_{DD} - \left(V_{SG1} - V_{GS3} \right) \tag{4}$$

where V_{SG1} and V_{GS3} are the gate-to-source voltage of the relevant transistors. The equations describing the operation in saturation and sub-threshold regions, respectively are

$$I_{D1} = \frac{1}{2} k_p \frac{W_1}{L_1} \left(V_{SG1} - V_{THP} \right)^2 \tag{5.a}$$

$$I_{D3} = I_{D03} \frac{W_3}{L_3} \exp\left(\frac{V_{GS3} - V_{THN}}{nU_T} \right) \tag{5.b}$$

where I_{D1} and I_{D3} are the drain currents of transistors M_1 and M_3, respectively. Besides, $k_p = \mu_n C_{ox}$ is the transconductance parameter of the PMOS transistor, U_T is the thermal voltage and I_{D03} is the saturation current. Also, I_{D03} and n are the process- dependent constants. From Equation (5), the V_{SG1} and V_{GS3} can be obtained as

$$V_{SG1} = \sqrt{\frac{2I_{in}}{k_p \left(W_1 / L_1 \right)}} + V_{THP} \tag{6.a}$$

$$V_{GS3} = nU_T \left| \ln\left(\frac{I_{b1}}{I_{D03}} \frac{L_3}{W_3} \right) \right| + V_{THN} \tag{6.b}$$

The input voltage of LSCM can be written as below

$$V_{in} = V_{DD} - \sqrt{\frac{2I_{in}}{k_p \left(\frac{W_1}{L_1} \right)}} + nU_T \left| \ln\left(\frac{I_{b1}}{I_{D03}} \frac{L_3}{W_3} \right) \right| - \left| V_{THP} \right| + V_{THN} \tag{7}$$

by using Equations (5) and (6). For low voltage operation, $V_{THN} > |V_{THP}|$ and $I_{in} > I_{b1}$ is required. This condition related to threshold voltages is arranged when the bulk-source voltage of the M3 is negative value using the bulk voltage (V_{bulk}) as shown in Equation (3).

The output voltage necessity for the proposed PMOS LSCM is given by

$$V_{out,max} \approx V_{DD} - V_{DS2,sat} \tag{8}$$

4 Proposed low-voltage PMOS current mirror structure

The low-voltage PMOS current mirror (LVCM) structure is shown in Figure 3.

Figure 3: Low-voltage PMOS current mirror.

The input voltage for the proposed CM is given by

$$V_{in} = V_{DD} - \left[\left(V_{SG1} + V_{SG4} \right) + \left(V_{GS3} + V_{GS6} \right) \right] \tag{9}$$

From Equation (3), it can be seen that the threshold voltage can be increased by using the bulk-source voltage for M_3 and M_6. Hence, it should be indicated that this condition for the PMOS transistor can achieve level-shifting operation. If Figure 3 is analyzed, it can be seen that $V_{SG1} > V_{GS3}$ and $V_{SG4} > V_{GS6}$ because there is a relationship between voltages as $V_{THN} > V_{THP}$. This condition is arranged when the bulk-source voltage of the M_5 and M_6 is negative value as seen in Equation (3). Also, the input voltage of the CM shown in Figure 3 can be written as

$$V_{in} = V_{DD} - \sqrt{\frac{2I_{in}}{k_p \left(\frac{W_1}{L_1} \right)}} - \sqrt{\frac{2I_{in}}{k_p \left(W_4 / L_4 \right)}}$$

$$+ nU_T \left| \ln\left(\frac{I_{b1} I_{b2}}{I_{D03} I_{D06}} \frac{L_3 L_6}{W_3 W_6} \right) \right| - 2 \left| V_{THP} \right| + 2V_{THN} \tag{10}$$

where $k_p = \mu_n C_{ox}$ is the transconductance parameter of the PMOS transistor, U_T is the thermal voltage and I_{D03}, I_{D06} is the saturation current. Also, I_{D03}, I_{D06} and n are the process- dependent constants. The maximum output voltage requirement for the proposed CM is given by

$$V_{out,max} \approx V_{DD} - (V_{DS2,sat} + V_{DS5,sat}) \qquad (11)$$

Input and output impedances of the proposed circuit can be defined as

$$R_{in} \approx \frac{g_{m1} + g_{m4}}{g_{m1} g_{m4}} \qquad (12.a)$$

$$R_{out} \approx \frac{g_{m5}}{g_{ds2} g_{ds5}} \qquad (12.b)$$

The proposed LVCM is shown in Figure 4. The transistors M_7 and M_8 have been added for biasing.

Figure 4: Enhanced low-voltage PMOS current mirror.

If the M_3 and M_6 are considered identical, the biasing current I_{b1} can be given as

$$I_{b1} = I_{D07} \frac{W_7}{L_7} \exp\left(\frac{-V_{THN}}{n U_T}\right) \qquad (13)$$

I_{D07} is the saturation current. Also, I_{D07} and n are the process-dependent constants. I_{b2} can be defined as similar to I_{b1}. It can be seen that these currents are always low. Thus, the M_3 and M_6 operate in the sub-threshold region. Also, using an external capacitance (C) shown in Figure 4 decreases effective input capacitance.

Figure 5 (a) indicates the conventional transconductance amplifier circuit. Figure 5 (b) indicates the proposed transconductance amplifier circuit for use in low voltage applications.

The drain resistance as a load is used in the transconductance amplifier. Replacing the drain resistance with a current mirror as an active load results in much higher voltage gain [11]. The proposed LVCM as an active load can be used in the transconductance amplifier shown in Figure 5 (b). Transconductance can be expressed as

$$G_m = \frac{I_0}{V_1 - V_2} \cong \sqrt{I_B k_n \frac{W}{L}} \qquad (14)$$

Here, it can be determined as $G_m \approx g_m = g_{m9} = g_{m10}$. Where V_1, V_2 are the input voltages, I_0 is the output current, g_{m9} and g_{m10} are the transconductances of transistors M_9 and M_{10}, respectively. W/L is the aspect ratio of the transistors using for differential pair. The bulk for differential pair is connected to drain in Figure 5 (b). Body bias is used to dynamically adjust the threshold voltage (V_{TH}) of a CMOS transistor. The polarity of the body bias for M_9 and M_{10} is positive values. This situation causes a decrease in the value of V_{TH} for M_9 and M_{10}. The bulk-connected structure is suitable for low voltage applications. Also, the current I_B is the biasing current for the differential pair. A low-voltage transconductance amplifier has been used in many active elements designed with low-power such as Op-Amp, OTA and current conveyor [1-4]. Thus, these active elements have gained operating capability at the low-voltage by using the proposed circuit.

5 Simulation results

The current mirror circuits (Figs. 1, 2, and 4) were simulated for TSMC 0.13 μm technology. The aspect ratios of the transistors are given in Table 1.

Table 1: The aspect ratio of the transistors.

Transistor	M1–M4	M5, M6	M7, M8	M9, M10	M11, M12
W/L (μm)	30/0.26	20/0.26	0.26/0.26	2/1	40/0.26

All the circuit operations have been simulated for the supply voltage ±0.5 V. Currents I_{b1} and I_{b2} are selected

a)

b)

Figure 5: Transconductance amplifiers a) conventional, b) proposed.

as 20 nA. Also, V_{bulk} is equal to -0.5V (V_{SS}). Comparison of current/voltage characteristics of the current mirrors is illustrated in Figure 6. V_{in} is the input voltage for LVCM is shown in Figure 3. The value of V_{in} is taken as 0 V. The I / V characteristic shown in Figure 6 is obtained by changing the supply voltage between 0 mV and 600 mV.

It is clearly shown that the supply voltage of the proposed LVCM requires the lowest value of the supply voltage compared to any other structures. Therefore, the proposed circuit is suitable for low voltage applications. The current transfer characteristic exhibits linear behavior as depicted in Figure 7. However, deviation from linearity occurs for larger value of currents.

The percentage gain error (I_{out} / I_{in}) of the proposed circuit is approximately 0.3 % for I_{in}=200 µA as displayed in Figure 8. Whereas, the percentage gain error (I_{out} / I_{in}) of the PMOS LSCM and conventional CM are 0.6 % and 0.9 % for I_{in}=200 µA, respectively.
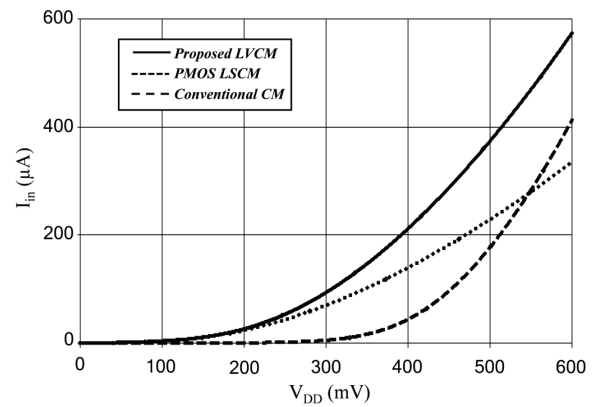
Figure 6: Comparison of I / V characteristics of various CMs.
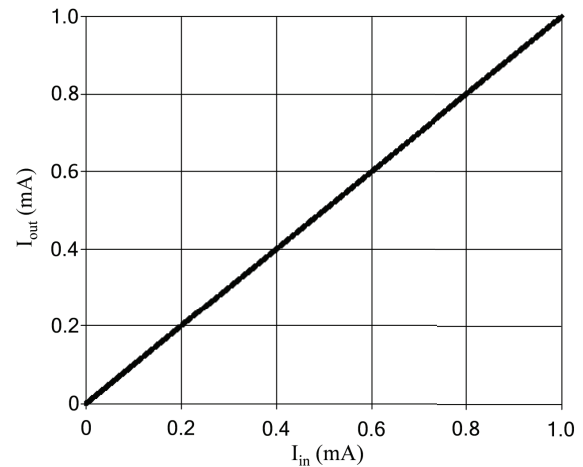
Figure 7: Current transfer characteristics of proposed LVCM.
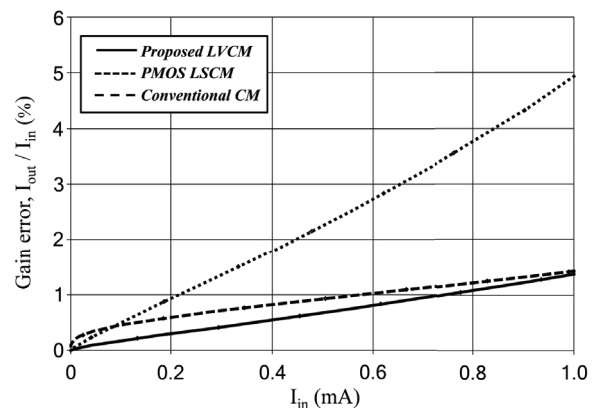
Figure 8: Current tracking errors of various CMs.

The I-V characteristics of the proposed LVCM at different input currents are illustrated in Figure 9. The output current swing of the LVCM is almost independent on V_{DD} for low output current values. The value of V_{out}

is taken as 0 V (V_{out} = 0 V). Considering the output current of the proposed LVCM it can be operated at 0.5 V as shown in Figure 9.
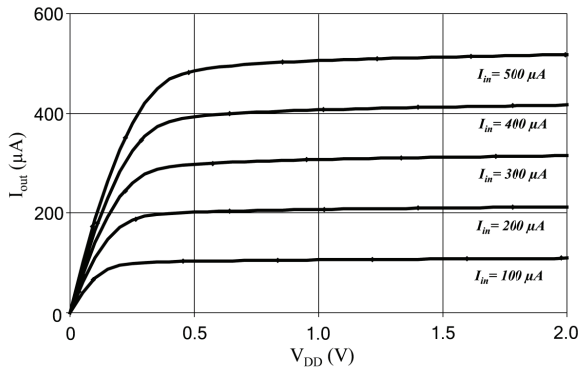
Figure 9: I-V characteristics of the proposed LVCM.

The frequency responses of the current mirrors are indicated in Figure 10.
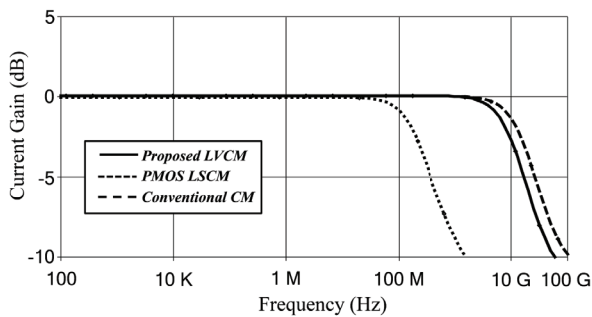
Figure 10: Comparison of the bandwidth of various CMs.

There is an improvement in the bandwidth when a capacitance (C) is used and the bandwidth is found to be 11 GHz. It is shown that the bandwidth reduces to 5 GHz when the C is not used in the design. It is seen that as the capacity value increases, the bandwidth increases. Also, the capacitance (C) has a value of 100 pF. The bandwidth of the PMOS LSCM and conventional CM are 0.24 GHz and 17.2 GHz, respectively.
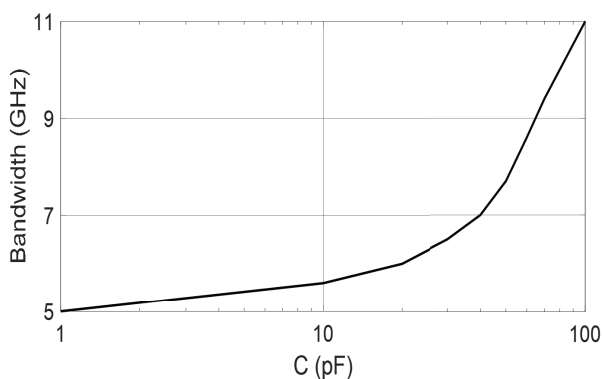
Figure 11: Variation of the bandwidth with external capacitor

The capacitance (C) has a value of 100 pF for 11 GHz shown in Figure 11. As the capacitance value decreases, the bandwidth decreases. The bandwidth can be sacrificed to obtain the lower value of capacitance.
The temperature effect on gain-bandwidth performance of the LVCM is depicted in Figure 12.
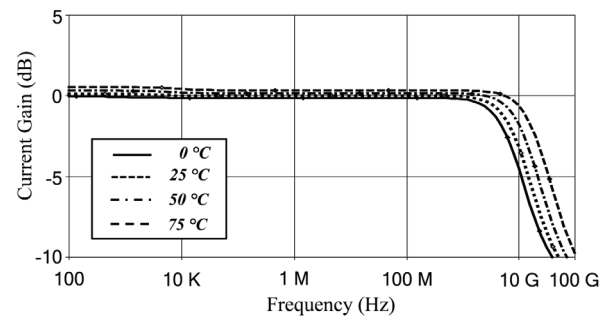
Figure 12: The temperature effect on Gain-Bandwidth performance of the LVCM.

The current gain is about equal to 0.35 dB for 75 °C as shown in Figure 12. Although higher temperature increases the gain of the LVCM the increase is tolerable. The LVCM exhibits temperature-dependent bandwidth characteristics depending on transistors M_3 and M_6 operates in sub-threshold region as shown in Figure 3. The Monte Carlo analysis which is repeated for 30 times is illustrated in Figure 13.
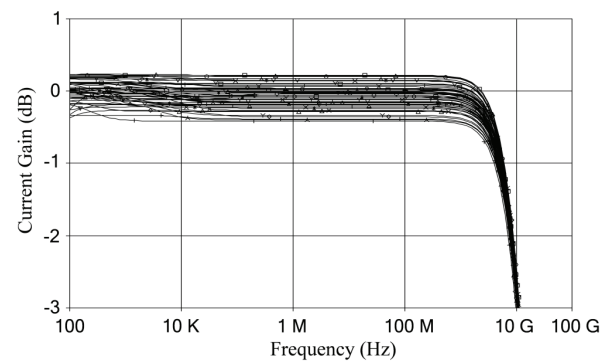
Figure 13: Monte Carlo analysis for Current Gain.

Figure 13 justifies that current gain value has still stable under 20 % random variations in threshold voltages of the transistors. Figure 13 indicates the good performance of the proposed circuit versus mismatches.

Performance comparison of the aforementioned current mirrors is depicted in Table 2.

Table 2: Performance comparison of the CMs.

Parameter	PMOS CM	Level Shifter CM	Proposed LVCM
Power dissipation (µW)	177	67.7	56.6
3 dB BW, I_{out} / I_{in} (GHz)	17.2	0.24	11
V_{in} (mV)	512	470	392
R_{in} (KΩ)	2.56	2.35	1.96
R_{out} (KΩ)	69.5	99.3	130
Gain error, I_{out} / I_{in} (%)	0.9	0.6	0.3
for supply voltage = ±0.5 V and input current I_{in} = 200 µA			

When the performance parameters of the CMs are investigated, it is clearly shown that the proposed structure has a lot of advantages compared with the others. Significantly, the proposed circuit's input resistance is much lower than the others, and it is seen that the suggested LVCM's low input voltage is one of the critical advantages. Also, the gain error belonging to currents (I_{out} / I_{in}) of the proposed circuit is reasonable compared to the other circuits.

The low-voltage transconductance amplifier used the LVCM and the conventional transconductance amplifier is shown in Figure 5. These circuits were simulated for TSMC 0.13 µm technology. The aspect ratios of the transistors are given in Table 1.

The relation between input difference voltage and output current of the transconductance amplifiers is depicted in Figure 14. Also, the supply voltage has been chosen as ±0.5 V for both amplifiers. The value of I_B shown in Figure 5 is chosen as 50 µA.
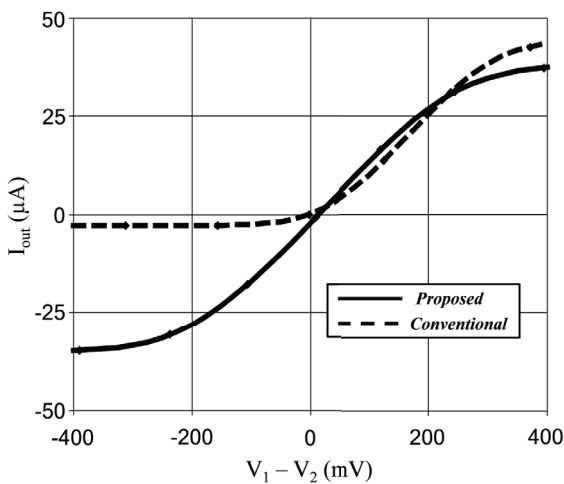
Figure 14: I / V characteristic of the transconductance amplifiers (input difference voltage versus output current)

Conventional transconductance amplifier has not exhibited good performance at low voltage. The circuit

has not strictly operated at ±0.5 V for the negative values of the output current. It is shown that the proposed circuit is more suitable than the other circuit for low voltage applications. However, a conventional transconductance amplifier can only be operated on minimum supply voltage with ±0.65 V, while the proposed circuit can be employed for lower voltage.

Figure 15 indicates the power consumptions of the proposed and conventional transconductance amplifiers for different biasing currents (I_B).
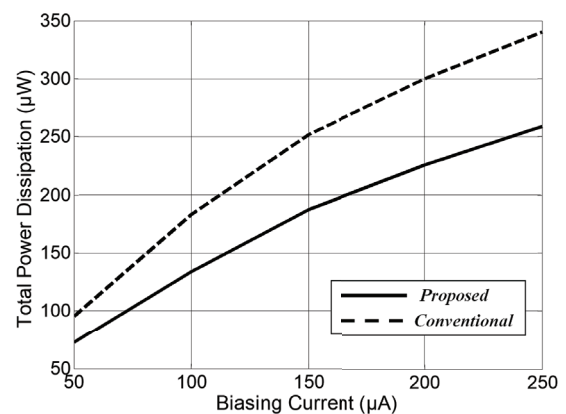

Figure 15: Total power dissipation versus biasing currents for circuits.

As seen in Figure 15, the presented circuit consumes lower power than the conventional circuit for diverse biasing currents. The proposed circuit consumes 70 µW for 50 µA of biasing current. Hence, the suggested circuit is suitable for low-power applications.

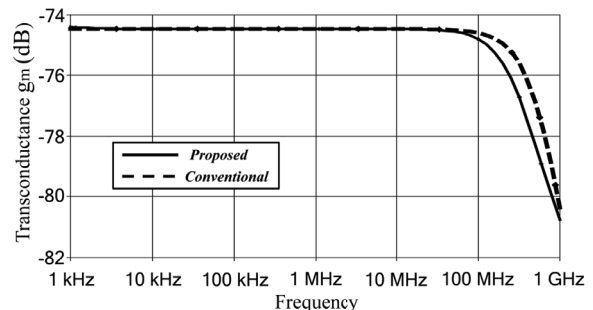The frequency performance of the transconductance amplifiers is illustrated in Figure 16.

Figure 16: The frequency response of the transconductance amplifiers.

Frequency responses of the transconductance (g_m) value for the proposed and conventional circuits are indicated in Figure 16, which gives a bandwidth (-3dB) of 398.8 MHz and 581.1 MHz, respectively.

The total harmonic distortion (THD) is evaluated for input voltage with different amplitudes for a biasing current of 50 μA, as shown in Figure 17.
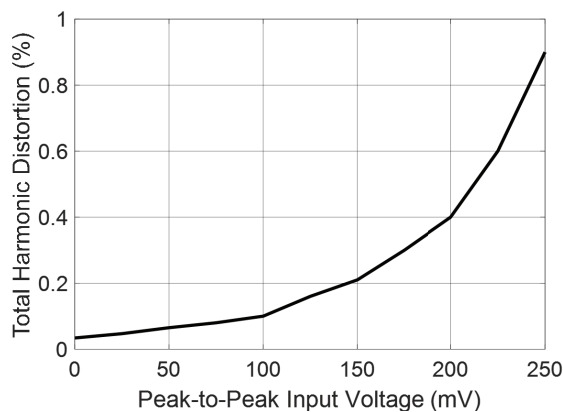

Figure 17: THD (%) versus input voltage (at a frequency of 1 MHz) for the proposed circuit.

The fundamental frequency (1st harmonic) has been specified and THD has been calculated via the PSpice program. The third harmonic provides the most important contribution to the total harmonic distortion of the circuit. The THD has a value of about 0.94% for 250 mV$_{P-P}$. It is shown that THD obtained according to the different peak-to-peak input voltages are reasonable values.

6 Conclusion

A low-voltage current mirror circuit employing the voltage level-shifting principle is demonstrated for use in differential pair as an active load. The proposed current mirror operates at ±0.5 V and its bandwidth is about 11 GHz. Also, it consumes 56.6 μW power. The proposed circuit exhibits better performance than the other CMs called PMOS CM and level shifter CM. It is undeniable that the simulation results confirm the validity of the theory and demonstrate the usage of the LVCM in electronic applications. Also, the proposed transconductance amplifier using LVCM has been compared to the conventional one. The proposed transconductance amplifier's bandwidth is about 581.1 MHz. It consumes 70 μW power. Finally, such a current mirror is appropriate for low-voltage applications, resulting in increasing threshold voltage. Hereafter, the suggested PMOS current mirror would be operated even at lower supply voltages if the threshold voltages could be decreased.

7 Conflict of interest

The authors declare no conflict of interest.

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