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Practical Floating Capacitance Multiplier Implementation with Commercially Available IC LT1228s

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Abstract: A practical realization of a tunable floating capacitance multiplier using commercially available integrated circuits, namely LT1228 is proposed. The synthetic capacitor utilizes only two IC LT1228s along with two passive components (one resistor and one capacitor). The capacitance multiplication factor is electronically controllable through the transconductance gain of the LT1228. The effects of non-ideal transfer gains and parasitic elements of the LT1228 on the circuit performance have been evaluated in detail. The applicability of the proposed floating capacitance multiplier as a second-order band-pass filter is also presented. The claimed theory is verified by several PSPICE simulations and experimental test results.

Keywords: capacitance multiplier; impedance simulation circuit; commercially available integrated circuit; electronically tunable

Praktična uporaba množilnika plavajoče kapacitivnosti s komercialnim IC LT1228s

Izvleček: Predstavljena je praktična uporaba nastavljivega množilnika plavajoče kapacitivnosti z uporabo komercialnega integriranega vezja LT1228. Sintetičen kondenzator uporablja le dva IC LT1228 in dva pasivna elementa (upor in kondenzator). Faktor množenja je elektronsko nastavljiv s transkonduktančnim ojačenjem LT1228. Natančno so opredeljeni prenosi neidealnih ojačenj parazitnih elementov. Uporabnost množilnika je prikazana na pasovnem filtru drugega reda. Teorija je verificirana v PSPICE simulatorju in z eksperimentalnimi testi.

Ključne besede: kapacitetni množilnik; impedančno simulacijsko vezje; komercialno integrirano vezje; elektronska nastavljivost

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1 Introduction

It is well known that the capacitance multiplier is a significant electronic block in the fabrication of high capacitance values in integrated circuit (IC) technology [1]-[2]. This is due to the large-value capacitors requiring a large silicon area on the IC chip. To overcome this limiting problem, the capacitance multiplier circuit which performs the multiplication of small capacitance values can be very useful [3]-[4]. Therefore, the design of capacitance multiplier circuits becomes an essential research issue in the area of analog ICs. Over the years, there are various floating capacitance multiplier circuits reported by several researchers employing numerous versatile active elements [5]-[13]. However, careful observation of the topologies reported in these references reveals that they still suffer from one or more of the following restrictions:

1. They contain three or more active components [5]-[6], [10], [12], which enlarge the area on the chip, and relatively high power dissipation.
2. They need to employ more than two passive components [7], [9]-[10].
3. They are unavailable in commercial IC form [6]-[9], [11]-[12], which cannot be practically implemented using already existing readily available ICs.
4. They lack the electronic adjustability for the capacitance multiplying factor [7], [9]-[10]. The in-

ternal tuning feature would be desirable for modern mixed-signal systems.

5. They use different types of active components for their implementations [5], [12]-[13].

The attention aim of this work is, therefore, to design a floating and tunable capacitance multiplier using already existing commercially available ICs, namely LT1228 [14]. The LT1228 structure internally consists of an operational transconductance amplifier (OTA) and a current feedback operational amplifier (CFOA) in the same IC package. Thus, it may be noted that LT1228 has now become a popular commercial IC for designing several types of analog signal processing circuits and applications [15]-[20]. Two LT1228s and two passive components, i.e. one resistor and one capacitor, are employed in this design. The capacitance scaling factor of the simulated circuit can be altered through the tunable transconductance gains of the LT1228s and/or the resistor in the circuit. A careful non-ideality analysis for the proposed capacitance multiplier circuit is investigated in detail. The second-order RLC band-pass filter implemented with the proposed tunable active capacitance simulator is given as an application. To verify the workability of the proposed circuit, it has been simulated in the PSPICE program using macro-model of IC LT1228, and also experimentally tested in a laboratory using commercially available IC namely LT1228s.

2 Circuit description

2.1 Commercially available IC LT1228

The LT1228 is a commercially available IC manufactured by Linear Technology Corporation [14]. The LT1228 internal circuit, which has the properties of both the operational transconductance amplifier (OTA) and the current feedback operational amplifier (CFOA), is shown in Fig.1(a). The OTA provides an electronic gain control with a differential voltage-to-current converter, whose transconductance gain (g_m) depends on an external bias current, while the CFOA is implemented to drive load low-impedance loads with excellent linearity at high frequencies. The circuit representation block of the LT1228 and its equivalent circuit are given in Fig.1(b) and 1(c), respectively. In ideal operation, the function of the LT1228 can be described by the following matrix relation:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_x \\ v_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & R_{OL} & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_x \\ i_o \end{bmatrix} \quad (1)$$

In equation (1), R_{OL} is the transresistance gain of the LT1228, which is ideally considered to be infinite. The g_m-parameter of this IC can be adaptable electronically with the help of the external bias current I_B and the expression is given by:

$$g_m = 10 I_B \quad (2)$$

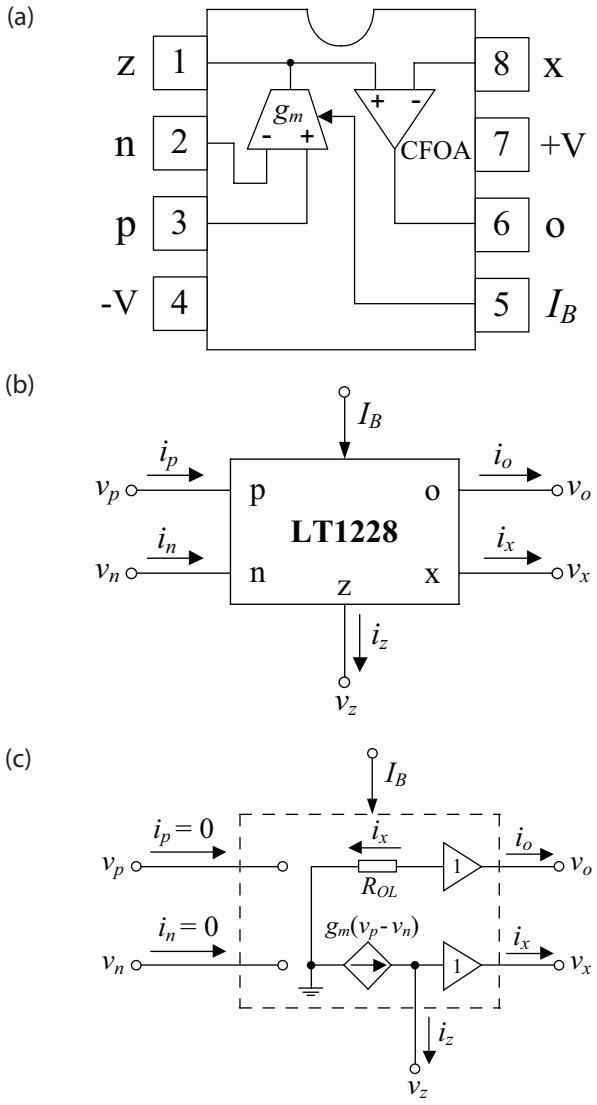


Figure 1: Commercially available IC LT1228: (a) package information; (b) electrical symbol; (c) equivalent circuit

2.2 Proposed floating capacitance multiplier design

The schematic diagram of the proposed floating capacitance multiplier circuit is given in Fig.2(a). It is composed of only two LT1228s, one resistor, and one capacitor. The equivalent circuit for the proposed capacitor implementation of Fig.2(a) is shown in Fig.2(b). Assuming that the matching condition of $g_m = g_{m1} = g_{m2}$ is satisfied, routing circuit analysis shows that the equivalent

input impedance looking between ports v_1 and v_2 of the proposed circuit in Fig.2(a) can be obtained as:

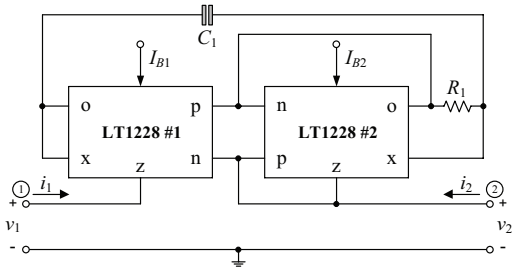
$$Z_{eq} = \frac{v_{id}}{i_{in}} = \left(\frac{v_1 - v_2}{i_1}\right) = \left(\frac{v_2 - v_1}{i_2}\right) = \frac{1}{sC_{eq}} = \frac{1}{s(g_m R_1 C_1)} \quad (3)$$

It is obvious that the proposed circuit of Fig.2(a) implements a floating tunable lossless capacitance with equivalent capacitance being given by:

$$C_{eq} = (g_m R_1) C_1 = K C_1 \quad (4)$$

where $K = g_m R_1$ represents the capacitance multiplication factor. The relation in (4) reveals that the capacitance magnification with a large multiplication factor is easily feasible by appropriate choosing g_m and/or R_1. Also from equation (2), the electronic tuning capability of the proposed design is evident through the bias currents of the LT1228s. It should be further noted here that two transconductance gains for this implementation need to be equal. This can be done easily by using simple current mirror to supply equal external bias currents to the two LT1228s.

(a)



(b)

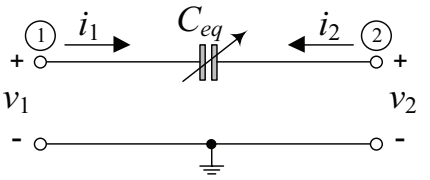


Figure 2: Proposed floating capacitance multiplier implementation: (a) circuit diagram; (b) ideal equivalent impedance

2.3 Non-ideality performance analysis

Consider the non-ideal transfer gains of the LT1228, the characteristic of the LT1228 given in equation (1) can be re-described by the following matrix equation:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_x \\ v_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 & 0 \\ 0 & 0 & \beta & 0 & 0 \\ 0 & 0 & 0 & R_{OL} & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_x \\ i_o \end{bmatrix} \quad (5)$$

In above equation, $\alpha = (1 - \varepsilon_{gm})$ and $\beta = (1 - \varepsilon_v)$, where $|\varepsilon_{gm}| << 1$ and $|\varepsilon_v| << 1$ are the transconductance tracking error and the voltage transfer error, respectively. Therefore, an analysis of the simulator given Fig.2(a) with the consideration of these parasitic gains gives the following expression for the equivalent input impedance looking into port 1 and ground as:

$$Z'_{eq1} = \left.\frac{v_1}{i_1}\right|_{v_2=0} = \frac{1}{sC'_{eq1}} = \frac{1}{s(g_{m1} R_1 C_1)(\alpha_1 \beta_1)} \quad (6)$$

It is obvious that the parasitic gains α_1 and β_1 directly deviate the value of the working capacitance C_1. To compensate for this, it can be governed by tuning the appropriate value for the $g_{m1}R_1$ product. On the other hand, the non-ideal equivalent impedance looking into port 2 and ground can be approximately found as:

$$Z'_{eq2} = \left.\frac{v_2}{i_2}\right|_{v_1=0} = \frac{1}{sC'_{eq2} + \left(\frac{1}{R'_{ex}}\right)} = \frac{1}{s(R_1 C_1 \beta_2)(g_{m2}\alpha_2) + (\beta_2 - 1)(g_{m2}\alpha_2)} \quad (7)$$

From equation (7), due to the LT1228 non-ideal gains, there is an extra undesired parallel resistance (R'_{ex}) appearing in parallel with the non-ideal equivalent capacitance. The non-ideal equivalent circuit for this case can then be represented as in Fig.3, where $C'_{eq2} = (R_1 C_1 \beta_2)(g_{m2}\alpha_2)$ and $R'_{ex} = 1/(\beta_2\text{-}1)(g_{m2}\alpha_2)$. Since a typical value of R'_{ex} is of the order of hundreds of kΩ, the parasitic elements C'_{eq2} and R'_{ex} introduce an extra pole at low frequency, which restricts the operating frequency range of the circuit. This effect on the frequency response of Z'_{eq2} will be shown in the following section.

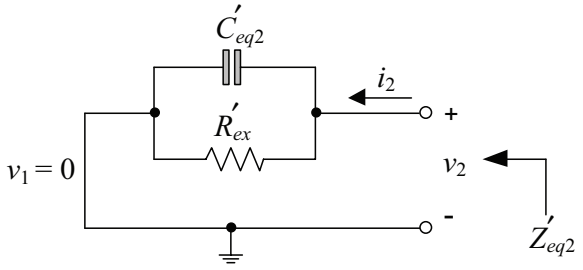


Figure 3: Non-ideal equivalent input impedance Z'_{eq2}.

In practice, if the parasitic impedances at the corresponding LT1228 terminals are taken into account, then the practical circuit model of the LT1228 can be drawn in Fig.4. At terminals p, n and z, there are the parasitic resistances R_p, R_n, and R_z appearing respectively in parallel with the parasitic capacitances C_p, C_n, and C_z. Their

impedance values are theoretically equal to infinity. On the other hand, the parasitic resistance R_x appears in series at terminal x. By considering $v_2 = 0$, the impedance of the designed capacitor with the consideration of the parasitic element effects can be given by:

$$Z''_{eq1} = \frac{v_1}{i_1}\bigg|_{v_2=0} = \frac{1}{sC''_{eq1}} = \frac{1}{s\left[\frac{g_{m1}R_1C_1}{1+\left(\frac{R_{x1}}{R_{OL1}}\right)} - C_{z1}\right] - \left(\frac{1}{R_{z1}}\right)} \quad (8)$$

where R_{OLi}, R_{xi}, R_{zi}, and C_{zi} (i = 1, 2) are the parasitic elements R_{OL}, R_x, R_z, and C_z of the i-th LT1228, respectively. For practical realization, R_{OL1} and R_{z1} are typically very large, yielding $R_{OL1} >> R_{x1}$ and $R_{z1} >> 1$. Therefore, an equivalent capacitance $C''_{eq1} \cong (g_{m1}R_1C_1 - C_{z1})$ is obtained from equation (8). It is further mentioned that there is not any additional parasitic pole and zero due to the parasitic elements, and the operating frequency limitation can be expressed as: $f \leq \min [1/2\pi(g_{m1}R_1C_1 - C_{z1})]$.

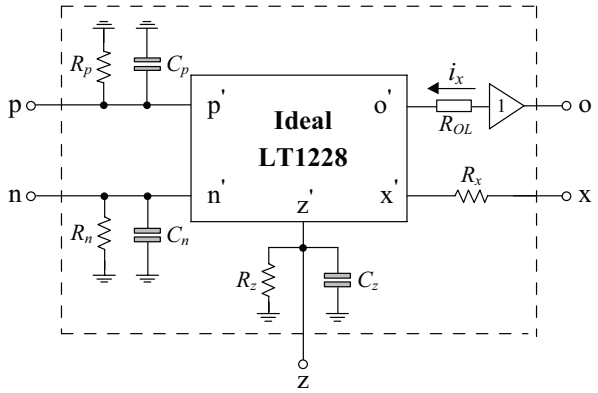


Figure 4: Practical LT1228 model with parasitic elements.

By defining $v_1 = 0$ and conducting relevant analyses, we can obtain the following expression for the non-ideal impedance seen between terminal 2 and ground as:

$$Z''_{eq2} = \frac{v_2}{i_2}\bigg|_{v_1=0} = \frac{1}{sC''_{eq2}} = \frac{1}{s\left[\frac{g_{m2}R_1C_1}{1+\left(\frac{R_{x2}}{R_{OL2}}\right)} - C''_2\right] - \left[\frac{g_{m2}}{1+\left(\frac{R_{OL2}}{R_{x2}}\right)} + \frac{1}{R''_2}\right]} \quad (9)$$

)

where $R''_2 = R_{n1}//R_{p2}//R_{z2}$ and $C''_2 = C_{n1}+C_{p2}+C_{z2}$. In equation (9), the negative terms exhibit non-ideal behavior of the proposed capacitance simulator by introducing a parallel resistive effect. Since $R_{OL2} >> R_{x2}$ and $R''_2 >> 1$, then equation (9) reduces to

$$Z''_{eq2} = \frac{1}{sC''_{eq2}} \cong \frac{1}{s\left[\frac{g_{m2}R_1C_1}{1+\left(\frac{R_{x2}}{R_{OL2}}\right)} - C''_2\right]} \quad (10)$$

The consideration of the above effect implies that in the frequency range of $f \leq \min [1/2\pi(g_{m2}R_1C_1 - C''_2)]$, and the inequality $g_{m2}R_1C_1 << C''_2$, the simulator operates practically as an expected ideal capacitance multiplier.

3 Computer simulation validation

To verify our proposed design, the circuit in Fig.2(a) has been simulated in PSPICE program using the macromodel parameters for the LT1228 provided by Linear Technology Corporation [14], with DC supply voltages of ±5 V. In simulations, the component values are taken as: R_1 = 1 kΩ, C_1 = 50 pF and $I_B = I_{B1} = I_{B2}$ = 200 µA. From equation (2), the transconductance gains are calculated as: $g_m = g_{m1} = g_{m2}$ = 2 mA/V. Also, from the relation in (4), the capacitance multiplication factor, and the simulated equivalent capacitance are calculated as: K = 2 and C_{eq} = 0.1 nF, respectively. The simulation results for input signals v_{id} and i_{in} of the proposed capacitance multiplier are given in Fig.5, when a 1-MHz sinusoidal signal of an amplitude 50 mV (peak) was applied as an input signal. The phase difference between v_{id} and i_{in} was observed to be 86.77° leading, as against the theoretical value of 90°. The corresponding frequency responses are also given in Fig.6. The total power consumption is measured to be 0.12 W when v_1 and v_2 are kept grounded.

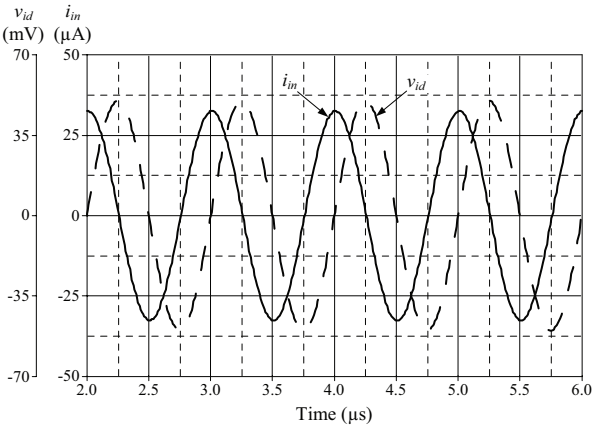


Figure 5: Simulation results for v_{id} and i_{in} of the proposed floating capacitance multiplier circuit in Fig.2(a).

In order to evaluate the impact of the unwanted parasitic resistance R'_{ex} the frequency responses of the non-

ideal equivalent impedance Z'_{eq2} ($Z'_{eq2} = v_2/i_2$) when v_1 =0 are depicted in Fig.7. It is observed that, at low frequency range between 1 kHz and 20 kHz, R'_{ex} mainly causes drop of the magnitude response of the Z'_{eq2} and also some deviates in phase response as depicted. However, some circuit techniques which reduce the parasitic impedance effects can be applied in the proposed capacitance multiplier circuit to improve the frequency performance [21]-[23].

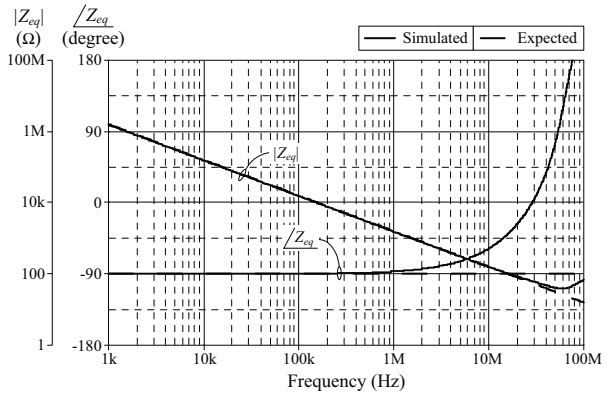


Figure 6: Expected and simulated frequency responses of the proposed floating capacitance multiplier circuit in Fig.2(a).

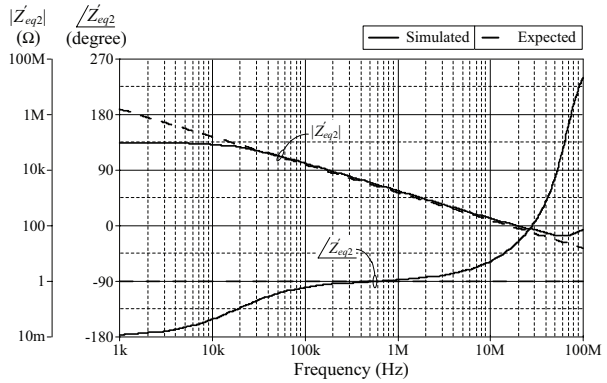


Figure 7: Frequency responses of the non-ideal equivalent input impedance Z'_{eq2} in Fig.3.

The adjustability of the proposed capacitance multiplier circuit is assessed by tuning the capacitance multiplication factor ($K = g_m R_1$), and also shown in Fig.8. Variations of C_{eq} against g_m and R_1 are demonstrated as examples. The C_{eq} tuning with g_m (varied from 0.1 mA/V to 10 mA/V) while keeping R_1 constant at 20 kΩ is shown in Fig.8(a), whereas the results in Fig.8(b) are obtained by setting g_m fixed at 10 mA/V and varying R_1 from 0.5 kΩ to 20 kΩ. It is evident from the results that the simulated capacitance value C_{eq} can enhance up to approximately 200 times with the maximum error in all cases less than 10%.

Fig.9 shows the temperature analysis results of the proposed capacitance multiplier circuit in Fig.2(a), where the ambient temperature is changed from 0°C to 100°C in the step of 20°C. From Fig.9, the simulation results demonstrate that the magnitude response has deviated with a variation of -8% ~ +22% over the temperature range of 0°C to 100°C.

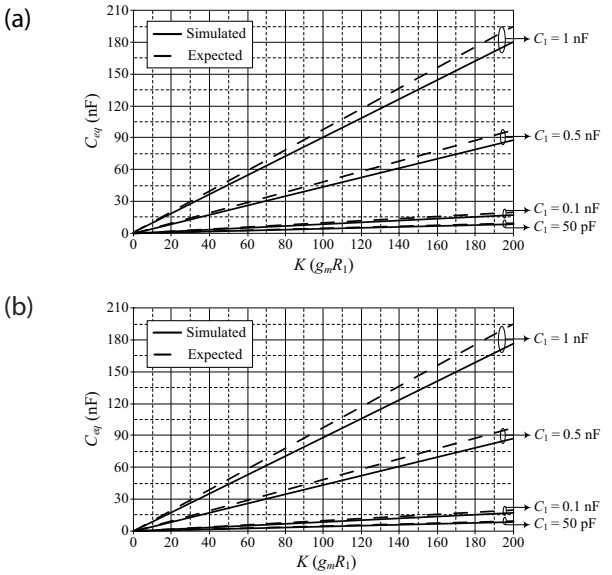


Figure 8: Variation of C_{eq} with the multiplication factor ($K = g_m R_1$): (a) g_m = 0.1 mA/V to 10 mA/V (I_B = 10 µA to 1000 µA) and R_1 = 20 kΩ; (b) g_m = 10 mA/V (I_B = 1000 µA) and R_1 = 0.5 kΩ to 20 kΩ

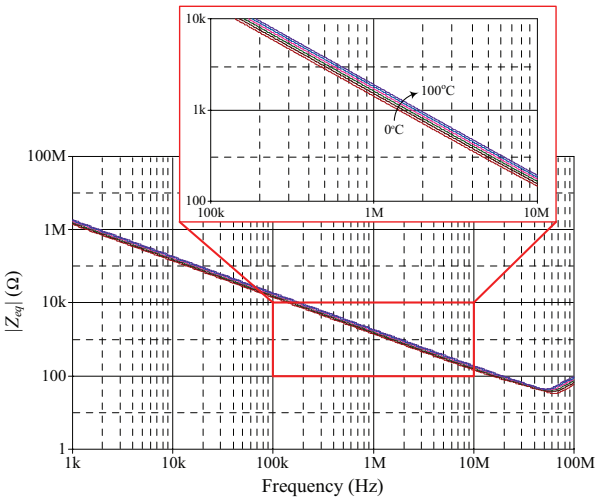


Figure 9: Temperature analysis results of the proposed floating capacitance multiplier circuit in Fig.2(a).

4 Experimental Evaluation

In the experimental evaluation, the availability of the proposed floating capacitance multiplier circuit in

Fig.2(a) has been verified in the laboratory using off-shelf IC's LT1228 [14] under ±5V supply voltages. All experimental measurements were performed through Keysight EDU-X 1002G oscilloscope and HP4395A impedance analyzer. To perform the experimental test, the components used have been: g_m = 2 mA/V (I_B = 200 µA), R_1 = 1 kΩ, and C_1 = 50 pF, yielding C_{eq} = 0.1 nF. Fig.10 shows the measured input waveforms v_{id} and i_{in} of the proposed circuit in Fig.2(a), when the input signal is 100 mV peak-to-peak at 1 MHz. The phase shift between v_{id} and i_{in} obtained from this experiment is measured as 86.8°. The corresponding frequency responses of the equivalent input impedance Z_{eq} are also represented in Fig.11. It appears from Figs.10 and 11 that the proposed circuit behaves as a lossless capacitor as expected.

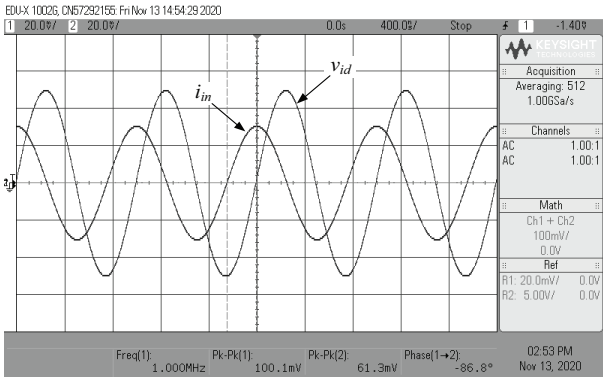


Figure 10: Measured time-domain behavior of the proposed floating capacitance multiplier circuit in Fig.2(a).

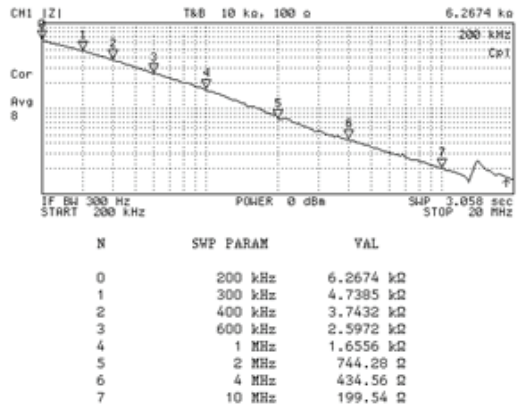
So as to survey the electronic tunability of the capacitance multiplier circuit, the measured magnitude and phase responses with three different values of g_m (i.e. g_m = 0.5 mA/V, 3 mA/V, and 5 mA/V) are shown in Fig.12. These results were obtained by taking R_1 = 1 kΩ and C_1 = 50 pF. This tuning process leads to obtain K = 0.5, 3 and 5 (C_{eq} = 25 pF, 0.15 nF, and 0.25 nF), respectively.

On the other hand, the magnitude-frequency responses of Z_{eq} for different values of R_1 are depicted in Fig.13. In Fig.13, setting g_m = 1 mA/V and C_1 = 50 pF, and different values for R_1 as 5 kΩ, 10 kΩ and 20 kΩ, results in the theoretical equivalent capacitances of C_{eq} = 0.25 nF, 0.5 nF, and 1 nF, respectively.

5 Illustrative application

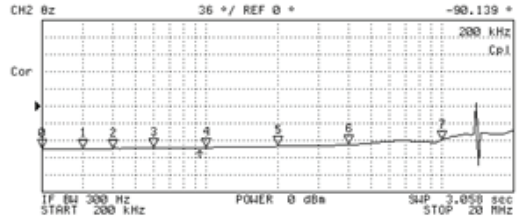
In this section, illustrative applicability of the proposed floating capacitance multiplier given in Fig.2(a) has been considered. It may be utilized in the implementation of the second-order RLC voltage-mode band-pass

(a)



N	SWP PARAM	VAL
0	200 kHz	6.2674 kΩ
1	300 kHz	4.7385 kΩ
2	400 kHz	3.7432 kΩ
3	600 kHz	2.5972 kΩ
4	1 MHz	1.6556 kΩ
5	2 MHz	744.28 Ω
6	4 MHz	434.56 Ω
7	10 MHz	199.54 Ω

(b)



N	SWP PARAM	VAL
0	200 kHz	-90.139 °
1	300 kHz	-89.404 °
2	400 kHz	-88.955 °
3	600 kHz	-88.053 °
4	1 MHz	-86.797 °
5	2 MHz	-84.349 °
6	4 MHz	-81.167 °
7	10 MHz	-71.401 °

Figure 11: Measured frequency behavior of the proposed floating capacitance multiplier circuit in Fig.2(a). (a) magnitude behavior ($|Z_{eq}|$); (b) phase behavior ($\angle Z_{eq}$)

(BP) filter as shown in Fig.14. The transfer function of the filter can be given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\left(\frac{R_{BP}}{L_{BP}}\right)s}{s^2 + \left(\frac{R_{BP}}{L_{BP}}\right)s + \left(\frac{1}{L_{BP}C_{eq}}\right)} \tag{11}$$

The center frequency (ω_c) and the quality factor (Q) are respectively expressed below:

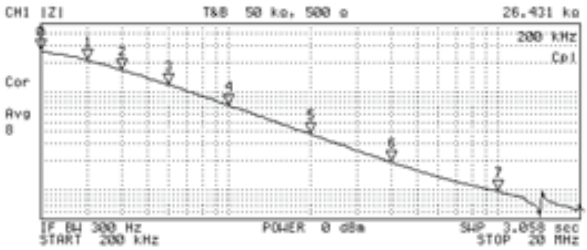
$$\omega_c = 2\pi f_c = \frac{1}{\sqrt{L_{BP}C_{eq}}} \tag{12}$$

and

$$Q = \left(\frac{1}{R_{BP}}\right)\sqrt{\frac{L_{BP}}{C_{eq}}} \tag{13}$$

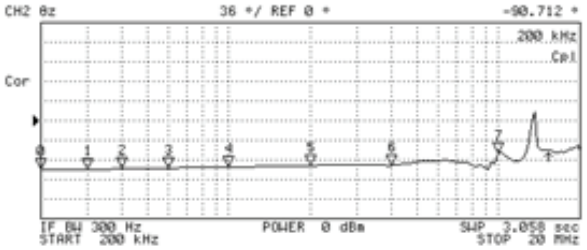
As an example for the circuit simulation, the following passive and active components were chosen as: R_{BP} = 3.3 kΩ, L_{BP} = 1 mH, and C_{eq} = 0.1 nF (g_m = 2 mA/V, R_1 = 1

Magnitude response



N	SWP PARAM	VAL
0	200 kHz	26.431 kΩ
1	300 kHz	22.523 kΩ
2	400 kHz	16.875 kΩ
3	600 kHz	11.838 kΩ
4	1 MHz	7.3235 kΩ
5	2 MHz	3.7322 kΩ
6	4 MHz	1.9232 kΩ
7	10 MHz	964.2 Ω

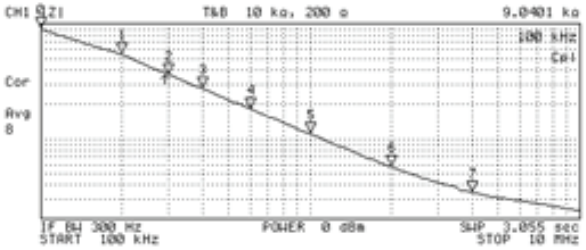
Phase response



N	SWP PARAM	VAL
0	200 kHz	-90.712 °
1	300 kHz	-89.632 °
2	400 kHz	-88.507 °
3	600 kHz	-86.948 °
4	1 MHz	-85.231 °
5	2 MHz	-82.577 °
6	4 MHz	-83.156 °
7	10 MHz	-61.257 °

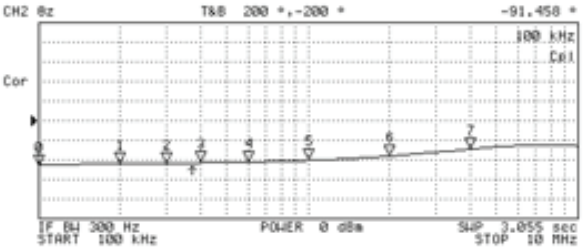
(a)

Magnitude response



N	SWP PARAM	VAL
0	100 kHz	9.0401 kΩ
1	200 kHz	5.4065 kΩ
2	300 kHz	3.6174 kΩ
3	400 kHz	2.7185 kΩ
4	600 kHz	1.818 kΩ
5	1 MHz	1.0969 kΩ
6	2 MHz	568.71 Ω
7	4 MHz	339.95 Ω

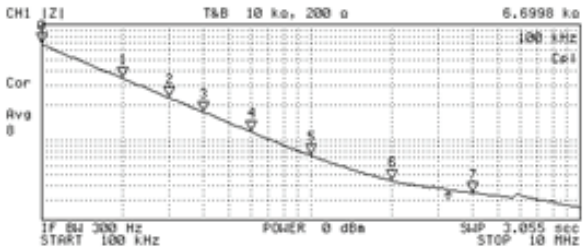
Phase response



N	SWP PARAM	VAL
0	100 kHz	-91.458 °
1	200 kHz	-87.653 °
2	300 kHz	-87.022 °
3	400 kHz	-86.241 °
4	600 kHz	-84.588 °
5	1 MHz	-81.155 °
6	2 MHz	-72.427 °
7	4 MHz	-57.8 °

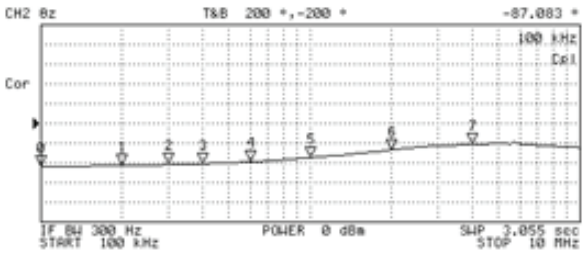
(b)

Magnitude response



N	SWP PARAM	VAL
0	100 kHz	6.6998 kΩ
1	200 kHz	3.4039 kΩ
2	300 kHz	2.2913 kΩ
3	400 kHz	1.7308 kΩ
4	600 kHz	1.1679 kΩ
5	1 MHz	728.97 Ω
6	2 MHz	438.58 Ω
7	4 MHz	342.88 Ω

Phase response

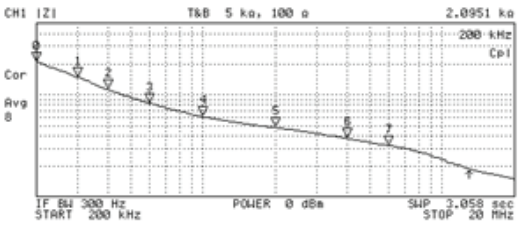


N	SWP PARAM	VAL
0	100 kHz	-87.083 °
1	200 kHz	-85.402 °
2	300 kHz	-83.531 °
3	400 kHz	-81.618 °
4	600 kHz	-77.721 °
5	1 MHz	-69.601 °
6	2 MHz	-53.82 °
7	4 MHz	-42.191 °

(c)

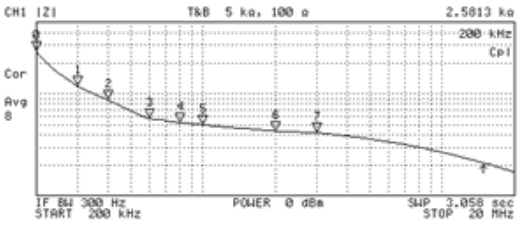
Figure 12: Measured frequency responses of Z_{eq} for different g_m.(a) g_m = 0.5 mA/V (K = 0.5, C_{eq} = 25 pF); (b) g_m = 3 mA/V (K = 3, C_{eq} = 0.15 nF); (c) g_m = 5 mA/V (K = 5, C_{eq} = 0.25 nF)

(a)



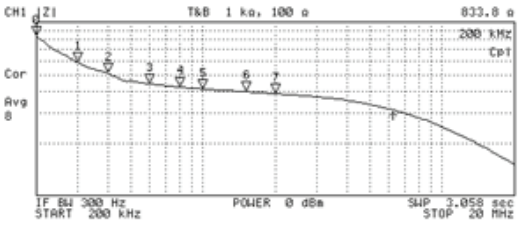
N	SWP PARAM	VAL
0	200 kHz	2.0951 kΩ
1	300 kHz	1.4825 kΩ
2	400 kHz	1.1176 kΩ
3	600 kHz	819.72 Ω
4	1 MHz	605.91 Ω
5	2 MHz	473.06 Ω
6	4 MHz	371.67 Ω
7	6 MHz	317.08 Ω

(b)



N	SWP PARAM	VAL
0	200 kHz	2.5813 kΩ
1	300 kHz	1.187 kΩ
2	400 kHz	860.11 Ω
3	600 kHz	565.6 Ω
4	800 kHz	516.3 Ω
5	1 MHz	492.23 Ω
6	2 MHz	427.13 Ω
7	3 MHz	411.61 Ω

(c)



N	SWP PARAM	VAL
0	200 kHz	833.8 Ω
1	300 kHz	587.5 Ω
2	400 kHz	505.98 Ω
3	600 kHz	440.37 Ω
4	800 kHz	421.06 Ω
5	1 MHz	411.32 Ω
6	1.5 MHz	397.1 Ω
7	2 MHz	386.81 Ω

Figure 13: Measured magnitude-frequency responses of Z_{eq} for different R_1(a) R_1 = 5 kΩ (K = 5, C_{eq} = 0.25 nF); (b) R_1 = 10 kΩ (K = 10, C_{eq} = 0.5 nF); (c) R_1 = 20 kΩ (K = 20, C_{eq} = 1 nF)

kΩ, and C_1 = 50 pF). The ideal and simulated frequency responses of the filter in Fig.14 are exhibited in Fig.15, in which the calculated and simulated values of f_c are found to be 503 kHz and 509 kHz, respectively. The simulated frequency characteristics are in good agreement with the predicted responses, thereby confirming the practical utility of the proposed capacitance multiplier circuit. The corresponding frequency spectrum of the output voltage (v_{out}) of the BP filter is also recorded in Fig.16, where the total harmonic distortion (THD) values observed is well within 1.17%.

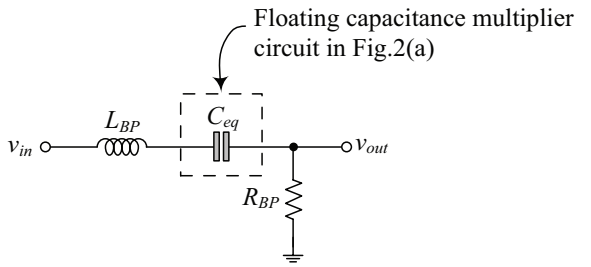


Figure 14: Second-order RLC voltage-mode BP filter implemented with C_{eq} from Fig.2(a).

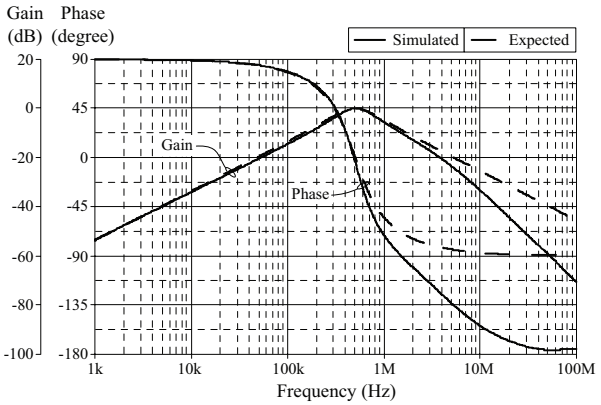


Figure 15: Expected and simulated frequency characteristics of the BP filter in Fig.14.

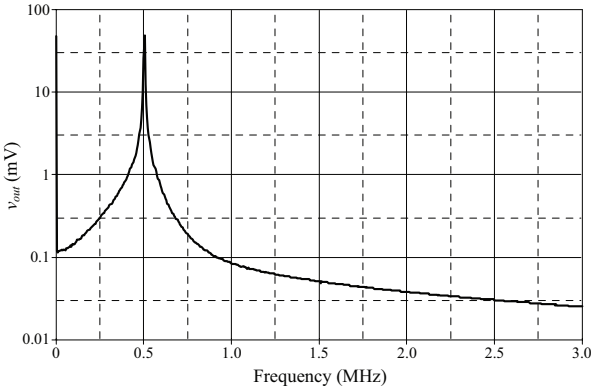


Figure 16: Output frequency spectrum of v_{out}.

Finally, in order to inspect random deviations of the BP filter center frequency due to the process and mismatch variations, Monte-Carlo analysis simulation has been evaluated with the same given parameters that resulted in the frequency characteristic of Fig.15. The simulations were performed 200 times with a 5% Gaussian deviation of relevant g_m, R_1, and C_1. The histogram of the center frequency is shown in Fig.17. According to statistical analysis results, the mean value is at 522 kHz with a standard deviation of 9.4 kHz, corresponding to 1.8% deviation from the nominal value.

6 Conclusive Discussion

This work is an attempt to present a practical realization of the tunable floating capacitance multiplier circuit using a commercially available IC LT1228. The synthetic capacitance simulator is constructed with two LT1228s, one resistor, and one capacitor. The electronic tuning feature of the simulated floating capacitor can be achieved by means of external bias currents of the IC LT1228s. The communication further discusses a second-order RLC voltage-mode band-pass filter to validate the applicability of the proposed capacitor simulation. PSPICE simulation and experimental results of the commercially available IC LT1228 are also included to demonstrate the convincing characteristics of the proposed circuit and its practical significance.

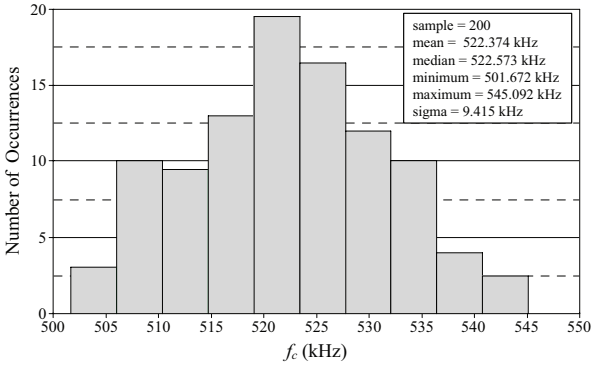


Figure 17: Monte-Carlo analysis results showing the deviation in the standard deviations of the BP filter center frequency.

7 Acknowledgment

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8 Conflict of interest

The authors confirm that this article content has no conflict of interest.

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