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The Implementation of Logic Gates Using Only Memristor Based Neuristor

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Abstract: One can learn about memristor-based neuron circuits in literature if one wishes to implement more effective circuits, as they are linear, have a high density, and consume little energy. This paper presents two logic gates based on memristor-based neurons. The neuron circuit can float, and therefore can be used as a circuit element. Electronic neurons, or neuristors, generate spikes when DC current is applied to them; likewise, the proposed logic gates generate spikes when appropriate inputs are applied to them. We simulated the proposed gates with SPICE using TSMC 0.18 µm CMOS process models.

Keywords: AND gate; OR gate; Neuron; Memristor; Neuristor

Uporaba logičnih vrat le z uporabo nevristorja na osnovi memristorja

Izvleček: Nevronks vezja na osnovi memristorja so linearna, velike gostote in porabijo malo energije. Članek predstavlja doje vrat na odnovi nevronov, ki temljijo na memristorjih. Nevronsko vezje lahko plava in se zato lahko uporablja kot element vezja. Elektronski nevroni ali nevristorji ustvarijo pri enosmernem toku konice; prav tako predlagani logični vhodi, pri ustreznem vhodnem signal, generirajo konice. Predlagana vrata smo simulirali s SPICE okolju z uporabo TSMC 0,18 µm CMOS tehnologije.

Ključne besede: IN vrata; ALI vrata; Nevron; Memristor; Nevistor

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1 Introduction

In, 1952, Hodgkin and Huxley proposed an electrical circuit model of an axon membrane [1] with passive circuit elements. The Hodgkin-Huxley (HH) model explains how the membrane potential gets conducted from one cell to another cell. The HH circuit is composed of three channels: a sodium channel, a potassium channel, and a leakage channel. The sodium and potassium channels are modelled with a capacitor and parallel nonlinear resistors. To understand how the brain works, researchers present realistic neuron models and circuits [2]-[5].

Leon Chua defined a new circuit element, dubbed a memristor, and demonstrated the connection between charge and flux [6],[7]. But memristors did not attract anyone's interest until the HP research group had managed to implement them as solid state devices [8]. The new element has nonlinear characteristics, memory, and an ultra-dense structure. Many types of of memristor emulator circuit ([9]; [10]; [11], [12] [13]; [14]) have been proposed given that it was not commercially available. More and more researchers' now are interested in modelling neuron and neural networks using memristors. Pickett and co-workers implemented a mottmemristor and memristor-based neuron circuit in Nature [15]. Shin et al. presented a memristor-based neuron circuit. Here, nonlinear opening and closing of sodium and potassium ion channels are modelled with a memristor [16]. Ren et al. proposed a model for connected neurons. [17]. Zhang and Liao created the memristor-based circuit of the FitzHugh-Nagumo

model and investigated the dynamic behaviour of neuronal circuit networks using memristors as a synapses [18]. Feali et al. modified the Pickett's circuit using both memristor and memcapacitor SPICE models [19].

This study presents two logic gates using a memristor-based floating neuristor circuit. The memristor in question is based on OTA (Operational Transconductance Amplifier), and has a fully floating structure. The neuristor also has a floating structure and generates voltage spikes when DC input current is applied to it. The neuristor-based logic gates behave as an AND and OR gate depending on the input signal amplitude. All of the simulation results are compatible with previous studies

2 Floating memristor circuits

We have used two memristor emulator circuits using two different operational transconductance (OTA) elements (Fig.1). The symmetric OTA used in this study was designed for the TSMC 0.18u process (Fig.1c.) The capacitor provides the memristor's memory behaviour; transistors behave as nonlinear resistors when operating in the subthreshold region. The transistors we've used are of a p-type. Their bulk terminals should be connected to the highest voltage in the circuit. We connected them bulk terminals to the drain terminals to provide more nonlinearity. Therefore, we were able to obtain more nonlinear memristive behaviour. The implementation of this memristor has been presented previously in [20]. First memristor (Fig.1a) is nonvolatile,

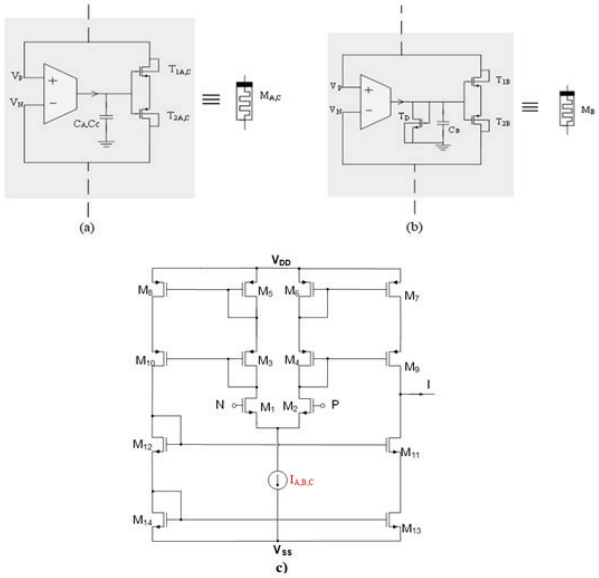

Figure 1: The circuit schematics of memristor emulators a) Fully floating memristor emulator circuit b) Modified fully floating memristor emulator circuit c) OTA circuit.

whilst the second memristor (Fig.1b) is volatile because of the T_D transistor. The memristor emulators fully float thanks to their symmetric structures. The OTA provides current to the capacitor, which is connected to the gate terminals of transistors. The charging and discharging mechanism provides both a memory effect and results in the memristor's resistance.

3 Memristor based neuristor circuit

Memristor-based electronic neurons were reported by Pickett and co-workers using mott memristors [15]. Feali put forth the memristor based neuristor SPICE model [19] after they were able to produce a electronic neuron (neuristor). The circuit we used in this study (Fig. 2) is composed of three memristors [20]. Two of them have parallel capacitors that emulate channel-I and channel-II. Neurons are composed of many types of channels, namely sodium, potassium, and calcium. However, only sodium and potassium channels are represented in Hodgkin & Huxley model [1]. The other channels are not very important (in comparison to sodium and potassium), and they represent a leakage channel in Hodgkin & Huxley's circuit model [1]. Therefore, we thought of these two key channels as channel-1 and channel-2. The capacitors model the channel capacitance. Memristors employ model the channel conductance. The conductances of memristors change when a DC input signal is applied, thereby charging and discharging the capacitor, and ultimately leading to voltage changes. If we control the voltage change, we can produce a spike train. Channel-I and channel-II behave as nonlinear resistors thanks to M_A and M_C memristors. These two channels are separated by a M_B nonlinear memristor. Channel-II is isolated from the output terminal of the circuit by Rout and C_{out}, which are located in the output stage of circuit. Moreover, both circuit elements also provide nonlinearity (thanks to the charging/discharging mechanisms of the capacitor) as well as an appropriate voltage drop to produce spike trains.

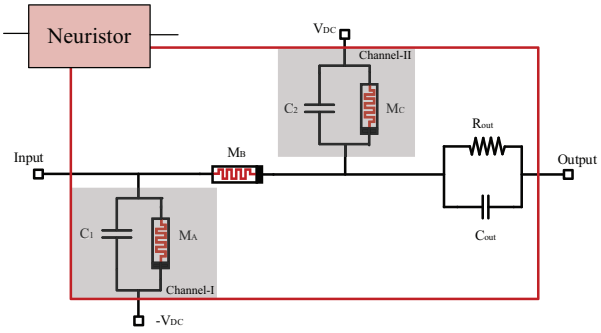

Figure 2: Memristor based floating neuristor circuit. Here, the M_A and M_C memristors have identical structure and the M_B memristor has modified structure [20].

Table 1: The values of the circuit elements.

Transistors	W(μm)	L(μm)	Capacitors	
$T_{1\text{-}2A}$	3	1	C_A	10 nF
$T_{1\text{-}2B}$	400	1	C_B	1 nF
$T_{1\text{-}2C}$	1	1	C_C	10 μF
T_D	1.6	1	C_1	10 nF
C_{out}	10 pF		C_2	1 pF
Currents (μA)			Voltage Sources (V)	
I_A	1		$V_{DD\text{-}A,C}$	0.9
I_B	100		$V_{SS\text{-}A,C}$	-0.9
I_C	0.1		$V_{DD\text{-}B}$	2
R_{out}	10 MΩ		$V_{SS\text{-}B}$	-2

The output stage of the circuit consists of one resistor and one capacitor. Spikes formation directly depends on the values of circuit elements and all values listed in Table 1. All simulations have been carried out using TSMC 0.18μm CMOS. We want to show the operation of one memristor when DC current is applied. Neurons can produce various spike types – e.g. fast spikes, initial bursting, and chattering. The details of these spike types can be found in [5]. Our circuit produced a regular spike type, a widely-known spike commonly used in VLSI design. The applied DC current and resulting voltage spikes are shown in Fig.3. The neuristor produces a spike train a DC current is applied. There are no observable spikes when a zero input signal is applied. Here, the applied DC signal value is 250nA; the resulting spike train amplitude changes from -1.3 V to 0.5V

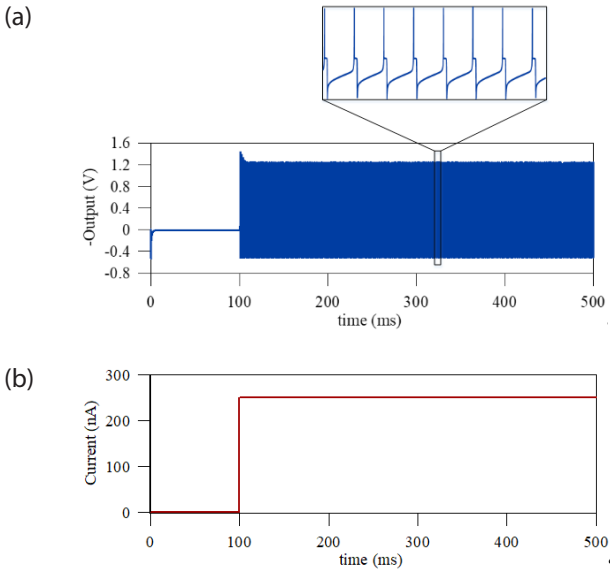

Figure 3: a) The response of neuristor circuit and b) applied input DC current signal.

4 Neuristor based logic gates

As shown in Fig.4, two neuristors are connected in a parallel fashion and then serial to another neuristor to obtain logic gates. These logic gates have two inputs and one output. The circuit behaves as both an AND and OR gate, depending on the amplitude of the applied signal. If the input signal amplitude reaches 40μA, the circuit behaves as an AND gate. If the applied signal reaches 150μA, then the circuit behaves as an OR gate. We applied 40μA current signals to both terminals of the proposed circuit (Fig.5b-c). If the applied input signals reach 40μA at the same time, the output of the circuit produces a spike train. However, if any of the inputs drop to zero, the circuit does not generate any output signal. In other words, the circuit behaves as an AND gate.

To obtain OR gate behaviour from the proposed circuit, we applied 150μA current signals to both terminal of the proposed circuit (Fig.6b-c). If one of the applied input signals reaches 150μA, then the circuit produces a spike train. However, if both of the inputs drops to zero, then the circuit does not produce any output signal at all. In other words, the circuit behaves as an OR gate.

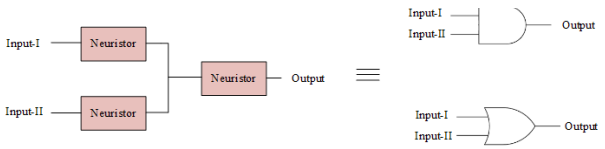

Figure 4: The circuit schematic of the neuristor based logic gates and their circuit symbols.

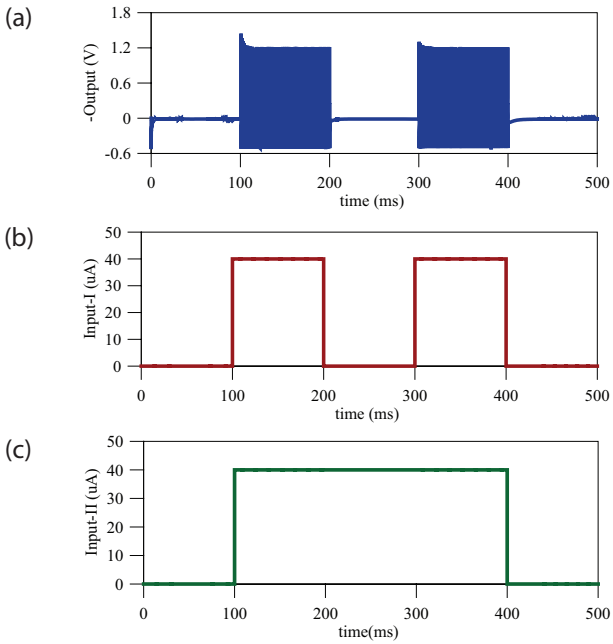

Figure 5: a) The response of neuristor based AND gate b) applied input signal-I c) input signal-II.

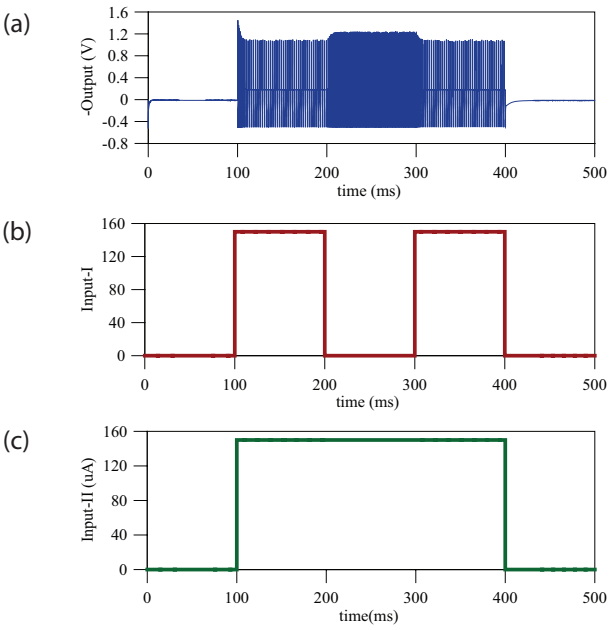

Figure 6: a) The response of neuristor based OR gate b) applied input signal-I c) input signal-II.

5 Conclusions

In this paper, we presented logic gates based on floating neuristor circuits. The neuristors are composed of two different OTA-based memristors that can fully float. The used memristor circuit has a very low current consumption; therefore, the neuristor circuit consumes little power. We were able to obtain both logic behaviours from only one circuit by changing the input signal amplitude. All of the simulations were carried out using TSMC 0.18.

6 Conflict of interest

The authors declare that there is no conflict of interest for this paper.
Also, there are no funding supports for this manuscript.

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