Original scientific paper
https://doi.org/10.33180/InfMIDEM2021.405

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 51, No. 4(2021), 253 – 259

Reduction of Random Dopant Fluctuation-induced Variation in Junctionless FinFETs via Negative Capacitance Effect

Bo Liu, Xianlong Chen, Ziqiang Xie, Mengxue Guo, Mengjie Zhao, Weifeng Lü

Hangzhou Dianzi University, Key Laboratory for RF Circuits and Systems of Ministry of Education, Hangzhou, China

Abstract: In this study, we investigated the impact of random dopant fluctuation (RDF) on junctionless (JL) fin field-effect transistors (FinFETs) with ferroelectric (FE) negative capacitance (NC) effect. The RDF-induced variations were captured by using built-in Sano methodology in three-dimensional technology computer-aided design (TCAD) simulation. Compared to the regular JL-FinFETs, the variations in JL-FinFETs with NC effect (NCJL-FinFETs) was observed to be less via statistical Monte Carlo analysis, which further enhanced its performance as well. The evaluation and estimation of threshold voltage (V_T), ON-state current (I_{on}), OFF-state current (I_{off}), and subthreshold swing (SS) by different FE layer thicknesses indicated reduction in the standard deviations of VT (δV_T) and Ion (δI_{on}) by 34.7% and 7.08%, respectively; the OFF-state current and its standard deviation shrank by approximately three orders of magnitude than the JL-FinFET counterpart. Although δSS was not monotonous, the SS was significantly improved to sub-60 mV/decade. To sum up, the regular JL-FinFETs containing the FE layer as NC effect not only improved the electrical performance, but also led to the resilience of the RDF-induced statistical variability.

Keywords: Random dopant fluctuations (RDF); negative capacitance effect; junctionless FinFETs; Monte Carlo analysis

Zmanjšanje naključnih nihanj zaradi fluktuacije dopantov v brezspojnih FinFET-ih preko učinka negativne kapacitivnosti

Izvleček: V študiji smo raziskali vpliv naključnega nihanja dopantov (RDF) na brezspojne (JL) poljske fin tranzistorje (FinFETs) s feroelektričnim (FE) učinkom negativne kapacitivnosti (NC). Nihanja, ki jih povzroča RDF, so bila zajeta z uporabo vgrajene Sano metodologije v tridimenzionalni računalniško podprti simulaciji tehnologije (TCAD). V primerjavi z običajnimi JL-FinFET-i je bilo s statistično analizo Monte Carlo ugotovljeno, da so spremembe pri JL-FinFET-ih z učinkom NC (NCJL-FinFET-i) manjše, kar je dodatno izboljšalo tudi njihovo zmogljivost. Ocenjevanje in vrednotenje napetosti praga (V_T), toka v stanju ON (I_{on}), toka v stanju OFF (I_{off}) in pod pragovnega nihanja (SS) z različnimi debelinami plasti FE, je pokazalo zmanjšanje standardnih odklonov V_T (δV_T) in Ion (δI_{on}) za 34,7 % oziroma 7,08 %; tok v stanju OFF in njegov standardni odklon sta se v primerjavi s podobnimi JL-FinFET zmanjšala za približno tri velikostne rede. Čeprav δSS ni bil monoton, se je SS znatno izboljšal, in sicer na manj kot 60 mV/dekado. Če povzamemo, običajni JL-FinFET, ki vsebujejo plast FE kot učinek NC, niso izboljšali le električnih lastnosti, temveč so tudi pripomogli k odpornosti na statistično variabilnost, ki jo povzroča RDF.

Ključne besede: naključne fluktuacije dopantov (RDF); učinek negativne kapacitivnosti; brezspojni FinFET-i; analiza Monte Carlo

** Corresponding Author's e-mail: lvwf@hdu.edu.cn*

1 Introduction

Over the years, fabrication of the field-effect transistors (FETs) with p-n junctions requires very steep doping concentration gradients between the silicon-bulk channel and source/drain (S/D) region [1-2]. Moreover, the formation of steep gradient p-n junction requires

How to cite:
B. Liu et al., "Reduction of Random Dopant Fluctuation-induced Variation in Junctionless FinFETs via Negative Capacitance Effect", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 51, No. 4(2021), pp. 253–259

ultra-fast thermal annealing process, which greatly increases the cost budget of manufacturing of equipment. To avoid the difficulty of making such p-n junctions, junctionless field-effect transistors (JL-FETs) were introduced [3-5]. JL-FETs involve the identical concentration of a single doping species along the semiconductor region, which are easier to fabricate than the inversion-mode FETs (IM-FETs) [6]. JL-FETs have nearly ideal subthreshold swing (SS), extremely low leakage current and smaller mobility degradation [7]. For these reasons, JL-FETs recently received significant attention as a potential replacement of IM-FETs in the future. In addition, negative capacitance field-effect transistors (NCFETs), which are fabricated by drawing into the ferroelectric (FE) material behaving as a series of NC stacked on the gate of the traditional complementary metal-oxide-semiconductor (CMOS) devices generally possess a higher performance and lower power consumption [8-10]. Owing to the good compatibility of the doped HfO2 layer with conventional high-κ semiconductor technology, the NCFETs have great potential to realize ultra-low power consumption and high-efficient switching even for sub-3 nm technology node [11]. Therefore, JL-FETs with NC effect are considered as a promising candidate for fabricating next generation advanced CMOS devices in lower power application.

However, random dopant fluctuation (RDF) as one of the most concerned variation sources for ultra-small semiconductor devices with further scaling has shown that its impact on the JL-FETs is more serious than the IM counterparts due to the heavy doping of dopant atoms [12-14]. Investigation also reports that JL-FETs are more sensitive to RDF than IM-FETs in baseline doping levels in silicon-bulk channel [15]. In rencent years, many novel junctionless architectures have been published in reputed journals, like Nanowire junctionless FETs and Nano tube junctionless FETs [16-17]. Therefore, electrical properties variability of conventional JL-FETs induced by RDF is going to be a worthwhile concern when the device scales to the nanometer region with the total number of dopant atoms increasingly discretized.

Several works have demonstrated that the NC effect can improve the performance of RDF-induced variability for conventional IM-FETs as well as planar NCFET-based CMOS circuits [18-20]. However, the NC effect on RDF-induced variations in JL triple-gate fin-type FET (JL-FinFET) has not been understood profoundly yet. Therefore, we have focused on the deficiency for JL-FinFET with NC effect in this work. In addition, the impact of doped HfO2 as different FE layer thickness on NC JL-FinFETs has been investigated in detail.

2 Negative capacitance and device structure

In recent years, ferroelectric materials have gained a lot of attention in the field of semiconductors. It was the first time that Sayeef Salahuddin and Supriyo Datta [21] adopted the NC effect of FE layers stacked on the gate of IM-FET, which had the ability to break the fundamental lower limit of 60 mV/decade SS to reduce the power dissipation. Many experiments in NC effect have proved that it can achieve the Sub-60mV/dec SS and lower the power [22-23]. In this study, the structure of the FE stacked around the gate-oxide layer is depicted in Figure .1 (a). The NC and the internal gate capacitance of the body can be considered as the following equivalent circuit depicted in Figure .1 (b). The device parameters are listed in Table 1. Incorporating the Landau–Khalatnikov (L-K) theory of NC effect in FE materials with the JL-FinFET structure constitutes the NCJL-FinFET [24]. The dynamic of NC can be expressed using the L-K equation as shown in Eq. 1:

$$E=2\alpha P+4\beta P^3+6\gamma P^5+\rho\frac{dP}{dt} \quad (1)$$

where α, β and γ are intrinsic parameters for FE materials, and ρ is a constant viscosity parameter which relies on the amplitude of the applied voltage. The voltage across the FE capacitor ($V_{FE} = V_{GS} - V_{IN}$) versus charge can be computed using the L-K equation:

$$V_{FE}=(2\alpha Q+4\beta Q^3)\times T_{fe} \quad (2)$$

where T_{fe} represents FE thickness, and Q is the surface charge density. α and β are Landau coefficients related to L-K equations and can be calculated by adapting the FE Q-VFE characteristics to obtain the existing values of remnant polarization P_r and coercive field E_c. In this study, P_r = 5 μC/cm² and E_c = 1 MV/cm were adopted in the HfO2-based FE material [25]. Based on this, we obtained $\alpha = -\frac{3\sqrt{3}}{4}\times\frac{E_C}{P_r}$, $\beta = \frac{3\sqrt{3}}{8}\times\frac{E_c}{P_r^3}$ and γ = 0 [26]. C_{FE} is the FE capacitance and is defined by dQ/dV_{FE}. From Eq. (2), C_{FE} can be expressed as,

$$C_{FE}^{-1} = (2\alpha + 12\beta Q^2)\times T_{fe} \quad (3)$$

The total gate capacitance C_T for NC-JL-FinFET can be obtained by:

$$C_T^{-1} = C_{FE}^{-1} + C_S^{-1} \quad (4)$$

The equation of the inner gate voltage V_{IN} and Ferroelectric capacitance can be expressed by:

$$V_{IN} = \frac{|C_{FE}|}{|C_{FE}| - C_S} V_{GS} \quad (5)$$

The increased total gate capacitance was derived by the NC effect of the FE layer stacked around the gate, which amplifies the internal voltage.

Table 1: Device parameters of the baseline JL-FinFET

Device Parameters	Value
Fin Width	5 nm
Fin Height	15 nm
Gate Length	20 nm
Oxide Layer thickness	0.9 nm
Spacer Thickness	5 nm
Source/Drain Length	15 nm
Channel Length	30 nm
Doping Concentration	$1.0e^{18}cm^{-3}$-$1.0e^{20}cm^{-3}$

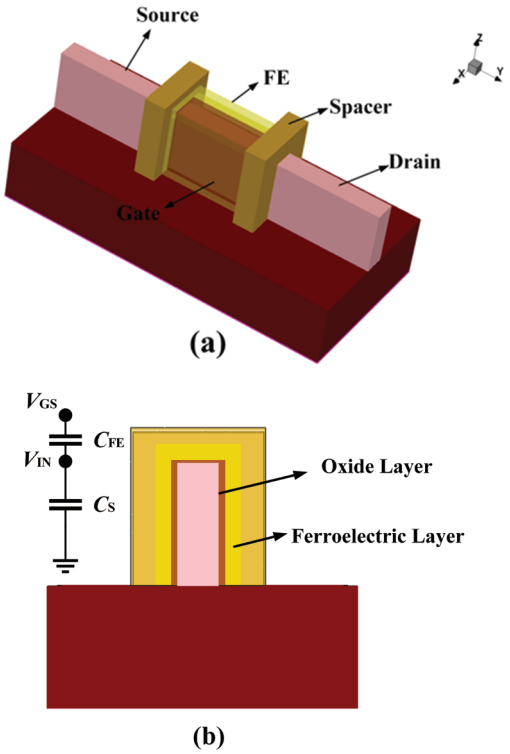

Figure 1: (a) Overall view and (b) lateral view of JL-FinFET.

3 Simulation scheme for RDF effect

To explore three-dimensional (3D) RDF effect on multiple thicknesses of the FE layer stacked around the gate of JL-FinFET, we utilized Sentaurus TCAD toolset, which contains 3D quantum correction (QC) drift-diffusion and QC Monte Carlo (MC) transport models, was employed for accurate mesh description [27]. The doping profile of the n-type NCJL-FinFET is depicted in Figure 2. We can see that the randomization of the arsenic atoms in the silicon-channel has been accomplished by built-in Sano method. The effect of randomization was supported by charge density theory. The doping profile was created using the following equation [28]:

$$\rho(r) = qk_c^3[\sin(k_c r) - k_c r\cos(k_c r)] \,/\, [2\pi^2(k_c r)^3] \quad (6)$$

where $k_C \approx 2n_{D/A}^{1/3}$ is the screening factor, and r is the radial distance from the center of the atoms, the $n_{D/A}$ represents the concentration of donors/acceptors. The Sano method adopts the above function to simulate the doping profile in the channel.

During the simulation, the drift diffusion was adopted in carriers' transport model based on the self-consistent solution of the Poisson equation. To prevent the disturbance of unphysical charge trapping and initiate further efforts to specify the nano-scale electronic devices with the short channel effect [29], the quantum mechanical effect was considered during the simulation of the NCJL-FinFET. The mobility model was incorporated with the high-field saturation and Shockley Read Hall physical model to accomplish the recombination and generation [30]. As a consequence of the time consumption of each randomization device, 200 randomization samples comprising varying doping profiles were reproduced. Subsequently, the overall statistical results of the RDF-induced variations in NCJL-FinFET were reproduced by the simulator.

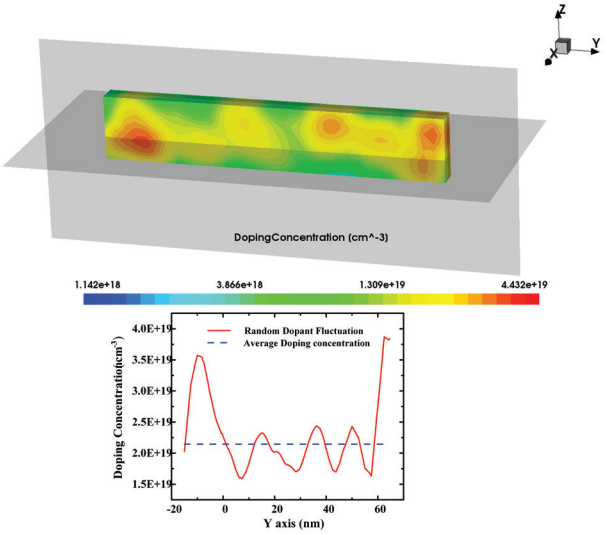

Figure 2: Randomized doping profile and structure of the n-type NCJL-FinFET.

4 Results and discussion

Figures .3(a)–(d) compare the ID-VG transfer characteristics of JL-FinFET without (T_{fe}=0 nm) and with (T_{fe} = 1, 2, 3 nm) NC effect (NCJL-FinFET) in uneven doping concentration levels at a drain biased voltage of 0.7 V. The normalized ID-VG curve was compared and calibrated with other published work. It can be observed that the OFF-state current (I_{off}) obviously decreases and ON-state current (I_{on}) slightly increases with the increase of the FE layer thickness. Due to the NC effect, the transport of the carriers in the silicon-bulk channel at low drain voltage (V_{DS}) was strongly controlled by the longitudinal electric field of gate voltage (V_{GS}) which is subject to the hysteresis in the NC region. In addition, it can be seen that the curve dispersion of randomly reproduced samples is gradually suppressed with the increment of the FE layer thickness; meanwhile the slop of the ID-VG curves gets slightly steeper. It can be computed that the switching current ratio (I_{switch} = I_{on}/ I_{off}) of the devices raises two orders of magnitude and becomes 400 times larger than that of regular JL-FinFETs. The I_{switch} can reach to 4.408e10 at T_{fe} = 3 nm. The huge I_{switch} contributes by the NC effect of the FE layer. However, for the standard deviation of I_{switch} (δI_{switch}), it represents the monotonic trends due to the OFF-state current being more vulnerable to the influence of the discrete dopant atoms. Therefore, JL-FinFETs with the NC effect exhibit more tolerance toward the transfer characteristics fluctuation induced by the RDF.

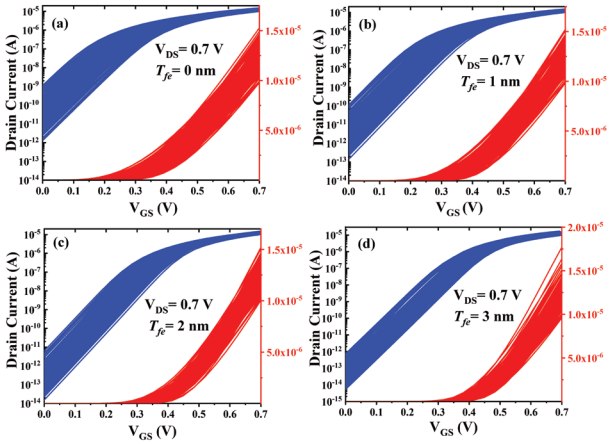

Figure 3: (a)–(d) ID-VG transfer characteristics of NCJL-FinFET with different thicknesses of ferroelectric layers

Figure .4(a) depicts the means of the threshold voltage (V_T) and subthreshold swing (SS) at a drain bias voltage of 0.7 V. We could observe that SS gradually decreases and VT gradually increases at T_{fe} less than 3 nm. However, an inflection point emerges in the curve when T_{fe} is approximately 3–4 nm. The appearance of turning point with an increasing Tfe attributes to the capacitance matching circumstance. Extremely thick FE layer leads to the capacitance mismatch effect because C_{FE} was derived by $2P_r/3\sqrt{3}E_cT_{fe}$ [31]. The perpendicular center-symmetry profile of the channel near the drain is gradually depleted over subthreshold region, which is modulated by the internal gate voltage. In addition, the threshold voltage requirement decreased at a certain range (T_{fe} = approximately 3–4 nm) due to the modulation of the perpendicular channel depletion. It can be concluded that V_T (extracted gate voltage at Id = 0.1 μA/μm) totally shifted towards the right in the coordinate system and its degree of dispersion became smaller. According to Figure .4 b, the V_{T1} (extracted gate voltage from the corresponding to the maximum slope) was positively correlated with V_T and V_{T1} increased rapidly because SS became steeper with an increase in the T_{fe}. Totally, the NC effect actually moderated the RDF-induced variations to the threshold voltage, and the performance of NC-JL-FinFET improved when compared to the regular JL-FinFET counterpart.

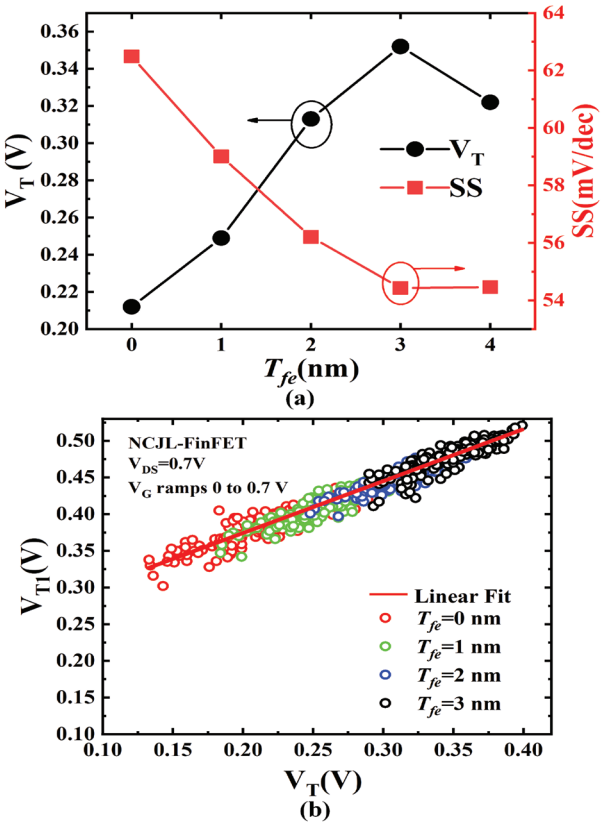

Figure 4: (a) Variation of threshold voltage with the thickness of ferroelectric layer and (b) The shift trend and dispersion between V_T (is extracted gate voltage at Id = 0.1 μA/μm) and V_{T1} (is extracted gate voltage from corresponding to the maximum slope) induced by the random doping in the 3D silicon-bulk channel of NCJL-FinFET.

Figures .5 (a)–(d) describe the expected normal value of the ON-state current and the simulation value of the

actual device model. Each simulation was performed at different particle concentrations, which was modeled via the actual manufacturing process in the TCAD tools flow. It is shown that the average ON-state current is increased from 12.4μA to 12.9μA. The average ON-state current is increased by 4.03% and the standard deviation of I_{on} (**δI_{on}**) is decreased to 7.08%. We could observe that the ON-state current fluctuation caused by the RDF upon the silicon-bulk channel was controlled by the NC effect. With an increase in the FE thickness, the expected values of the ON-state current became less than the actual values. This indicated that the ON-state performance improvement owed to the silicon-bulk channel and the drain/source region did not have the steep mutation particle species boundary. Compared to the JL-FinFET, its counterparts with the NC effect exhibited more immunity toward the impact of RDF in the saturation region.

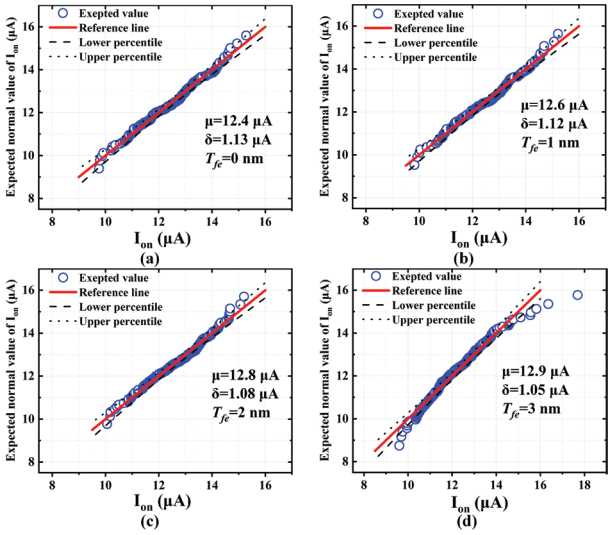

Figure 5: (a)–(d) Expected normal value of the ON-state current (I_{on}) and simulated value of the actual device model

The histogram of V_T distribution for each FE layer thickness at the drain biased voltage of 0.7 V is exhibited in Figures .6(a)–(d). The total dispersion of V_T presents a linear gaussian distribution. It can be observed that the fluctuation of V_T in the device with NC effect is to a small extent. As the FE thickness increases, the threshold voltage is least affected by RDF. The increase in the threshold voltage ensures the stability of the electrical characteristics of the device in the cut-off region because achieving full depletion would be easier if the gate control is enhanced.

In Table 2, it can be observed that mean value of SS among the random samples decreases slightly as the T_{fe} increases. Although the standard deviation of SS (δSS) is reduced, it did not exhibit a nonmonotonic trend all the time. The non-monotonic behavior of the impact of RDF on I_{on} originated from its strong attachment on the matching between FE capacitance and the internal silicon-bulk capacitance [32]. The OFF-state current (I_{off}) of the NCJL-FinFET gradually decreased by two orders of magnitude. Although the fluctuation in OFF-state leakage and threshold voltage were weakened compared to JL-FinFETs, the OFF-state current was actually more sensitive to the RDF in the silicon-bulk channel when compared to the IM transistors. Consequently, we found a monotonic suppression of I_{off} fluctuation with an increase in the T_{fe}

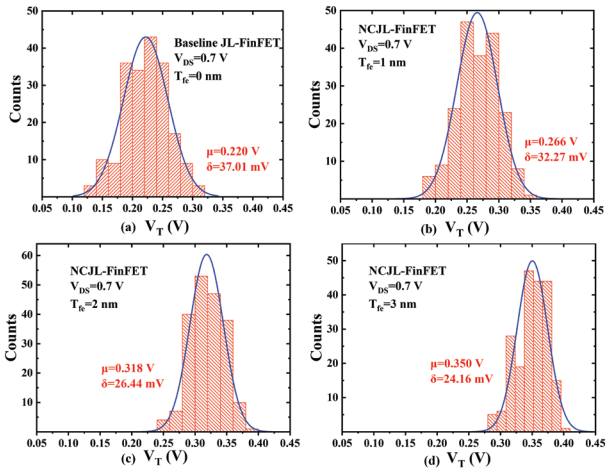

Figure .6: (a)–(d) Histogram of V_T distribution for each ferroelectric layer thickness (1, 2, 3 nm) and the baseline JL-FinFET at the biased drain voltage of 0.7 V

5 Conclusions

In this study, we investigated the impact of RDF on the conventional JL-FinFETs with NC effect. Through the

Table 2: Summary of statistical moments of the distribution of SS and Ioff at biased drain voltage of 0.7 V among the NC-JL-FinFET with different T_{fe}.

Tfe(nm)	SS(mV/dec)	δSS	δSS/SS	Ioff(A)	δIoff (A)	δIoff/Ioff
0	62.49	0.80626	1.29%	1.040e-10	1.881e-10	1.809
1	59.01	0.49307	0.84%	9.525e-12	1.670e-11	1.753
2	56.21	0.70523	1.23%	5.229e-13	8.308e-13	1.588
3	54.43	1.39964	2.57%	8.104e-14	1.154e-13	1.423

TCAD simulation, it can be concluded that the NCJL-FinFETs are more resilient toward the RDF-induced threshold voltage and OFF-state current variability. The significance of the resilience of the device counters against the total variability increases with respect to the increase in the thickness of the FE layer. Threshold voltage and subthreshold swing were not completely linear with the FE layer thickness related to the interaction between the capacitance mismatch effect and junctionless bulk-channel modulation. The leakage current of NCJL-FinFETs in the cut-off region were considerably smaller than that of JL-FinFETs. The increment of ON-state current was not evident in NCJL-FinFETs but also shows upward trend. The subthreshold swing decreased to 54.43 mV/dec, though no improvement was evident on this variation. On the whole, we have shown that there can be suppression of RDF-induced variability and performance enhancement of JL-FinFETs with NC effect, which also depends on the applied bias voltage and FE layer thickness.

6 Acknowledgments

This work is supported by Zhejiang Provincial Natural Science Foundation of China (Grant No. LY22F040005), and National Natural Science Foundation of China (Grant No. 62071160).

7 Conflict of interest

The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

8 References

1. W. Shockley, "The theory of p-n junctions in the semiconductors and p-n junction transistors." *Bell Labs Tech.J.*, vol. 28, no. 3, pp. 435–489, 1949. https://doi.org/10.1002/j.15387305.1949.tb03645.x
2. B. P. Algul, K. Uchida, "Optimization of Source/Drain Doping Level of Carbon Nanotube Field-Effect Transistors to Suppress OFF-State Leakage Current while Keeping Ideal ON-State Current." *Jpn.J.Appl.Phys.*, vol. 51, no. 6, pp. 823-843, 2012. https://doi.org/10.1143/JJAP.51.06FD27
3. C. Lee, A. Afzalian, N. D. Akhavan, R. Yan, L. Ferain and J. Colinge, "Junctionless multigate field-effect transistor." *Appl. Phys. Lett.*, Vol. 94, no. 5, pp. 053511, 2009. https://doi.org/10.1063/1.3079411
4. S. Migita, Y. Morita, M. Masahara, H. Ota, "Fabrication and Demonstration of 3-nm-Channel-Length Junctionless Field-Effect Transistors on Silicon-on-Insulator Substrates Using Anisotropic Wet Etching and Lateral Diffusion of Dopants." *Jpn. J. Appl. Phys.*, vol. 52, no. 4, pp. CA01-1-CA01-5, 2013. https://doi.org/10.7567/JJAP.52.04CA01
5. A. K. Jain, M. J. Kumar, "Sub-10 nm Scalability of Junctionless FETs using a Ground Plane in High-K BOX: A Simulation Study." *IEEE Access.*, vol. 8, no. 137, pp. 540-548, 2020. https://doi.org/10.1109/ACCESS.2020.3012579
6. J. Kim, J. W. Han, M. Meyyappan, "Reduction of Variability in Junctionless and Inversion-Mode FinFETs by Stringer Gate Structure." *IEEE Trans. Electron Devices.*, vol. 65, no. 2, pp. 470-475, 2018. https://doi.org/10.1109/TED.2017.2786238
7. C. Lee, A. N. Nazarov, I. Ferain, N. D. Akhavan, R. Yan, L. Ferain and J. Colinge, "Low subthreshold slope in junctionless multigate transistors." *Appl. Phys. Lett.*, vol. 96, no. 10, pp. 102106, 2010. https://doi.org/10.1063/1.3358131
8. K. S. Li, P. G. Chen, T. Y. Lai, C. G. Lin, C. Hu, "Sub-60mV-swing negative-capacitance FinFET without hysteresis." In *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015. https://doi.org/10.1109/IEDM.2015.7409760
9. T. Yu, W. Lü, Z. Zhao, P. Si and K. Zhang, "Effect of different capacitance matching on negative capacitance FDSOI transistors." *Microelectron. J*, vol. 98, pp. 104730, 2020. https://doi.org/10.1016/j.mejo.2020.104730
10. H. Ota, S. Migita, J. Hattori, K. Fukuda, A. Toriumi, "Material and device engineering in fully depleted silicon-on-insulator transistors to realize a steep subthreshold swing using negative capacitance." *Jpn.j.appl.phys.*, vol. 55, no. 8S2, 2016. https://doi.org/10.7567/JJAP.55.08PD01
11. N. M. Hossain, S. Quader, A. B. Siddik and M. I. B. Chowdhury, "TCAD based performance analysis of junctionless cylindrical double gate all around FET up to 5nm technology node." in *20th International Conference of Computer and Information Technology (ICCIT)*, 2017. https://doi.org/10.1109/iccitechn.2017.8281858
12. C. Shin, J. K. Kim, G. S. Kim, "Random Dopant Fluctuation-Induced Threshold Voltage Variation-Immune Ge FinFET with Metal-Interlayer-Semiconductor Source/Drain." *IEEE Trans. Electron Devices.*, vol. 63, no. 11, pp. 4167-4172, 2016. https://doi.org/ 10.1109/TED.2016.2606511
13. G. Leung, C. O. Chui, "Variability Impact of Random Dopant Fluctuation on Nanoscale Junctionless FinFETs." *IEEE Trans. Electron Devices.*, vol. 33, no. 6 pp. 767-769, 2012. https://doi.org/ 10.1109/LED.2012.2191931
14. G. Ghibaudo, "Evaluation of variability performance of junctionless and conventional Trigate transistors." *Solid-State Electron*, vol. 75 pp. 13-15, 2012. https://doi.org/ 10.1016/j.sse.2012.04.040

15. J. Kim, J. W. Han, M. Meyyappan, "Reduction of Variability in Junctionless and Inversion-Mode FinFETs by Stringer Gate Structure." *IEEE Trans. Electron Devices,* vol. 65, no. 2, pp. 470-475, 2018. https://doi.org/10.1109/TED.2017.2786238
16. A. K. Jain, A. Singha. "Sub-10-nm Scalability of Emerging Nanowire Junctionless FETs Using a Schottky Metallic Core" *IEEE J. Electron Devices Mat.*, vol. 50, no. 3, pp. 1110-1117, 2021. https://doi.org/10.1007/s11664-020-08638-1.
17. A. K. Jain, J. Singh, M. J. Kumar. "Investigation of the scalability of emerging nanotube junctionless fets using an intrinsic pocket" *IEEE J. Electron Devices Soc.,* vol.7, no.2 pp.888-896, 2019 https://doi.org/10.1109/JEDS.2019.2935319
18. L. Y. Chen, Y. F. Hsieh, K. H. Kao, "Undoped and Doped Junctionless FETs: Source/Drain Contacts and Immunity to Random Dopant Fluctuation." *IEEE Electron Device Lett.*, vol. 38, no. 6, pp.708-711, 2017. https://doi.org/10.1109/LED.2017.2690993
19. K. Zhang, W. Lü, P. Si, Z. Zhao T. Yu, "Performance improvement of timing and power variations due to random dopant fluctuation in negative-capacitance CMOS inverters." *IET Circ. Devices Syst.,* vol. 14, no. 6, pp. 908-914, 2020. https://doi.org/10.1049/iet-cds.2020.0101
20. S. Wang, G. Leung, A. Pan, C. O. Chui, "Evaluation of Digital Circuit-Level Variability in Inversion-Mode and Junctionless FinFET Technologies." *IEEE Trans. Electron Devices,* vol. 60, no. 7, pp. 2186-2193, 2013. https://doi.org/10.1109/TED.2013.2264937
21. S. Salahuddin, S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices." *Nano Lett.*, Vol. 8, no. 2, pp. 405-410, 2008. https://doi.org/10.1021/nl071804g
22. Z. Krivokapic, U. Rana, R. Galatage, A. Razavieh, S. Banna, "14nm Ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications." in *IEEE International Electron Devices Meeting (IEDM)* 2017. https://doi.org/10.1109/IEDM.2017.8268393
23. Daewoong, Kwon, Korok, "Improved Subthreshold Swing and Short Channel Effect in FDSOI n-Channel Negative Capacitance Field Effect Transistors.", *IEEE Electron Device Lett.* Vol. 39, no. 2, pp. 300 -303, 2017. https://doi.org/10.1109/LED.2017.2787063
24. C. Jiang, R. Liang, W. Jing, J. Xu, "Analytical drain current model for long-channel double-gate negative capacitance junctionless transistors using Landau theory." In *IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC'16),* 2016. https://doi.org/10.1109/EDSSC.2016.7785204.
25. M. H. Park, Y. H. Lee, H. J. Kim, Y. J. Kim, T. Moon, K. D. Kim, J. Müller, A. Kersch, U. Schroeder, T. Mikolajick and C. S. Hwang, "Ferroelectricity and Antiferroelectricity of Doped Thin HfO2-Based Films." *Adv. Mater*, vol. 27, no. 11, pp. 1811-1831, 2015. https://doi.org/10.1002/chin.201521244
26. C. W. Yeung, A. I. Khan, S. Salahuddin and C. Hu, "Device design considerations for ultra-thin body non-hysteretic negative capacitance FETs." in *Third Berkeley Symposium on Energy Efficient Electronic Systems (E3S),* 2013. https://doi.org/10.1109/E3S.2013.6705876
27. N. Sano, K. Matsuzawa, M. Mukai, "On discrete random dopant modeling in drift-diffusion simulations: physical meaning of 'atomistic' dopants." *Microelectron. Reliab.,* vol. 43, no.2 pp. 189-199, 2002. https://doi.org/10.1016/S0026-2714(01)00138-X
28. Sentaurus Device User Guide; Synopsys, Inc.: Mountain View, CA, USA, 2018
29. K. Nayak, S. Agarwal, M. Bajaj, K. V. R. M. Murali, V. R. Rao, "Random Dopant Fluctuation Induced Variability in Undoped Channel Si Gate all Around Nanowire n-MOSFET" *IEEE Trans. Electron Devices,* vol. 62, no. 2, pp.685-688, 2015. https://doi.org/10.1109/TED.2014.2383352
30. H. Carrillo-Nunez, M. M. Mirza, D. J. Paul, D. A. Maclaren, V. P. Georgiev, "Impact of Randomly Distributed Dopants on Ω-Gate Junctionless Silicon Nanowire Transistors" *IEEE Trans. Electron Devices,* vol. 65, no. 5, pp. 1692-1698, 2018. https://doi.org/10.1109/TED.2018.2817919
31. C. I. Lin, K. A. Islam, S. Salahuddin and C. Hu, "Effects of the Variation of Ferroelectric properties on Negative Capacitance FET Characteristics" *IEEE Trans. Electron Devices,* vol.63, no. 5, pp. 2197-2199, 2016. https://doi.org/10.1109/TED.2016.2514783
32. M. Kao, Y. Lin, H. Agarwal, Y. Liao, P. Kushwaha, A. Dasgupta, S. Salahuddin and C. Hu, "Optimization of NCFET by Matching Dielectric and Ferroelectric Nonuniformly Along the Channel." *IEEE Electron Device Lett*, vol. 40, no. 5, pp. 822-825, 2019. https://doi.org/10.1109/LED.2019.2906314

Arrived: 24. 05. 2021
Accepted: 12. 11. 2021