Original scientific paper
https://doi.org/10.33180/InfMIDEM2022.201

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 52, No. 2(2022), 71 – 82

Five-Level Transformerless Common Ground Type Inverter with Reduced Device Count

Gopinath Narayanan Pandurengan[1], Vijayakumar Krishnasamy[1], Jagabar Sathik Mohamed Ali[2], Dhafer Almakhles[2]

[1]Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology University, Kattankulathur, Tamil Nadu, India
[2]Energy Lab, College of Engineering, Prince Sultan University, Riyadh, Saudi Arabia

Abstract: In recent days, the transformerless grid-connected PV inverter is paid more attention due to its compactness and high efficiency with low cost. This paper presents a new five-level transformerless switched capacitor type inverter with a reduced number of power components. The proposed topology has a lower number of power components with a common ground connection between the negative terminal of the input side and load that eliminates the leakage current. The switched capacitors do not require any sensors for their balancing. The different modes of operation and control of the PWM technique are discussed. The proposed topology is compared with recent transformerless inverters, and the advantages of the proposed topology are highlighted. The simulation and experimental results are presented. The prototype hardware setup is built for 1.2 kW and has the simulated maximum efficiency of 96.4%. The performance of the proposed topology is measured by applying various load and modulation index variations.

Keywords: Common ground; Leakage current; Multilevel inverter; Transformerless inverter; Switched capacitor

Petstopenjski pretvornik brez transformatorja s skupno ozemljitvijo in manjšim številom naprav

Izvleček: V zadnjih dneh se zaradi kompaktnosti in visoke učinkovitosti ob nizkih stroških več pozornosti namenja breztransformatorskim PV pretvornikom, ki so priključeni na omrežje. V tem članku je predstavljen nov petstopenjski breztransformatorski razsmernik s stikalnim kondenzatorjem z zmanjšanim številom močnostnih komponent. Predlagana topologija ima manjše število močnostnih komponent s skupno ozemljitveno povezavo med negativno sponko vhodne strani in bremenom, ki odpravlja uhajalni tok. Preklopni kondenzatorji ne potrebujejo senzorjev za uravnoteženje. Obravnavani so različni načini delovanja in krmilne tehnike PWM. Predlagana topologija je primerjana z novejšimi breztransformatorskimi pretvorniki, poudarjene pa so tudi prednosti predlagane topologije. Predstavljeni so simulacijski in eksperimentalni rezultati. Prototipna strojna oprema je izdelana za 1,2 kW in ima simulirano največjo učinkovitost 96,4 %. Učinkovitost predlagane topologije je izmerjena z različnimi spremembami obremenitve in modulacijskega indeksa.

Ključne besede: skupna zemlja; uhajalni tok; večnivojski razsmernik; breztransformatorski razsmernik; preklopni kondenzator

** Corresponding Author's e-mail: mjsathik@ieee.org*

1 Introduction

The PV system is a more promising renewable energy source because of no greenhouse gases, pollution-free, clean, return on investment, and emission-free. Various advantages like reliability, the noiseless operation makes the photovoltaic system a more attractive and promising renewable energy source. Such a photovoltaic system with grid integration can be done generally through galvanic isolation, which is transformer-based and non-galvanic isolation which is a transformerless

How to cite:
G N.. Pandurengan et al., "Five-Level Transformerless Common Ground Type Inverter with Reduced Device Count", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 52, No. 2(2022), pp. 71–82

based method [1]. The high-frequency transformer on the DC side and line transformers on the AC side ensures safer operation in the existing system. But the use of transformer leads to decrease in efficiency, more weight, high cost and power losses, need regular maintenance and bulky size. To overcome the drawbacks of transformer-based galvanic isolation, transformerless inverter topologies are developed. The transformerless inverters offer high efficiency, compactness, and low leakage current. However, the power quality concern, output voltage distortion and safety due to the leakage current, isolation capabilities are the main predicament in grid-connected transformerless inverter-based PV systems. Many types of transformerless inverters have been developed to reduce the leakage current [2]. The MLI inverter proposed in [3] has the ability of self-voltage balancing and boosting for the grid-connected renewable energy system. The source of leakage current is a common-mode voltage which can be minimized by proper selection of switching sequence. Parasitic capacitance i.e., stray capacitance is usually appearing between photovoltaic panels negative terminal and neutral side of the grid. In a non-galvanic i.e., transformerless inverters a direct ground current path is developed between the PV and grid grounds. The variable high-frequency common mode voltage (CMV) of the inverter where it can be clamped between the null of ac grid and the parasitic capacitor of the PV arrays negative terminal excites the resonant circuit formed by parasitic capacitor and inverter filer inductor, which produces leakage current. By connecting negative terminal of PV side and neutral of grid side, the CMV will be cancelled out since the parasitic capacitance is clamped to ground potential. Hence, the leakage current can be eliminated [5]. The CMV can be maintained constantly through PWM controlling techniques, decoupling the photovoltaic and grid to reduce the leakage current. There are some methods to mitigate the leakage current.

Suppressing the leakage current problem is possible with the grid neutral terminal's direct connection with the negative PV terminal. This direct connection of grid neutral and PV negative terminal called common ground type transformerless inverters results in zero leakage current. Many topologies have been proposed to minimize the leakage current value. Still, each having has disadvantages like the higher switch count, the high voltage stress on the capacitor and the larger size of the capacitor [6]. The topology developed [7] has four topological variants with high dc-bus utilization and constant total common-mode voltage. By providing the DC and AC decoupling in inverter circuit will reduce the leakage current. A new DC decoupling inverter topology with less power components is proposed to reduce leakage current [9]. However, the complete elimination of leakage current is not achieved by decoupling methods due to its dc bus utilization limit. A switched-capacitor inverter with a common ground type is presented in [11]. The switched capacitor acts as a virtual dc-link, and this is charging in the positive half cycle and discharging at the negative half cycle. A simple peak current controller controls the output current. A common ground type topology with flying capacitor leg plus a half-bridge cell is presented in [12], gives superior performance in terms of harmonic distortion, thus allowing filter reduction. The multilevel transformerless half-bridge topology is presented in [13]. This topology can inject reactive power into the grid, thereby making it low voltage ride-through capability LVRT.

A virtual dc bus concept with feedforward space vector modulation technique is presented in [14]. The modulation strategy decouples the output variables from voltage capacitor oscillations, thus providing a low output current THD, and this is independent of the size of dc capacitors. Asymmetrical T-type common ground transformerless inverter is proposed in [15]. The EMI filter design and the modulation scheme allow the reduction of leakage current with high efficiency. Various methods have been introduced to minimize the leakage current in transformerless inverters. The common ground transformerless inverter topologies are efficiently eliminating the leakage current [5], [11], [14]. Although common ground transformerless inverters have numerous benefits, they also have certain drawbacks, such as the requirement for additional protection circuits due to high inrush current and the discontinuous nature of input current. This article proposes a new six switch one diode five-level 6S-1D-5L transformerless inverter topology with a common ground. The

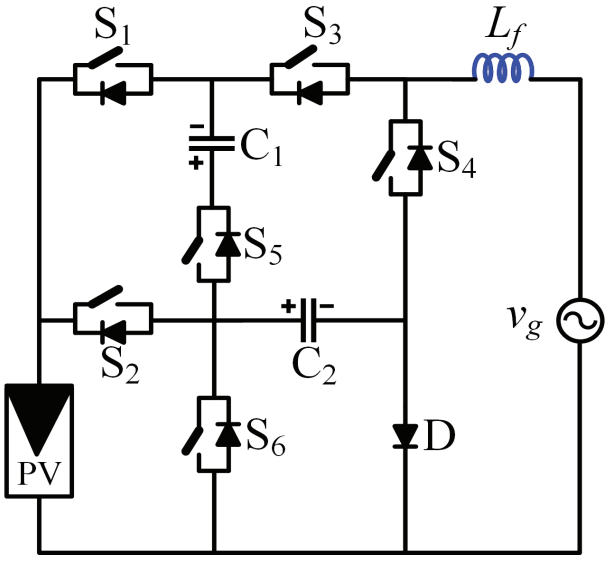


Figure 1: Circuit diagram of proposed 6S-1D-5L Topology.

proposed topology has significant advantages like low capacitor voltage stress and low power device.

2 Description and its operating principle

2.1 Description of 6S-1D-5L inverter topology

The power circuit of the proposed 5L-Inverter topology is shown in Fig. 1. The proposed topology comprises six switches (S_1, S_2, S_3, S_4, S_5 and S_6), two capacitors C_1 & C_2 and one diode D for five-level voltage output. The voltage rating of the capacitors C_1 and C_2 are $0.5v_{in}$ and $v_{in,}$ respectively The C_1 and C_2 are charging in the positive half cycle and discharging in the negative half cycle. The negative terminal of the load is directly connected to the dc source negative terminal, which is called common ground.

A few highlights of the new 6S-1D-5L inverter are,

- The proposed topology has few power components.
- The capacitors voltages are self-balanced and do ot require any additional sensors.
- The number of ON-state switches is less.
- Maximum voltage stress across the switch is equal to $1.5V_{in}$.
- Total capacitor voltage stress is reduced.
- No leakage currents.

2.2 Description of 6S-1D-5L inverter topology

Different switching Levels (Level 1 to Level 5) that generate five levels of the output voltage waveform of the proposed inverter and the switching sequence are listed in Table 1. The analysis of voltage stress and current stress of all the switches is summarized and shown in Table 2 and Table 3. The switch S_1 blocks the sum of the voltage across the C_1 and dc source voltage, and this S_1 has to withstand the maximum voltage, i.e., 1.5 V_{in}. The maximum current flow through the switch S_3. During the positive half cycle, the C_2 capacitor is connected in parallel to dc source through switch S_3, and it draws more charging current.

Table 1: Operating levels of the proposed topology.

Levels	Conducting Switches						FCs Status	
	S_1	S_2	S_3	S_4	S_5	S_6	C_1	C_2
V_{in}	1	1	1	0	0	0	-	↑
0.5 V_{in}	0	1	1	0	1	0	↑	↑
0	0	1	0	1	0	0	-	↑
-0.5 V_{in}	0	0	1	0	1	1	↓	-
$-V_{in}$	0	0	0	1	0	1	-	↓

Table 2: Voltage stress of switches

Levels	Switches					
	S_1	S_2	S_3	S_4	S_5	S_6
V_{in}	0	0	0	1	0.5	1
0.5 V_{in}	0.5	0	0	0.5	0	1
0	0	0	0.5	0	0	1
-0.5 V_{in}	1.5	1	0	0.5	0	0
$-V_{in}$	1.5	1	1	0	0.5	0

The blue line and red line in Fig. 2 indicate the current flow from source to load and vice versa.

Level 1: ($V_0 = V_{in}$): During this level of operation, the switches S_1, S_2 and S_3 are switched ON. The capacitor C_2 is charged during this output voltage level. The respective level is shown in Fig. 2a.

Table 3: Current stress of switches

Levels	Switches					
	S_1	S_2	S_3	S_4	S_5	S_6
V_{in}	I_{L1}	I_L- I_{L1}	I_{L1}	0	0	0
0.5 V_{in}	0	I_L	I_{L2}	0	I_{L2}	0
0	0	0	0	I_{L3}	0	0
-0.5 V_{in}	0	0	I_{L4}	0	I_{L4}	I_{L4}
$-V_{in}$	0	0	0	I_{L5}	0	I_{L5}

Level 2 :($V_0 = 0.5V_{in)}$: The switches S_2, S_3 and S_5 are switched ON to generate the output voltage of $V_0 = 0.5V_{in.}$ The respective level is shown in Fig. 2b. In this operating level, the capacitors C_1 and C_2 are charged to $0.5V_{in}$ and V_{in}.

Level 3:($V_{0=}$ 0): The switches S2, and S4 are ON. The output voltage in this level is V0 = 0. The respective level is shown in Fig. 2c.

Level 4: ($V_0 = -0.5V_{in)}$ The switches S_3, S_5 and S_6 are switched ON to generate the output voltage of $V_0 = -0.5V_{in.}$ The respective level is shown in Fig. 2d. In this operating level, the capacitor C_1 is discharged.

Level 5: ($V_0 = -V_{in}$): The switches S_4 and S_6 are switched ON to generate the output voltage of $V_0 = -V_{in}$. The respective level is shown in Fig. 2e. In this operating level, the capacitor C_2 is discharged.

3 PWM Modulation technique

Several modulation schemes have been developed to generate stepped output voltage levels in MLIs. The

pulse width modulation technique is classified as a low-frequency switching scheme and a high-frequency switching scheme based on the switching frequency. The multi-carrier level-shifted pulse width modulation technique is one of the familiar modulation methods. For the proposed 6S-1D-5L inverter topology, alternate phase opposition disposition pulse width modulation (APOD-PWM) has been employed, which is shown in Fig. 3a. The carrier signals V_c are compared with a sinusoidal reference signal V_{ref} to generate gate signals. For the proposed inverter topology, the alternate phase opposition disposition pulse width modulation employs four carrier signals, two on the positive side and two on the negative side, compared with the sinusoidal reference signal V_{ref}. The logic scheme to generate the gate

pulses for switches are shown in Fig. 3b. The modulation index is an important factor that supports to control of the load voltage, and it is defined as:

$$\mathrm{MI} = \frac{\mathrm{V_{ref}}}{2 \times \mathrm{V_c}}, \mathrm{V_o} = \mathrm{M} \times \mathrm{Vin} \tag{1}$$

The logical expression for the gating signals is expressed as:

$$S_1 = A_3 \tag{2}$$

$$S_2 = A_1 + A_2 \tag{3}$$

$$S_3 = A_2 + A_4 A_5\,' \tag{4}$$

$$S_4 = A_1 + A_5 \tag{5}$$

$$S_5 = A_4 \tag{6}$$

$$\mathrm{S_6} = \mathrm{A_2 A_3\,' + A_4 A_5\,'} \tag{7}$$

4 Power loss analysis

The equivalent circuit of the proposed 6S-1D-5L topology is shown in Fig. 4a. The equivalent circuit is derived by replacing the switches and capacitors with their equivalent internal resistances. In the equivalent circuit R_{sl}, R_{esr}, R_L and R_d indicate the internal resistance of individual switch, the resistance of the capacitor, the resistance of the load, and the diode resistance.

4.1 Conduction loss

The conduction losses are calculated by multiplying the on-state voltage drop of the switch and the conduction current. The total conduction losses have been calculated with pure resistive load at a steady state. All

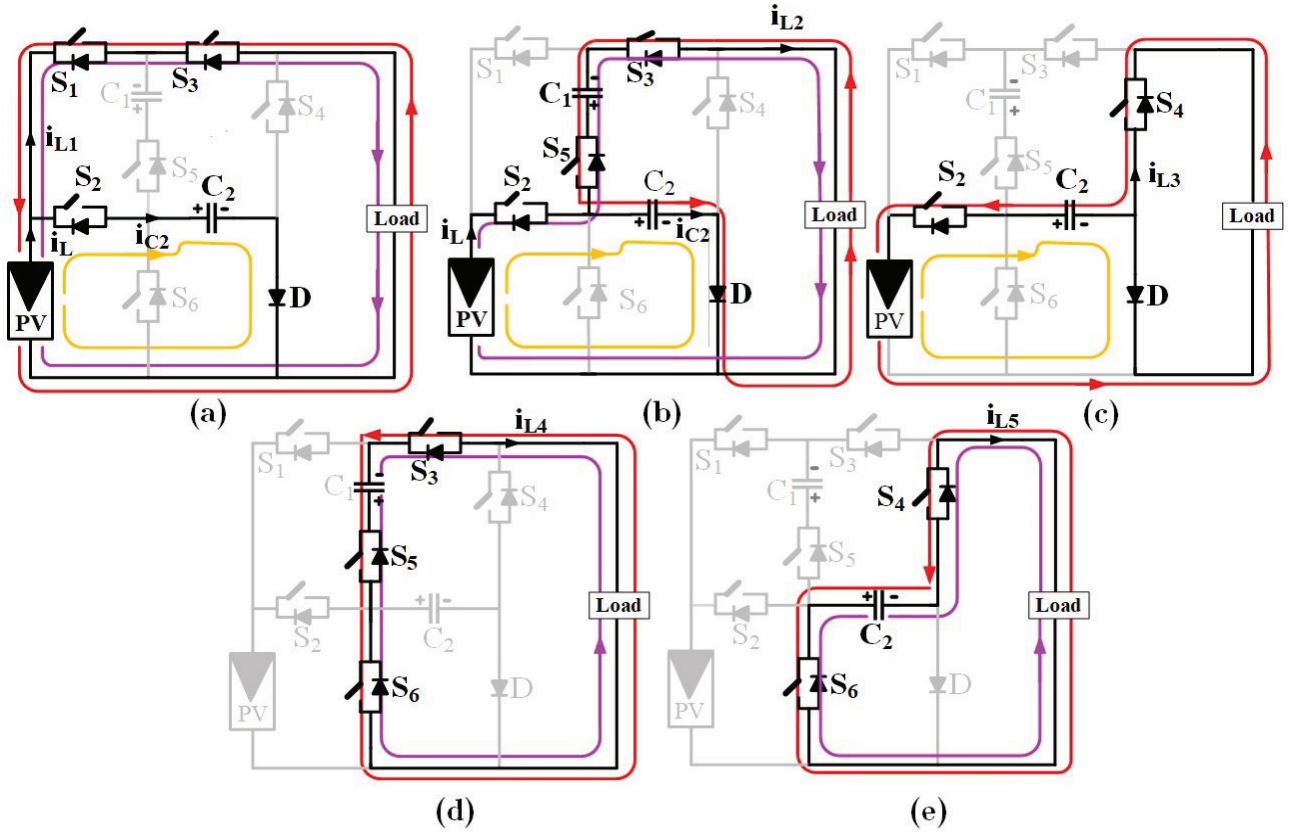
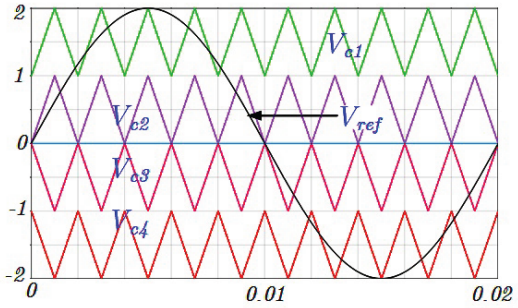


Figure 2: Switching levels of proposed inverter topology.

(a)



(b)

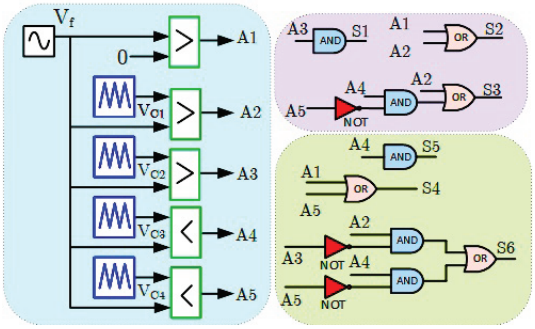


Figure 3: Modulation Technique (a) APOD PWM methods and (b) Logic Diagram

working levels of the proposed topology are considered and its equivalent circuit is shown in Fig. 4(b-e) to calculate the maximum conduction loss. Pure resistive loading condition is considered because there should not exist any auxiliary current path between load current and output voltage to facilitate the charging of capacitors. Therefore, the resistive loading condition is considered the worst condition for calculating losses in switched capacitor-based multi-level inverters [8].
From equivalent circuit of Fig. 4b during $V_0=V_{in}$:

$$I_{dc} = I_{charging} + I_{L1} \tag{8}$$

Where I_{L1} is the load current during $V_0=V_{in}$.

From equivalent circuit of Fig. 4c during $V_0=0.5V_{in}$:

$$I_{dc} = I_{charging} + I_{L2} \tag{9}$$

Where I_{L2} is the load current during $V_0=V_{in}$.

From equivalent circuit of Fig. 4d:

$$I_{dischargingC1} = \frac{V_{C1}}{R_{esr} + 3R_{sr}} \tag{10}$$

From equivalent circuit of Fig. 4e:

$$I_{dischargingC2} = \frac{V_{C2}}{R_{esr} + 2R_{sr}} \tag{11}$$

By applying Kirchhoff's voltage law and Kirchhoff's current law to equivalent circuits of Fig. 4(b-e), the instantaneous value of conduction losses can be calculated using as follows:

$$P_{C1} = 2R_{sr}\left(I_{L1}\right)^2 + (R_{sr} + R_{esr})\left(I_{charging}\right)^2 \tag{12}$$

$$P_{C2} = R_{sr}\left(I_{dc}\right)^2 + (R_{esr} + R_d)\left(I_{charging}\right)^2 + (2R_{sr} + R_{esr})\left(I_{L2}\right)^2 \tag{13}$$

$$P_{C3} = (R_{esr} + 3R_{sr})\left(I_{discharging}\right)^2 \tag{14}$$

Where $I_{discharging}$ represents the capacitor C_1 discharging current.

$$P_{C4} = (R_{esr} + 2R_{sr})\left(I_{discharging}\right)^2 \tag{15}$$

Where $I_{discharging}$ represents the capacitor C_2 discharging current.

The average conduction loss for one complete cycle of output voltage waveform is calculated by using related time interval. From Fig. 5, the time interval for V_{in}, $0.5V_{in}$, $-0.5V_{in}$ and $-V_{in}$ is (t_3-t_2), (t_2-t_1), (t_7-t_6), and(t_8-t_7). By using the calculated instantaneous conduction loss, the average value of conduction loss is calculated as:

$$P_{C1}' = \frac{2}{T_{f0}} P_{C1}\left(t_3 - t_2\right); P'_{C2} = \frac{2}{T_{f0}} P_{C2}\left(t_2 - t_1\right)$$

$$P_{C3}' = \frac{2}{T_{f0}} P_{C3}\left(t_7 - t_6\right); P'_{C4} = \frac{2}{T_{f0}} P_{C4}\left(t_8 - t_7\right)$$

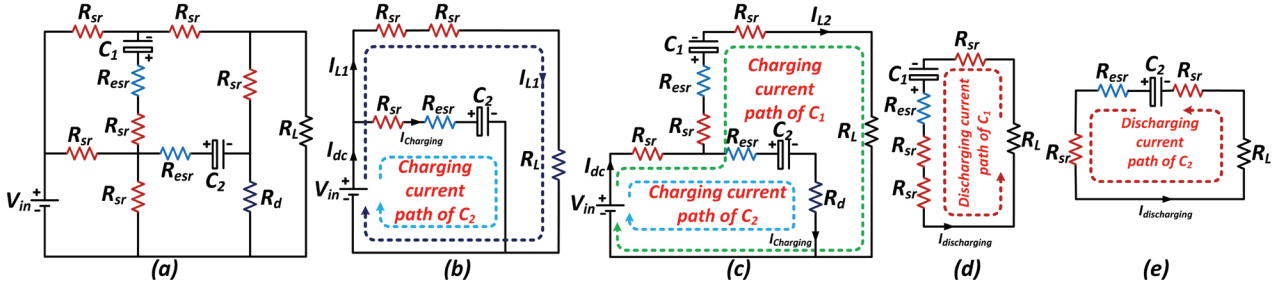


Figure 4: Equivalent circuit (a) Proposed circuit (b) $V_o = V_{in}$ (c) $V_o = 0.5V_{in}$ (d) $V_o = -0.5V_{in}$ (e) $V_o = -V_{in}$

The total conduction loss can be calculated using (16):

$$P_C = P_{C1}^{'} + P_{C2}^{'} + P_{C3}^{'} + P_{C4}^{'} \quad (16)$$

P_{C1}, P_{C2}, P_{C3}, and P_{C4} are instantaneous values of conduction losses and P'_{C1}, P'_{C2}, P'_{C3}, P'_{C4} are average values *of* conduction losses over one complete cycle.

4.2 Switching loss

The switching of semiconducting devices during turn-on and turn-off transitions are termed switching losses. The switching losses can be obtained by integrating the voltage and the current on the particular switching period. Here the switching losses can be calculated using linear polynomial approximation.

The energy dissipated during turn-on period of a semiconductor switch is:

$$E_{on} = \int_0^{T_{on}} V(t) \times I(t)\, dt \quad (17)$$

$$= \int_0^{T_{on}} \left(V_{swon} \times \frac{T}{T_{on}} \right) \times \left(\frac{-I_1 (T - T_{on})}{T_{on}} \right) dt = \frac{V_{swon} \times I_1 \times T_{on}}{6} \quad (18)$$

Where V_{swon} is the on-state voltage on the switch, I_1 is the current through the switch after turning on, T_{on} is the turn-on time of the semiconductor switch.

The energy dissipated during turn off period of a semiconductor switch is:

$$E_{off} = \int_0^{T_{off}} V(t) \times I(t) dt \quad (19)$$

$$= \int_0^{T_{off}} \left(V_{swoff} \times \frac{T}{T_{off}} \right) \times \left(\frac{-I_1 (T - T_{off})}{T_{off}} \right) dt = \frac{V_{swoff} \times I_2 \times T_{off}}{6} \quad (20)$$

Using fundamental frequency switching method, the total switching loss is estimated using (21):

$$P_{switch} = f \times \left(N_{on} E_{on} + N_{off} E_{off} \right) \quad (21)$$

Where , N_{on} is the number of turn ON switches, and N_{off} is the number of turns OFF switches during one fundamental cycle.

4.3 Capacitor Ripple Loss

The difference between capacitor voltage and the input voltage results in capacitor ripple losses [8], [10]. The capacitor ripple voltage is calculated using the equation (22):

$$\Delta V_{c_i} = \frac{1}{C_i} \int i(t)\, dt \quad (22)$$

Where C_i is the capacitance value, *i(t)* is the current flowing through the capacitors. Hence, from the longest discharge duration capacitors, the capacitor ripple loss over a cycle is calculated as:

$$P_{ripple} = \frac{f}{2} \times C \times (\Delta V_C)^2 \quad (23)$$

$$\Delta V_{C1} = \frac{I_p}{C_1 \times f_{sw}} \quad (24)$$

$$\Delta V_{C2} = \frac{I_{pm}}{\pi \times f \times C_2} \left[\cos\left(\frac{\pi}{3} - \theta \right) - \sin\theta \right] \quad (25)$$

4.4 Inductor Loss

In inductors, the total losses are depending on two losses a) copper loss and b) iron losses. For the output filter inductor, the loses are expressed as [14]:

$$P_{cu} = (i_L)^2 R_L \quad (26)$$

$$P_{core} = k f^{\alpha} V_{cl} B^{\lambda} \quad (27)$$

Where R_L is the inductor's series resistance, f is the frequency, V_{cl} is the core volume, and B is the flux density. K, α, λ are constants which depends on the core material. The inductor loss is expressed as:

$$P_L = P_{cu} + P_{core} \quad (28)$$

The total loss is estimated as follows (26):

$$P_{Loss} = P_C + P_{switch} + P_{ripple} + P_L \quad (29)$$

The overall efficiency is estimated as follows (27):

$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}} \tag{30}$$

The proposed topology's efficiency without the output filter inductor is 96%. When the output filter inductor is considered, the efficiency is reduced to 95.43%.

5 Design considerations of passive elements

The voltage balancing of passive elements is important in switched-capacitor inverter topologies. The proposed new topology formed using flying capacitor C_1 and switched capacitor C_2. The capacitors C_1 and C_2 are charged to half of the input voltage ($0.5V_{in}$) and the full (V_{in}) input voltage. Since the capacitor C_2 is charged and discharged using a series-parallel technique, it does not require any separate voltage balancing method. Unlike C_2, capacitor C_1 is charged and discharged during ($+0.5V_{in}$) and ($-0.5V_{in}$) output voltage waveform. The capacitor C_1 currents only during $\pm 0.5V_{in,}$ and the ner charge of capacitor C_1 over a fundamental period is expressed as [16]:

$$Q_{C1,net} = \left(\frac{2V_{C1} - V_{in}}{Z}\right) T \tag{31}$$

Under steady-state conditions the voltage across C_1 will equal $0.5V_{in}$. From (28), the total charge of the capacitor C_1 will be zero in a given fundamental cycle, and it is achieved without any supplementary voltage balancing methods. Regarding the sizing of the capacitor C_1, the required parameters are, allowable voltage ripple ΔV_{C1}, switching frequency f_{sw}, peak value of load current. From this C_1 is calculated as [18]:

$$C_1 = \frac{I_p}{\Delta V_{C1} \times f_{sw}} \tag{32}$$

As shown in Fig. 5, the longest discharge period of C_2 occurs from t_3 to t_2.Where t1, t2, t3 are $T_{fo}/12$,$T_{fo}/6$, $T_{fo}/4$ which are expressed from fundamental time period $T_{fo.}$ At R-load during steady state operation the load current flow is given as:

$$I_L(t) = \begin{cases} \frac{V_{in}}{2} & ; \frac{T_{fo}}{12} \le T \le \frac{T_{fo}}{6} \\ V_{in} & ; \frac{T_{fo}}{6} \le \beta \le \frac{T_{fo}}{4} \end{cases} \tag{33}$$

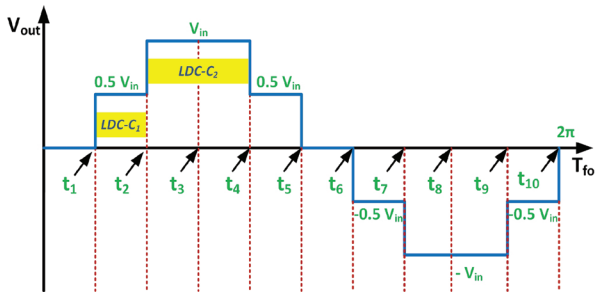


Figure 5: Typical 5 level waveform

The charge of capacitor C_2 during its longest discharging period is expressed as:

$$Q_{C2} = 2 \times \int_{\frac{T_{fo}}{6}}^{\frac{T_{fo}}{4}} I_L(t)\, dt \tag{34}$$

By substituting the equation (33) in (34),

$$Q_{C2} = 2 \times \int_{\frac{T_{fo}}{6}}^{\frac{T_{fo}}{4}} \frac{V_{in}}{R_L}\, dt \tag{35}$$

From the above equation the optimum value of capacitor C_2 is calculated as:

$$C_{2,mx} \ge \frac{\pi}{3 \times R_L \times k \times \omega} \tag{36}$$

Similarly, for resistive-inductive loading the load current is expressed as:

$$I_L = I_{pm} \sin(\omega t - \theta) \tag{37}$$

Using (37) in (34) the capacitance of capacitors C_2 is written as:

$$Q_{C2} = 2 \times \int_{\frac{T_{fo}}{6}}^{\frac{T_{fo}}{4}} I_{pm} \sin(\omega t - \theta)\, dt \tag{38}$$

$$Q_{C2} = 2 \times I_{pm} \int_{\frac{T_{fo}}{6}}^{\frac{T_{fo}}{4}} (\sin \omega t \times \cos \theta - \cos \omega t \times \sin \theta)\, dt$$

$$Q_{C2} = 2 \times I_{pm} \times \left[\cos\left(\frac{\omega T_{fo}}{6} - \theta \right) - \cos\left(\frac{\omega T_{fo}}{4} - \theta \right) \right] \quad (39)$$

$$Q_{C2} = 2 \times I_{pm} \times \left[\cos\left(\frac{\pi}{3} - \theta \right) - \sin \theta \right]$$

From (39), a maximum value of capacitances for C_2 can be calculated as:

$$C_{2,mx} = \frac{2I_{pm}}{\omega \times k \times V_{in}} \times \left[\cos\left(\frac{\pi}{3} - \theta \right) - \sin \theta \right] \quad (40)$$

Where I_{pm} is maximum load current, k is the ripple factor. Fig. 6(a-c) shows the graph between optimum value of capacitance with different load values, different frequencies, and different phase angles. The ripple factor of k=0.01, 0.05 and 0.1 and ω=100π has been taken for calculating the optimum value of capacitances.

Fig. 6b shows the graph between optimum value of capacitance C_2 and frequency. This graph is plotted by considering the load resistance of 200 Ω. Fig. 6c is the graph plotted for different phase angles of θ with allowable voltage ripple of 0.05 and 0.1, I_{pm} = 8 A, V_{in} = 400V, f =50 Hz and ω = 100π at fundamental frequency. It is seen from the Fig. 6c that, as the phase angle increases the capacitance decreases.

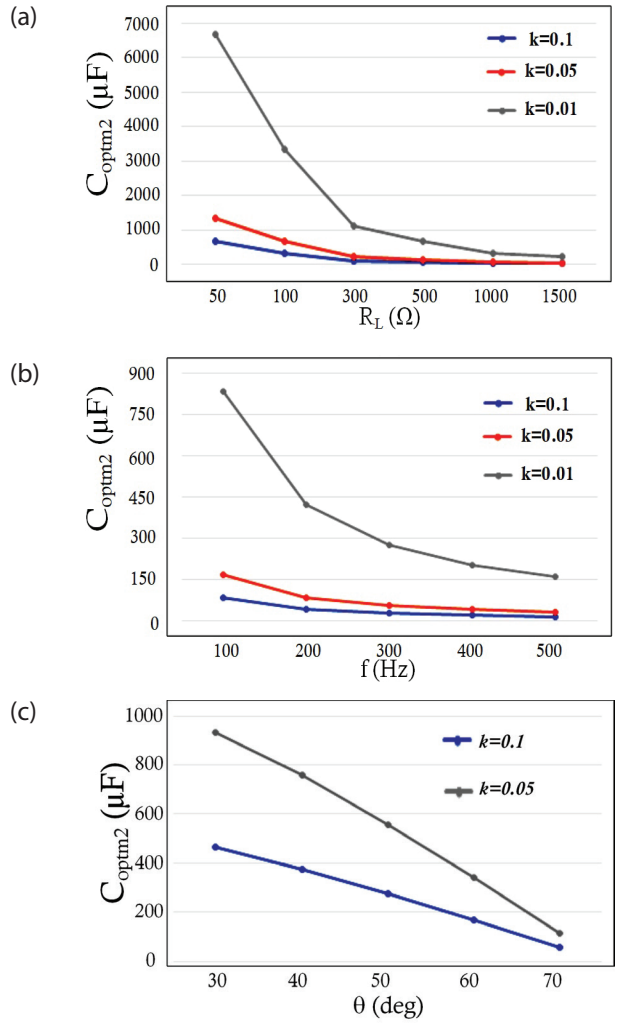


Figure 6: Variation of optimal capacitance versus (a) R_L (resistive load) (b) frequency (Hz) (c) phase angle θ

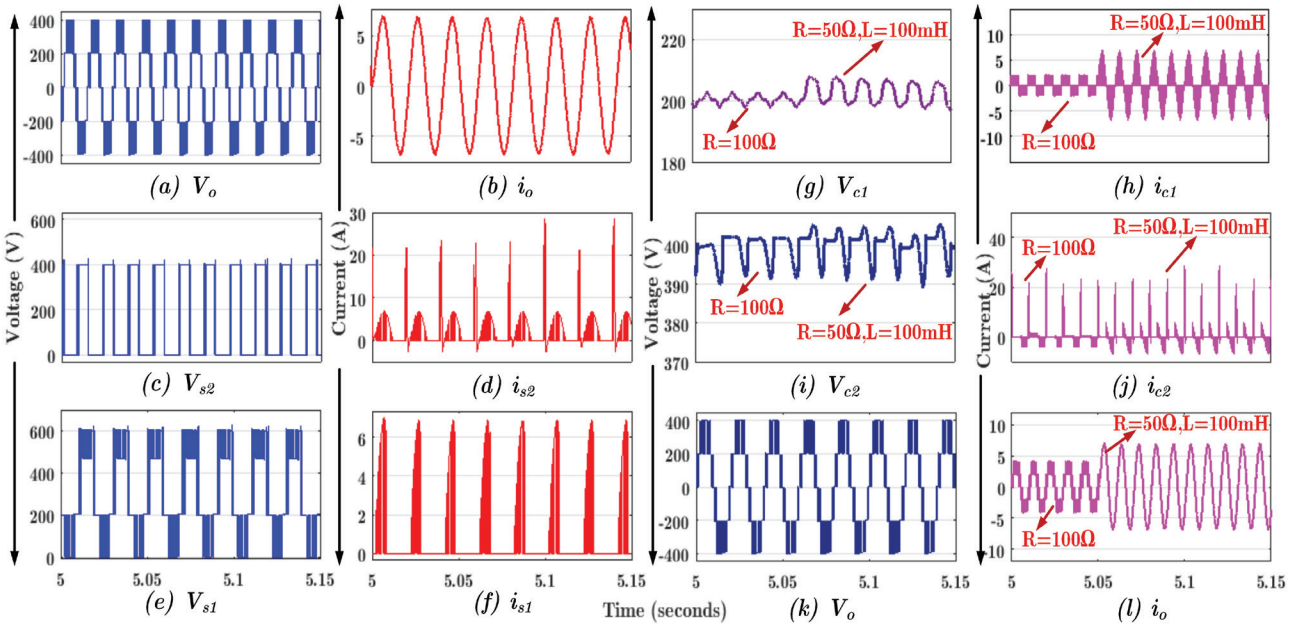


Figure 7: Simulation outputs of proposed 6S-1D-5L inverter topology for 1.2 kW

6 Simulation and experimental results

6.1 Simulation results

The operation of the proposed 6S-1D-5L inverter topology is examined for generating five-level output voltage using MATLAB/Simulink environment. The parameters used for the simulation and values of components used in the proposed inverter topology is tabulated in Table 4. While using alternate high-frequency phase opposition disposition pulse width modulation schemes with R=100 Ω, the load current is observed as 4 A. The load voltage and current waveforms for the RL-Load of R=50 Ω & L=100 mH are shown in Fig. 7a and Fig. 7b respectively. During RL-load, the voltage and current of the switches S_2 and S_1 are obtained and shown in Fig. 7(c-f).

Table 4: Simulation and Experimental Parameters.

Parameters	Simulation	Experimental
Input Voltage	400 V	
Capacitor C1	200 V / 1700 µF	200 V / 2200 µF / LGU2D222MELC
Capacitor C2	400 V / 1700 µF	450 V / 1700 µF / PG6DI
Output Voltage	400 V	
RL Load	R=100 Ω and R= 50 Ω & L= 100 mH	
Switching frequency	5 kHz	
Digital Controller	-	TMS320 F28379D
Gate Drive Circuit	-	TLP 250
IGBT Switch	-	SKM75GB063D

6.2 Experimental results

A laboratory prototype was developed to validate the performance of the proposed topology. The Semikron IGBT switches SKM75GB063D with TLP250 driver circuits were used to develop the 1200 W prototype, as shown in Fig. 9. The Texas Instruments TMS320F28379D were used to generate the gating pulses with a switching frequency of 5 kHz. The direct parallel connection of dc source and capacitors increases the charging current, also called inrush current. This inrush current leads to reducing the power components' life, and higher current rating devices are needed and source able to supply high current. To reduce this inrush current soft charging is used, as shown in Fig. 10. A small inductor with a value of 30 µH is inserted in the capacitor charging loop. In the case of capacitor C_1, it doesn't require because the capacitor is connected series with the load during the charging state. The soft charging path will be provided as long as the RLC circuit operates under damping conditions [17]. Initially, the output results are observed for the pure resistive load with the value of R=100 Ω, and the corresponding voltage and current waveform of load and capacitors are shown in Fig. 11a. Most of the inverters operate in inductive load, so it is necessary to test the proposed topology in resistive and inductive loading conditions. So, the proposed topology is tested with a load value of R=50Ω, L=50 mH and measured. It confirms that the proposed topology can perform for any inductive load, as shown in Fig. 11b. Here worth mentioning that the voltage across the capacitors V_{C1} and V_{C2} are not disturbed for inductive load shown in Fig. 11b. The step input variation shown in Fig. 11c confirms that the proposed topology can generate the 5L during the sudden input variation, as shown in Fig. 11c. The load will not be constant, and it is dynamic. So, the load variations are applied by changing from R=100 Ω & R=50 Ω to L=100 mH and the corresponding waveform shown in Fig. 11d. Further, the modulation index is another important factor in an inverter, and it is worth indicating the performance of the proposed topology with the variations of the modulation index. Varying MI=0.5, MI=0.8 and MI=1 test the effect of the modulation index and the corresponding waveforms are shown in Fig. 11e. Hence, the experimental results are confirmed that the proposed topology can operate in any loading conditions. Finally, the proposed topology simulation and measured efficiency are shown in Fig. 12 for different output power. The maximum efficiency is achieved at low output power and low in high output power.

7 Comparative Study

To evaluate the merits and demerits of the proposed 6S-1D-5L topology, the proposed topology is compared with recent inverter topologies, and it is given in Table 5.

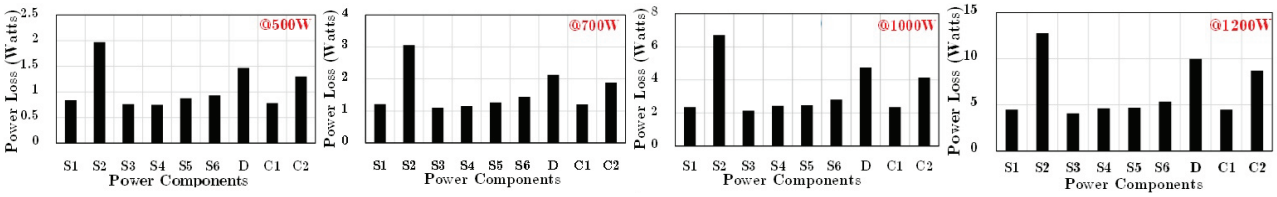


Figure 8: Simulation power loss for various output power (a) 500 W (b) 700 W (c) 1000 W and (d) 1200 W

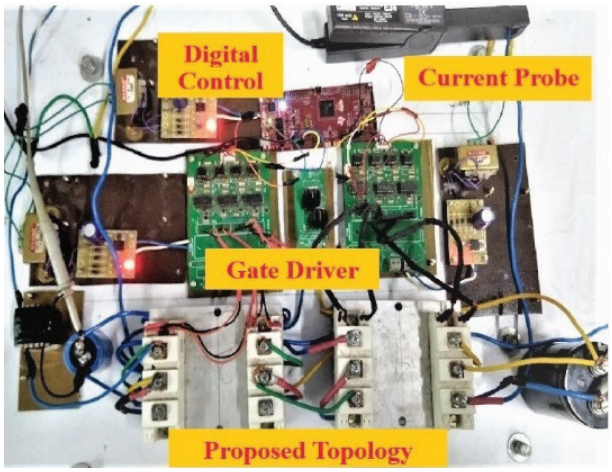


Figure 9: Photograph of prototype hardware setup

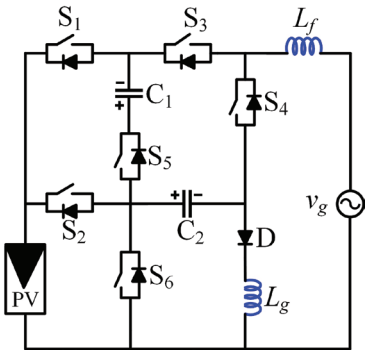


Figure 10: Proposed circuit topology with soft charging inductor

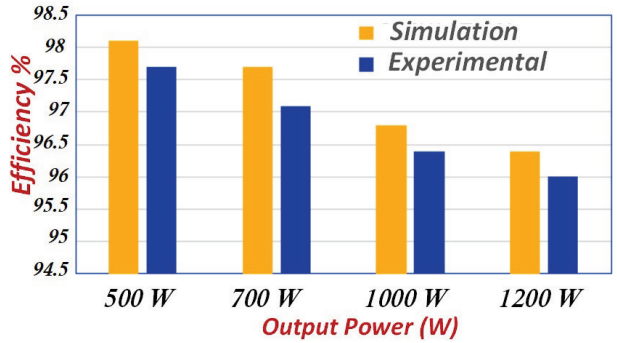


Figure 12: The efficiency of simulation versus hardware result

The comparison is made by considering significant features such as N_S –Number of switches, N_{DR}-Number of driver circuits, N_C-Number of capacitors, N_D-Number of diodes, *TSV* (p.u)-Total standing voltage in per unit, *G*-Gain, V_{Stress}– Maximum voltage stress, V_{Stress}/G, MCS- Maximum number of conducting switches, *CGT*-Common ground type, LC-Leakage Current, P_T- Total Power, η=efficiency. It is observed that the proposed topology has a minimum number of switching components and gate driver units than the topologies mentioned [3], [5], [10], [14]-[15]. The topology [11] offers the same *TSV* (p.u) as that of the proposed 6S-1D-5L inverter topology, but the voltage stress of the topology is very high than the proposed topology. On comparing with the tabulated topologies in the comparative study, it is clear that the proposed topology has the least total standing voltages TSV (p.u) except topologies [12], [14] but the volt-

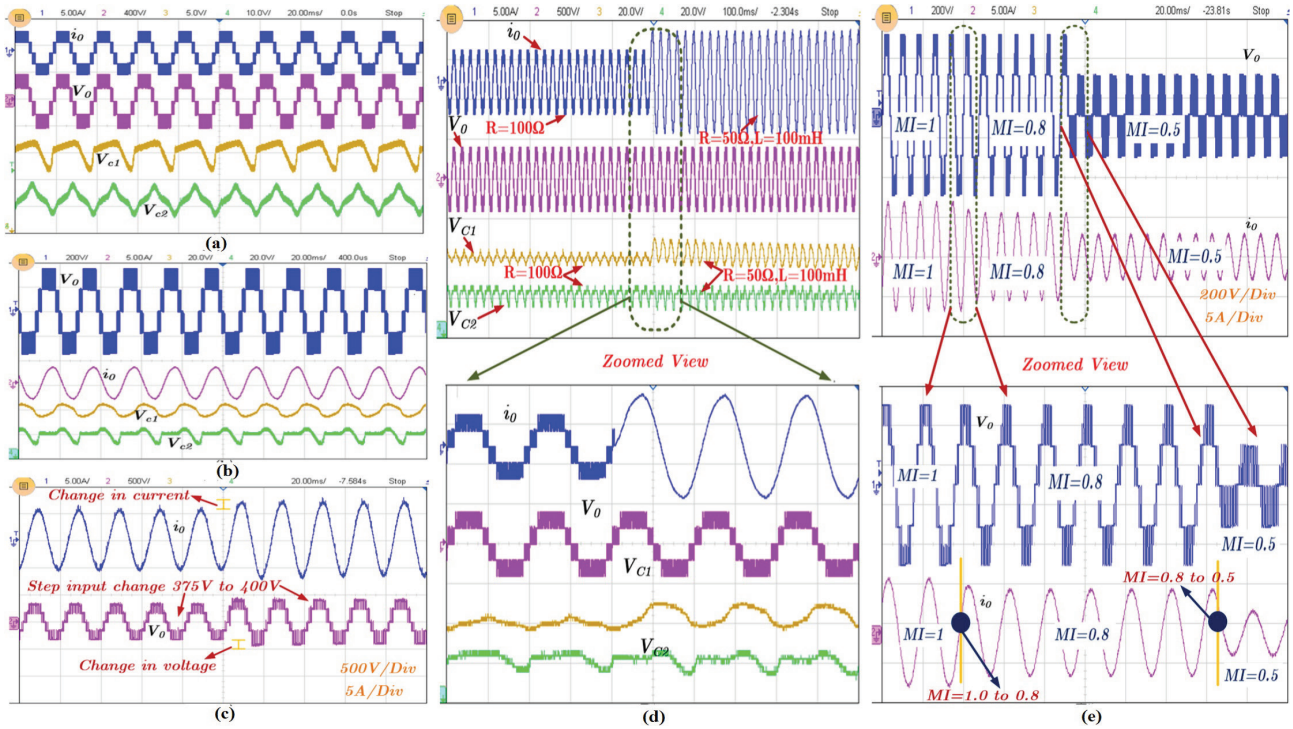


Figure 11: Experimental results of proposed 6S-1D-5L topology (a) for R-Load, (b) for RL load, (c) for step input change, (d) for R to RL load variations and (e) Modulation variation from 1 to 0.8 to 0.5

Table 4: Comparative study with other multilevel inverter topologies

Top	NS	NDR	NC	ND	TSV (p.u.)	G	Capacitor Voltage	V_{Stress}	VStress / G	MCS	CGT	LC /P_T/η%
[3]	9	9	1	0	9	1:2	$2V_{in}$	1	0.5	5	No	NA / 2kW / 97.91
[5]	8	6	3	0	6.5	1:1	V_{in}	1.5	1.5	3	Yes	Zero / 500W / 97.1
[7]	8	8	2	1	12	1:1	$0.5V_{in}$	2	2	4	No	NA / 500W / 96.8
[10]	7	7	2	4	9	1:2	V_{in}	2	1	4	No	NA / 600W / 96.8
[11]	7	6	2	2	6	1:2	V_{in}	4	2	2	Yes	Zero / 600W / 98.1
[12]	6	6	3	1	5	1:1	V_{in}	1	1	3	Yes	Near Zero / 1.2kW / 95.8
[13]	6	6	3	0	8	1:1	V_{in}	1	1	3	Yes	Zero / 1kW / 97
[14]	7	7	3	0	5	1:1	V_{in}	1	1	4	Yes	Zero / 500W / 96.4
[15]	6	6	2	2	10	1:1	$0.5V_{in}$	1.5	1.5	2	No	NA / 400W /97.8
[19]	7	6	3	1	7	1:2	$2V_{in}$	2	1	3	Yes	Zero/750W/98.1
[20]	6	6	3	2	5	1:2	$2V_{in}$	2	1	3	Yes	Zero / 510W/98.1
Pro	6	6	2	1	6	1:1	V_{in}	1.5	1.5	3	Yes	Zero / 1.2kW / 95.43

age stress across the capacitor is very low in the proposed topology which reduces the cost of the inverter. With better TSV (p.u) than other topologies, the proposed topology uses fewer switches. Even with better TSV (p.u) of topology [14], the maximum number of conducting switches is more. On comparing with the topologies [7], [11], the ratio of voltage stress to gain (V_{Stress} /G) of the proposed topology is less. Also, with reference to the comparison Table 5, except for the topology [11], [15] the proposed topology has a smaller number of maximum conducting states than the others. The topology presented in [19] proposes a common ground structure which generates 3L. Despite the usage of two capacitors, the number of ac voltage levels is still three. Also, voltage across one of the capacitors is twice the input voltage. In [20], common ground structure with boosting ability is proposed. But it requires flying capacitor with two times the input supply and also the maximum stress across the switch is equal to twice the input supply. Also, the proposed topology offers high efficiency at low output power.

8 Conclusion

A new transformerless inverter for low power applications is presented in this paper. The proposed topology used two capacitors, and the negative terminal of theload and dc source have a common connection, as discussed. The capacitors voltage is balanced without any additional sensors, and the same is verified in both simulation and experimental results. The output results are discussed, confirming that the proposed topology is suitable for dynamic load variation and modulation index changes. Further, the PLECS analyses the power loss and the various power loss for different output power and the same output power, the measured efficiency is presented. The measured efficiency for the 1.2 kW is 96% without output filter inductor. When including output filter inductor, the efficiency is 95.43% which has a good agreement with simulation efficiency of 96.4%.

9 Acknowledgements

The authors express their gratitude to the SRM Institute of Science and Technology Kattankulathur, Campus 603203, India and Renewable Energy Laboratory (REL), College of Engineering, Prince Sultan University, Riyadh 11586, Saudi Arabia, for financial and technical knowledge transfer. The authors would like to acknowledge the support of Prince Sultan University for paying the Article Processing Fee (APC).

10 Conflict of interest

Authors declaring conflict interest

11 References

1. W. Li, Y. Gu, H. Luo, W. Cui, X. He and C. Xia, "Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4537-4551, 2015, https://doi.org/10.1109/TIE.2015.2399278.
2. Y. P. Siwakoti and F. Blaabjerg, "Common-Ground-Type Transformerless Inverters for Single-Phase Solar Photovoltaic Systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2100-2111, 2018, https://doi.org/10.1109/TIE.2017.2740821.
3. N. Sandeep, J. S. M. Ali, U. R. Yaragatti and K. Vijayakumar,"ASelf-BalancingFive-Level Boosting

Inverter With Reduced Components," *IEEE Trans. Power Electron*., vol. 34, no. 7, pp. 6020-6024,2019, https://doi.org/10.1109/TPEL.2018.2889785
4. M. Saeedifard, R. Iravani and J. Pou, "Analysis and Control of DC-Capacitor-Voltage-Drift Phenomenon of a Passive Front-End Five-Level Converter," *IEEE Trans. Ind. Electron*., vol. 54, no. 6, pp. 3255-3266, 2007, https://doi.org/10.1109/TIE.2007.905967.
5. N. Sandeep, M. J. Sathik, U. R. Yaragatti, V. Krishnasamy, A. K. Verma and H. R. Pota, "Common-Ground-TypeFive-Level Transformerless Inverter Topology With Full DC Bus Utilization," *IEEE Trans. Ind Appl*., vol. 56, no. 4, pp. 4071-4080,2020, https://doi.org/10.1109/TIA.2020.2996152.
6. O. Lopez, R. Teodorescu and J. Doval-Gandoy, "Multilevel transformerless topologies for single-phase grid-connected converters," *Proc. 32nd Annu. Conf. IEEE Ind. Electron*., 2006, pp. 5191-5196, https://doi.org/10.1109/IECON.2006.347656.
7. G. V. Bharath, A. Hota and V. Agarwal, "A New Family of 1-φ Five-Level Transformerless Inverters for Solar PV Applications," *IEEE Trans. Ind. Appl.,* vol. 56, no. 1, pp. 561-569,2020, https://doi.org/10.1109/TIA.2019.2943125.
8. M. J. Sathik et al.,"Switched-capacitor multilevel inverter with self-voltage-balancing for high frequency power distribution system," *IET Power Electron*., Vol. 13, no. 9, pp. 1807-1818,2020, https://doi.org/10.1049/iet-pel.2019.1249
9. M. J. Sathik, N. Sandeep, D. J. Almakhles and U. R. Yaragatti, "A Five-Level Boosting Inverter for PV Application," *IEEE Emerg. Sel. Topics Power Electron*., vol. 9, no. 4, pp. 5016-5025, 2021, https://doi.org/10.1109/JESTPE.2020.3046786.
10. M. Saeedian, S. M. Hosseini and J. Adabi, "A Five-Level Step-Up Module for Multilevel Inverters: Topology, Modulation Strategy, and Implementation," *IEEE J. Emerg. Sel. Topics Power Electron.* vol. 6, no. 4, pp. 2215-2226, 2018, https://doi.org/10.1109/JESTPE.2018.2819498.
11. R. Barzegarkhoo, Y. P. Siwakoti and F. Blaabjerg, "A New Switched-Capacitor Five-Level Inverter Suitable for Transformerless Grid-Connected Applications," *IEEE Trans. Power Electron*., vol. 35, no. 8, pp. 8140-8153, 2020, https://doi.org/10.1109/TPEL.2020.2967336.
12. F. B. Grigoletto, "Five-Level Transformerless Inverter for Single-Phase Solar Photovoltaic Applications," *IEEE Emerg. Sel. Topics Power Electron*., vol. 8, no. 4, pp. 3411-3422, 2020, https://doi.org/10.1109/JESTPE.2019.2891937.
13. A. Kadam and A. Shukla, "A Multilevel Transformerless Inverter Employing Ground Connection Between PV Negative Terminal and Grid Neutral Point," *IEEE Trans. Ind. Electron*., vol. 64, no. 11, pp. 8897-8907, 2017, https://doi.org/10.1109/TIE.2017.2696460.
14. F. B. Grigoletto, "Multilevel Common-Ground Transformerless Inverter for Photovoltaic Applications," I*EEE Trans. Emerg. Sel. Topics Power Electron*., vol. 9, no. 1, pp. 831-842, 2021, https://doi.org/10.1109/JESTPE.2020.2979158.
15. G. E. Valderrama, G. V. Guzman, E. I. Pool-Mazún, P. R. Martinez-Rodriguez, M. J. Lopez-Sanchez and J. M. S. Zuñiga, "A Single-Phase Asymmetrical T-Type Five-Level Transformerless PV Inverter," *IEEE Trans. Emerg. Sel. Topics Power Electron*., vol. 6, no. 1, pp. 140-150, 2018, https://doi.org/10.1109/JESTPE.2017.2726989.
16. B. S. Naik, Y. Suresh, J. Venkataramanaiah and A. K. Panda, "A Hybrid Nine-Level Inverter Topology With Boosting Capability and Reduced Component Count," *IEEE Trans. Circuits Syst*. II Express Briefs., vol. 68, no. 1, pp. 316-320, 2021, https://doi.org/10.1109/TCSII.2020.2998496.
17. A. Kumar and P. Sensarma, "A Four-Switch Single-Stage Single-Phase Buck–Boost Inverter," *IEEE Trans. Power Electron*., vol. 32, no. 7, pp. 5282-5292, 2017, https://doi.org/10.1109/TPEL.2016.2605150.
18. N. Sandeep and U. R. Yaragatti, "Design and Implementation of a Sensorless Multilevel Inverter With Reduced Part Count," *IEEE Trans. Power Electron*., vol. 32, no. 9, pp. 6677-6683, 2017, https://doi.org/10.1109/TPEL.2017.2681739.
19. N. Vosoughi, S. H. Hosseini and M. Sabahi, "A New Single-Phase Transformerless Grid-Connected Inverter With Boosting Ability and Common Ground Feature," *IEEE Trans. Ind. Electron*., vol. 67, no. 11, pp. 9313-9325, 2020, https://doi.org/10.1109/TIE.2019.2952781.
20. N. Vosoughi, S. H. Hosseini and M. Sabahi, "A New Transformer-Less Five-Level Grid-Tied Inverter for Photovoltaic Applications," *IEEE Trans. Energy Convers.,* vol. 35, no. 1, pp. 106-118, 2020, https://doi.org/10.1109/TEC.2019.2940539.

Arrived: 01. 09. 2021
Accepted: 07. 03. 2022