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# Digital Signal Processing for a Multi-Channel Chemical Sensor Interface

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**Abstract:** This paper presents digital signal processing for a miniature, multi-channel, multi-sensor detection system, based on chemically functionalized COMB micro-capacitors and low noise integrated analog electronics. The presented system is capable of detecting traces of different molecules in the air. Currently, it is possible to detect less than 3ppt of target molecules in the atmosphere at room temperature in a 1 Hz bandwidth. For such multi-channel measurements with extreme requirements regarding sensitivity, it is necessary to have the appropriate analog signal processing electronics, as well as digital signal processing hardware, algorithms, and software. The complete architecture of the DSP part of a multi-channel sensor measurement system is explained, together with some simulation and the measured results.

**Keywords:** Digital Signal Processing DSP, decimation filter, FPGA, measurement of capacitance changes, measurement system

# Digitalno signalno procesiranje več-kanalnega merilnega sistema za merjenje kapacitivnosti kemično modificiranih COMB senzorjev

**Izvleček:** Članek opisuje digitalno signalno procesiranje miniaturnega, večkanalnega detekcijskega sistema, ki temelji na kemično modificiranih COMB senzorjih, integriranem nizko-šumnem analognem integriranem vezju ter vezju za digitalno procesiranju signalov. Predstavljen detekcijski sistem zaznava različne molekule v zraku v izjemno majhnih koncentracijah; detekcijski nivo pri sobni temperaturi znaša 3 molekule TNT med 1012 molekulami nosilnega plina pri pasovni širini 1Hz. Pomemben gradnik več-kanalnega senzorskega merilnega sistema s skrajnimi zahtevami glede občutljivosti, je tudi primerno digitalno procesiranje signalov, ustrezna arhitektura, algoritmi in pomožni programi, ki jih predstavljamo v članku skupaj s rezultati nekaterih pomembnih simulacij ter nekaterimi merilnimi rezultati.

**Ključne besede:** Digitalno Signalno Procesiranje DSP, CIC decimacijski filter, FPGA, merjenje spremembe kapacitivnosti, merilni sistem

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## 1 Introduction

Vapor detection systems already exist on the market. Chemo-mechanical sensors, initiated in the mid-1990s are based on a cantilever where adsorption of the target molecules on a modified surface bends the cantilever [1]. However, position measurement is difficult because of changing temperature, pressure, sensor vibration, etc. A differential capacitance comb-shaped (COMB) sensor and associated low noise electronics provide much lower sensitivity to the environmental influences. In this work, we present the DSP (Digital Signal Processing) part of a multi-channel detection system based on the measurements of the capacitance difference between modified (chemically treated, i.e. functionalized) and reference (untreated) capacitors [2]. The primary role of DSP is to extract useful information from the ΣΔ modulator bit-stream. As an important part of the complete detection system, it must be designed properly to get optimal results in as short time as possible, without introducing additional noise.

This paper is organized as follows. A general description of the entire measurement system is given in Section 2 with a short explanation of the analog signal processing module implemented on the ASIC (Application–Specific Integrated Circuit). Section 3 describes a 30-channel digital signal processor, while

Section 4 describes its implementation on the FPGA. The user interface and some measurement results are presented in Section 5 while the conclusions are given in Section 6.

## 2 Measurement system

A simplified block diagram of the signal processing electronics and data processing software running on the PC is shown in Figure 1. The whole measurement system is basically a lock-in amplifier [2] built from: low noise, analog front-end (AFE) electronics; digital front-end (DFE) control logic and the DSP. The AFE and DFE are integrated into the ASIC (application specific integrated circuit) designed in 0.25um BCD (BIPOLAR-CMOS-DMOS) process, while the DSP is currently realized on the FPGA. The AFE consists of necessary analog electronic components [2],[3] which are programmable, so that different gains, frequencies, and excitation signals for the sensors can be adjusted. The AFE configuration is set by DFE through a Serial Peripheral Interface (SPI). The existing ASIC is capable of processing the signals from two differential sensors. Each sensor must be calibrated, since the initial difference of two capacitors in one differential sensor can reach up to 10%. Therefore, a programmable capacitor array is implemented on the AFE part, which is connected in parallel to each sensor's capacitor. The programmability range of the calibration capacitors is from 1fF to 64fF in steps of 1fF.

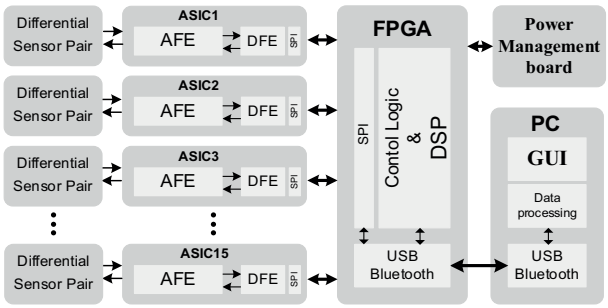


**Figure 1:** Measurement system block structure

The measurement results of each sensor are proportional to the capacitance difference caused by adsorption of the target molecule to the modified sensor. During calibration, in a natural atmosphere without traces of the target molecules, we calibrate the difference between each differential capacitor and bring the result close to zero. In this way the dynamic range of the measurement channel is increased so that higher channel gains and excitation voltages are possible. The multi-channel measurement system consists of 15 ASICs, each with two differential sensors; thus a 30 – channel measurement system is implemented. Each digital signal from the AFE carries the information of the capacitance difference. Signals from all sensors are connected to the FPGA, where DSP algorithms extract the information. The results of the DSP processing are sent to the PC via Bluetooth or USB interface, where further signal processing prepares the results for the presentation and storage.

The decisive parts regarding the sensitivity of the entire measurement system are differential comb capacitors and low noise electronics, which must be capable of detecting a low number of adsorbed target molecules on the surface of the functionalized capacitor [2]. The block diagram of one ASIC channel including two sensors is shown on Figure 2 [2],[3]. Two differential sensors can be connected to one measurement channel.

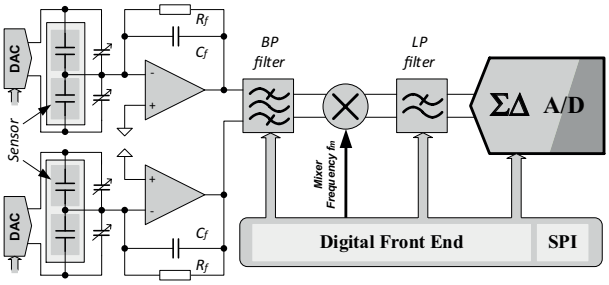


**Figure 2:** Block diagram of the ASIC including two sensors [2],[3].

Sensors are driven by square-wave signals $V_s$ with slightly different frequencies. The difference in charges from the sensor is transformed into the voltage using a low noise charge amplifier with the help of the excitation signals. The output voltage of the charge amplifier can be calculated according to (1).

$$V_{cho}(s) = V_s \cdot \frac{\Delta C}{C_f} \cdot \frac{s}{1/(C_f \cdot R_f) + s} \tag{1}$$

The frequencies are selected well above the *1/f* noise corner frequency of the charge amplifier. The amplitude and frequency of the excitation signals are fully programmable. The output signal of the charge amplifier $V_{cho}$ is band-pass filtered and amplified. The signal contains the main spectral components from two sensors and corresponding higher harmonics due to square-wave excitation signals. Therefore, the analog mixer generates the differences and sums of all main and harmonic spectral components. The differences are $f_{o1} = f_{s1} - f_m$ for the first sensor, and $f_{o2} = f_{s2} - f_m$ for the second. Low frequency signals are amplified, while high frequencies and the remains of the higher harmonics from the mixing products are

attenuated by a programmable analog low-pass filter. The resulting signal is finally quantized with a second order Σ-Δ A/D converter, implemented in the AFE part of the ASIC [2],[3]. The described AFE structure enables the possibility of using one analog channel for more sensors, avoiding the influence of the DC offset voltage and the *1/f* noise.

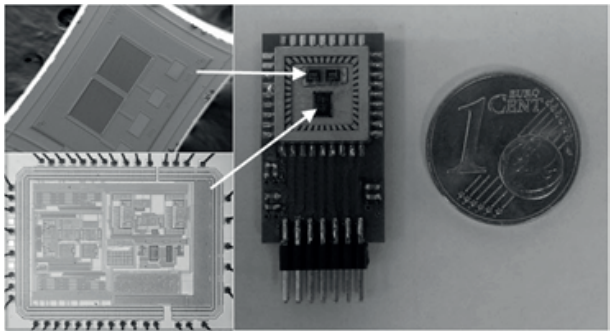

**Figure 3:** System in Package (SiP) measurement board: (left) COMB differential sensor and ASIC. (right) measurement board.

The SEM micrograph of a differential COMB capacitive sensor and photomicrograph of the ASIC is shown on the left side of Figure 3. The PCB with one ASIC and two differential sensors as a System In Package (SiP) is presented on the right side of Figure 3; for a size comparison an 1 Euro-cent coin is added. The ASIC and sensor sizes are 2.5×2mm and 1.2×1.5mm, respectively.

Another important part of the system is the digital part implemented on the FPGA. It consists of the SPI (Serial Peripheral Interface), a communication unit for the connection with the PC, a command decoder, excitation signal generators, a data encoder, a multi-channel DSP, and an additional digital signal processing hardware for extracting the information from the decimation filters. In next section, the DSP part will be described in detail. The block diagram of the complete implementation on the FPGA is shown in Figure 4.

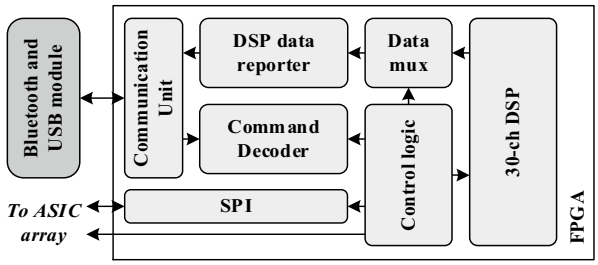


**Figure 4:** Block diagram of the FPGA implementation

The visual representations of DSP results are managed by the Graphical User Interface (GUI) developed to run on the PC (see Figure 1). It allows us to control various parameters of the analog part, as well as the parameters of the DSP module. It is possible to control various gains, excitation frequencies, voltages, and calibration capacitors in the AFE part, while in the DSP part we can control frequencies and phases of the down-mixing signals and decimation ratio of the last decimation filter. The programmability of the last decimation filter enables the possibility to adjust the bandwidth and the output data rate.

## 3 Digital signal processing

Each ASIC converts the capacitance changes from two differential sensors into a digital bit-stream, which is captured by the DSP for further digital signal processing. The DSP was designed and tested with a top-down design approach using Matlab and Simulink [4],[5]. After modeling, the DSP algorithms were coded to the Register Transfer Level (RTL) using VHDL, and then synthesized and implemented on the FPGA. The hierarchical Simulink environment makes it possible to efficiently model, simulate, and design all circuits on a high hierarchical level. Another important advantage of the high-level approach is to model and simulate the analogue and digital parts together in a very short time. In this way the appropriate decisions can be executed early in the design process, which improves the efficiency of the design. Signals used for driving, mixing, down-sampling timing, and further filtering must be strictly coherent (the measurement period is a multiple of every signal period and their ratios are prime numbers). All digital filters are realized with Cascaded Integrator – Comb (CIC) decimation filter architecture [6], as shown in Figure 5. The purpose of the CIC decimation filter is to remove the out-of-band shaped quantization noise and to reduce the data rate to the Nyquist rate. The order of the decimation filter should be larger than the order of the modulator to sufficiently suppress the out-of-band quantization

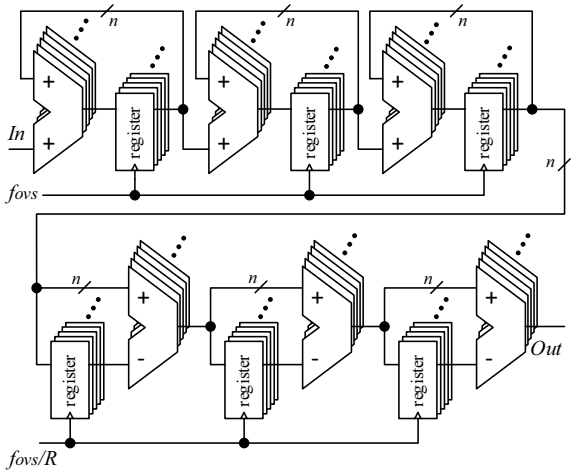


**Figure 5:** 3rd order CIC decimation filter structure [6]

noise. In our case we use a 3rd order sinc decimation filter with the standard structure [6] presented in Figure 5. The filter word length is optimized in such a way that no additional quantization noise due to finite word lengths is added into the filtering process [6]. In the full-precision mode, all registers following the first register must support the maximum accumulation produced by the first integrator section.

According to the known CIC filter properties, the overflows of the integrating and differentiating sections are not significant if the wrap-around two's complement arithmetic is used with a modular wrap-around property [4]. The integrating stages run with the oversampling frequency, while the comb sections run with a sampling frequency divided by the factor *R* (oversampling ratio). The decimation ratio in the first decimation filter stage is small in order to generate coherent signals.

The transfer function in the z-domain and the corresponding maximum dynamic range growth at DC for the decimation filter are given in (2), where *N* is the order of the filter and *R* is the decimation factor [6], [7], [8].

$$H_{dec}(\mathrm{z}) = \left[\frac{1-z^{-RM}}{1-z^{-1}}\right]^N \Rightarrow \left|H_{dec}(\mathrm{e}^{j0})\right| = RM^N \quad (2)$$

In our case, the comb filter differential delay *M* is always equal to 1 and will not be addressed in further equations. It is known that the transfer function has zeros $f_Z$ defined in (3), where *k* is the integer multiplier ($k \in \mathbb{Z}$).

$$f_Z = k \cdot f_{dec} = k \cdot \frac{f_{ovs}}{R} \quad (3)$$

All components in the pass-band are mapped around the multiples of the output sampling frequency $f_Z$. If we define $f_{cut}$ to be the passband cutoff frequency of a usable pass-band *f*, then the imaging regions are defined as (4).

$$\left(f_Z - f_{cut}\right) \le f \le \left(f_Z + f_{cut}\right) \quad (4)$$

The passband cutoff frequency has to be smaller than $f_{ovs}/2R$ in order to avoid aliasing of the imaging frequency bands around the zeroes $f_z$. To attenuate those regions in the cascaded filter structure, the decimation rates are selected in such a way that the zeroes of all filters are covered with zeroes caused by the output sampling frequency of the previous filter. By increasing the number of stages, we improve the filter's ability to reject the image components. Unfortunately, the attenuation at the passband edge is increased as well, which can be compensated with appropriate FIR filter in series after CIC filter. In our case the relevant signals after digital down-mixing become DC components, therefore the compensation filter is unnecessary. This process is shown in Figure 7 below.

The main parts of the DSP are: the configuration register, down-mixers, frequency dividers, and CIC filters. As previously mentioned, each ASIC process the signals from two sensors and thus each bit-stream contains information from two sensors. The DSP separates those two components into separate channels; each channel is followed by digital filter to reduce the bandwidth and provide appropriate outputs for further processing. The block diagram of a complete DSP is presented in Figure 6.

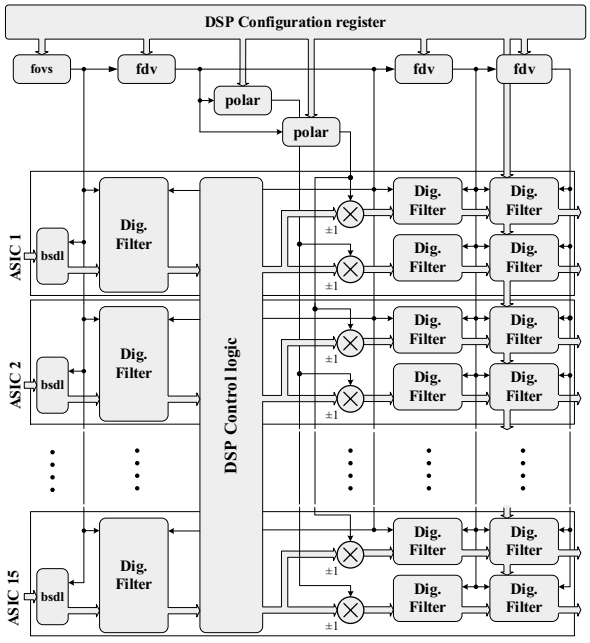


**Figure 6:** Block diagram of the DSP

The output of each ΣΔ - modulator is a stream of 1-bit data, with the frequency of 6.25 MHz. The first decimation filter performs only a rough filtering to remove high frequency-shaped quantization noise of the bit-stream, using decimation rate $R_1 = f_{ovs}/f_{dec1} = f_{ovs}/2f_N = 16$. Accordingly, the output rate is reduced from $f_{ovs}$ to $f_{dec1} = f_{ovs}/R_1 = 390625\ Hz$. The spectrum contains two main components at frequencies $f_{o1}$ and $f_{o2}$ and the remains of the attenuated high frequency of the mixing process and thermal noise. The amplitudes of the main spectral components are proportional to the corresponding sensor capacitance difference and excitation signal amplitudes. The noise, which reduces the signal-to-noise ratio (SnR) of the measurement, can be reduced by decreasing the bandwidth of the digital

results. The main spectral components of each channel are translated to DC by mixing the output signal from the first filter with two digital square-waves with frequencies $f_{o1}$ and $f_{o2}$. The results are two separated DC digital signals, as shown in Figure 6, where $G_{D1}$, $G_{D2}$ and $G_{D3}$ represent the gain of the filters.

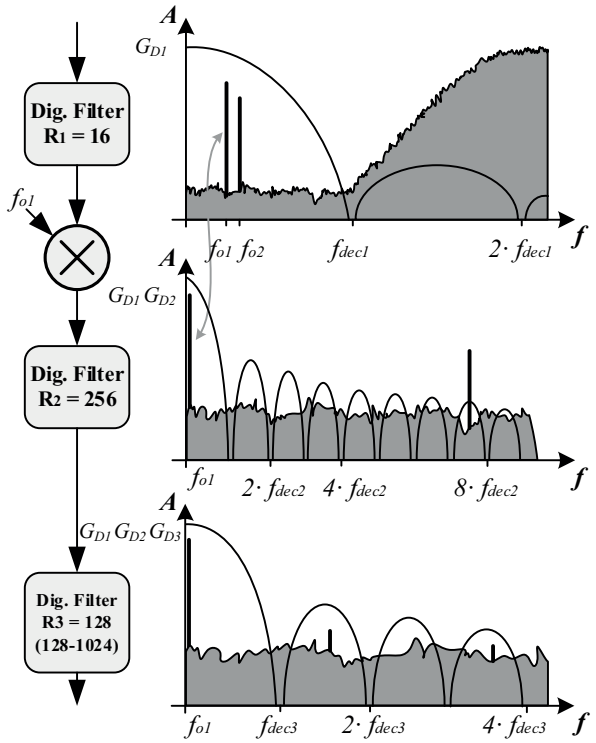


**Figure 7:** Digital signal processing for one channel

In order to remove the remains of the high frequency spectral components and to reduce the data rate, two additional decimation filters are used with the default decimation rates $R_2$ = 256 and $R_3$ = 128 with zeroes at $k{\cdot}f_{dec1}/R_2$ and $k{\cdot}f_{dec2}/R_3$, respectively. This procedure is presented in Figure 7. The bandwidth and the output data rate after both low-pass digital filters is reduced to $f_{ovs}/(R_1R_2R_3) \cong 12$ Hz. With the ability to change the last decimation rate in a range from 128 to 1024, we can reduce the output data rate down to ~ 1.5Hz. The results are then transferred to the PC for further filtering, decimation, storage, and presentation.

## 4 Implementation of the dsp and other digital parts

The majority of the digital circuits including the DSP are implemented on the FPGA as shown in Figure 4. For correct operation of all decimation filters, we have to ensure appropriate word length to prevent data distortion due to the overflow. The highest pass-band gain occurs at the DC, which is a function of the number of stages as defined in (2). Since the two's complement arithmetic is used, the maximum required number of bits $B_{MAX}$ for the accumulation is calculated by using (5) [6], where $N{\cdot}\lceil log_2 R \rceil$ represents the maximum register growth.

$$B_{MAX} = N \cdot \lceil \log_2 R \rceil + B_{IN} \tag{5}$$

$B_{IN}$ is the number of input bits, $N$ is number of stages and $R$ is the decimation ratio. Brackets $\lceil x \rceil$ represents ceil function (the smallest integer not less than x). In multistage decimation CIC filters, this can result in large register widths due to register growth for every added decimation filter by $N{\cdot}\lceil log_2 R \rceil$, leading to high consumption of hardware resources. The word-length of registers is possible to control by truncation and unbiased rounding to even numbers in each output stage. This reduces the gain of the filter by a factor of $2^{Btr}$, where *Btr* is the number of cut off LSB bits. Truncation also increases the overall quantization noise, which has to be below the noise of analog electronics. With the help of the Matlab Simulink system simulations we have found that the output word-length of 22-bits in the second, and 24-bits in the third decimation filter are long enough to maintain the 100 dB dynamic range. The complete system is designed in such a way that the quantization noise generated in the modulator and in the decimation filters is always smaller than amplified thermal noise generated in the charge amplifier. The overall truncation noise variance σ at each filter output is defined in (6), where $B_{MAX}$ is the maximum register growth according equation (5), and $B_{OUT}$ is an output word-length [6].

$$\sigma^2 = \frac{\left(2^{B_{MAX}-B_{OUT}}\right)^2}{12} \tag{6}$$

The total quantization noise variance of all digital filters is then calculated using (7), where $\sigma_k$ is the output variance of the error for each filter.

$$\sigma_{out}^2 = \sum_{k=1}^{n} \sigma_k^2 \tag{7}$$

A detailed description of the quantization noise can be found in [6]. In our case, the first 3rd order decimator ($R_1$ = 16) requires 14 bits, the second decimator ($R_2$ = 256) requires 38 bits with output truncation to 22 bits, and the third decimator with programmable down-sampling ratio $R_3$ from 128 to 1024 requires 43 to 52 bits (depending on the R factor) with output truncation to 24 bits. The FPGA resources allow us to build simple CIC filter structures with equal (maximal) number of internal bits for all integrator and comb stages. In the

integrated version of the system it will be considered to use the Hogenauer pruning technique to reduce usage of the silicon area, as well as power consumption. The word-length profiles of CIC decimation filters in each channel are shown in Figure 8.

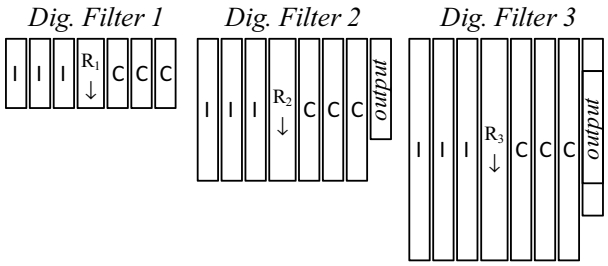


**Figure 8:** Word-length profile of CIC decimators

The word-length of the last decimator changes according to equation (5), due to the controllable decimation rate. The highest word-length *Bmax(R=1024)* has been used to assure appropriate accumulation for all selectable decimation rates defined by $R^m$, where *m* is in the range of 7 to 10. The wrap-around two's complement arithmetic also provides correct results before truncation for lower decimation rates. Truncation without adjustment at the output, starting from MSB, would result in the output value reduced by the factor $2^{Bmax(1024)-Bmax(R)}$, where *Bmax(R)* represents the word-length of the selected decimation rate *R*. This happens because of the larger word-length at smaller decimation rates that would be otherwise smaller according to (5). To get the correct result it is necessary to truncate the output, left shifted for *Bmax1024 – BmaxR* bits. The position of truncation output bits at different decimation rates is shown in Figure 9.

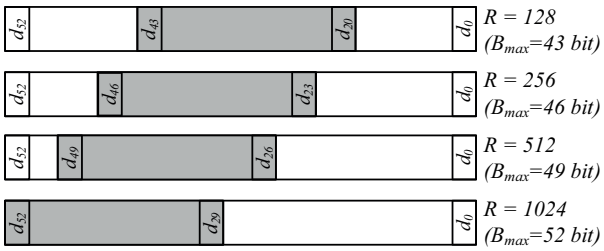


**Figure 9:** Truncation at last decimator according to decimation rate R

Another issue in order to assure correct system operation is the need for the synchronization of sensor excitation signals with the down-mixing signals $f_{o1}$ and $f_{o2}$.

Synchronization is needed because the excitation signals are generated in the ASIC, while the down-mixing signals $f_{o1}$ and $f_{o2}$ are generated in the physically separated block (FPGA). Those two pairs of signals must have the same phase to obtain a valid measurement

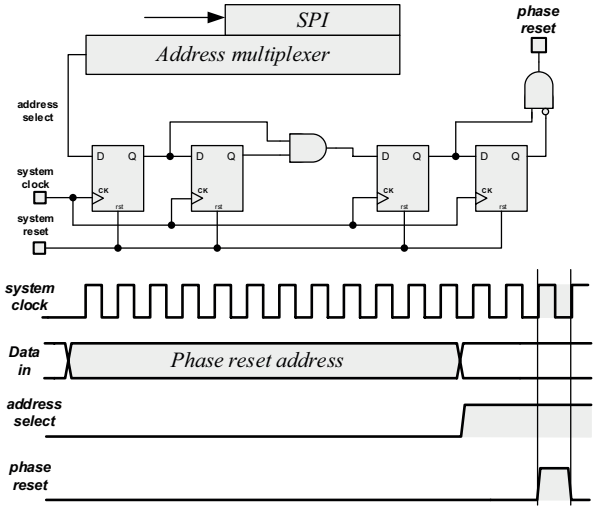


**Figure 10:** Phase reset circuit implemented in the ASIC and in the FPGA with timing diagram

result. The synchronization takes place with the simultaneous phase reset in the ASIC and FPGA at the beginning of each measurement cycle. The reset circuit shown in Figure 10 is initiated by the simultaneous decoding of the unique SPI address in both systems. The first two flip-flops prevent the meta-stability, while the other two realize the front edge detector. When required, the reset pulse with one clock cycle width is generated in both systems.

Another significant part of the system is the DSP data reporter, responsible for proper data transfer from the DSP to the communication unit. Generally, the DSP data reporter is a finite state machine, which converts the last filter output into a stream of hexadecimal characters. The universal asynchronous receiver/transmitter transfer rate was adapted to send the results from 30 channels at the smallest selectable decimation rate (i.e. the highest output rate). A simplified block diagram of the DSP data reporter with the communication and PC data processing units is shown in Figure 11.

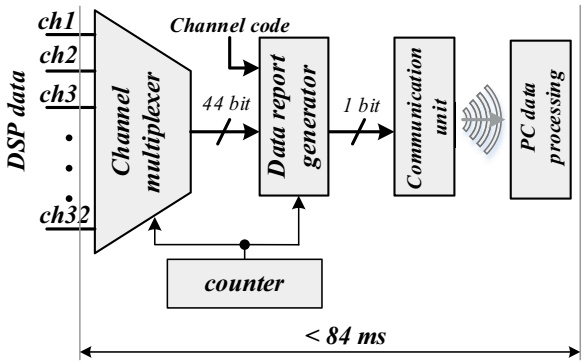


**Figure 11:** DSP data reporter block diagram with Communication unit

Table 4.1 shows the device utilization summary of the implementation on the FPGA for the entire digital system.

**Table 4.1:** FPGA hardware utilization summery

| *Logic Utilization* | *Used* |
|---|---|
| *Number of Slices* | 20698 |
| *Number of Slice Flip Flops* | 23377 |
| *Number of 4 input LUTs* | 25261 |
| *Number of bonded IOBs* | 59 |
| *Number of GCLKs* | 3 |

## *5 Measurement results and data processing*

The measurements were performed in a controlled laboratory environment using a gas generator and the measurement system, described in Section 2 and 3, and shown in Figure 12. Figure 13 shows the Graphical User Interface (GUI), written with the C# (C Sharp) programming language in the Visual Studio environment.

The GUI allows us to control the current system parameters through ASIC and DSP settings. The digital response at the DSP output is *ΔN,* which is dimensionless

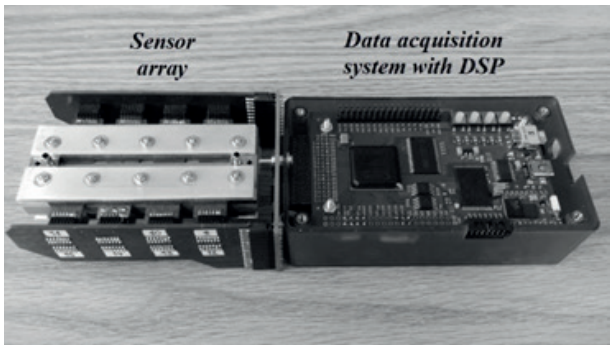


**Figure 12:** Measurement system with Sensor array and Data acquisition system

and proportional to the relative change of the capacitance $\Delta C_x/C_f$. $\Delta N$ can be estimated using (8), where $\Delta V_{sx}$ is the excitation signal amplitude, $G_A$ is the gain of complete analogue measurement path and $G_{D1}$, $G_{D2}$ and $G_{D3}$ are the gains of the DSP part [2].

$$\Delta N \cong \Delta V_{sx} \cdot \frac{\Delta C_x}{C_f} \cdot G_A \cdot G_{D1} \cdot G_{D2} \cdot G_{D3} \tag{8}$$

It is also necessary to consider the gain loss due to truncation at the output of last two decimation filters. The gains of truncated filters in equation (8) have to be reduced according to (9).

$$G_{D1} = R_1^N,\ G_{D2} = \frac{R_2^N}{2^{B_{MAX2}-B_{OUT2}}},\ G_{D3} = \frac{R_3^N}{2^{B_{MAX3}-B_{OUT3}}} \tag{9}$$

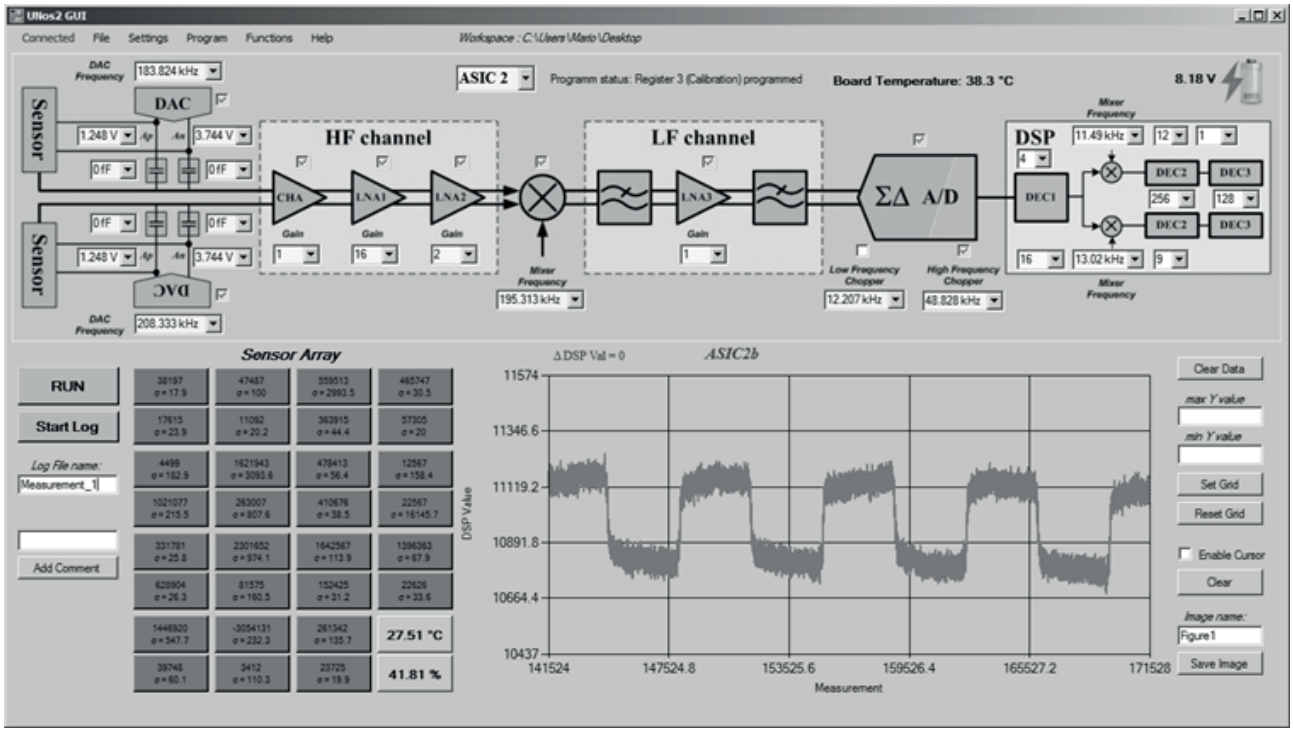


**Figure 13:** User interface with a measurement result on the modified sensor

The DSP provides ~1.5 to ~12 results per second depending of the last decimation rate. Those results can be filtered on the PC, using the moving average filter according to (10).

$$AVG(n) = AVG(n-1) + \frac{x(n)}{M} - \frac{x(n-M)}{M} \qquad (10)$$

The moving average period *M* can be set with a constant value from 8 to 512. The algorithm in the GUI also calculates a standard deviation of the results and generates Matlab scripts for further analysis. All results can be stored in the files for off-line processing and examination. To monitor environmental conditions of the gas mixtures, one measurement channel is dedicated for the temperature and the humidity sensor.

The DSP result presented in Figure 14 shows the consequence of switching the input gas between dry $N_2$ and the $N_2$ contaminated with the target molecules (TNT with ½ vapor pressure) for one channel with 12Hz bandwidth. The modified sensor surface is functionalized with APS molecules [2], while the untreated reference sensor is used as a control sensor to track only environmental changes without the response to the target molecules. We estimate the normalized sensitivity $S_{TNT}$ in 1 Hz band using (11) [2], where ΔN is the difference between two results from DSP and *BW*=12Hz (after DSP filtering).

$$S_{TNT} \cong \frac{3.5 \cdot 10^{-12}}{\left(\Delta N_{TNT}\sqrt{BW}\right)} = \frac{3.5 \cdot 10^{-12}}{\sqrt{Hz}} \qquad (11)$$

The measured, input referred noise level of the DSP is much smaller than the equivalent input referred thermal noise level of the charge amplifier. From this, we can conclude that DSP does not bring additional noise to the system. The long measurement times are the consequence of slow gas flow, caused by piezoelectric pumps capacity (15 ml/min) and relatively big nonfunctional volume of connecting tubes.

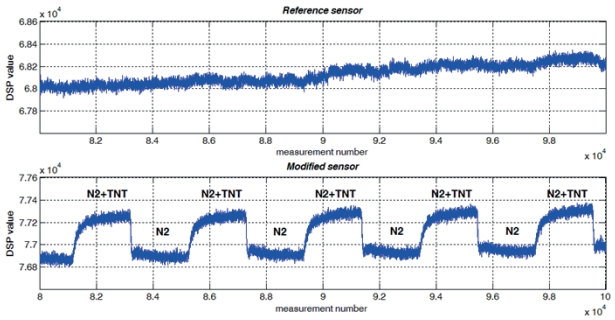


**Figure 14:** Measured response of the system, switching between pure N2 and a mixture of N2 and 50% vapor pressure of TNT at room temperature. The environmental drift in the reference sensor is repeated in the modified sensor.

## 6 Conclusions

The implementation of Digital Signal Processing for a miniature, multi-channel, vapor trace detection system is presented. At the moment the detection system it is capable of detecting vapor traces of different explosives. The 30-channel measurement system including all measurement boards (ASICs + sensors), consumes a relatively low amount of energy (approximately 200mA at 7.2V). A further plan is to integrate a complete detection system, which could lead to a cheap, efficient, and very selective vapor trace detection system for different molecules in the air. Integration will reduce the volume and power consumption of the complete system. The power and silicon area will also be reduced with appropriate pruning technique for internal word-length reduction in filter registers. We also plan to upgrade the GUI with an automatic sensor calibration and test engine to be able to verify the operation of each ASIC in the array during the startup time.

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