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Design of an active inductor based LNA in Silterra 130 nm CMOS process technology

Mohammad Arif Sobhan Bhuiyan, Jia Xien Chew, Mamun Bin Ibne Reaz, Noorfazila Kamal

Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, Bangi, Selangor, Malaysia

Abstract: In this paper, an active inductor based CMOS low noise amplifier (LNA) has been illustrated for 2.4 GHz ISM band RF receivers. The proposed LNA has three stages: the common gate amplifier, the active inductor and the output buffer. The LNA is designed in Silterra 130-nm CMOS process. It operates at 1.2V supply voltage and exhibit a high gain (S21) of 33dB and reverse isolation (S12) of -33.1dB. The power dissipation of the LNA is only 1.51mW with 8.51 dB noise figure and 35.5dB IIP3. In the proposed LNA, active inductor circuit replaces the usual passive spiral inductor to keep the size of the chip area at 0.0004mm2. Such an LNA will be a better choice for high performance, fully integrated, low cost and low power RF receivers.

Keywords: CMOS; LNA; Active Inductor; RF

Zasnova nizko šumnega ojačevalnika na osnovi aktivne dušilke s Silterra 130 nm CMOS tehnološkim procesom

Izvleček: V članku je prikazan CMOS nizko šumni ojačevalnik (LNA) na osnovi aktivne dušilke za RF sprejemnike v ISM frekvenčnem območju 2,4 GHz. Predlagani LNA je sestavljen iz treh stopenj: ojačevalnik s skupnimi vrati, aktivna dušilka in izhodni ojačevalnik. LNA je načrtovan za Silterra 130-nm CMOS proces. Deluje pri napajalni napetosti 1,2 V, ima veliko ojačenje (S21) 33 dB in majhno povratno ojačenje (S12) 33,1 dB. Poraba moči znaša le 1,51 mW, šumno število ima 8.51 dB in IIP3 35,5 dB. Pri predlaganem LNA aktivna dušilka nadomešča običajno pasivno spiralno dušilko, s čimer dosežemo velikost vezja le 0,0004 mm2. Tak LNA bo boljša izbira za visokozmogljive v celoti integrirane nizkocenovne RF sprejemnike nizkih moči.

Ključne besede: CMOS; LNA; aktivna dušilka; RF

** Corresponding Author's e-mail: asobhan@eng.ukm.my*

1 Introduction

The continuous advancement in CMOS technology allows the researchers to fabricate fully on-chip transceivers without compromising the performance issues. Therefore, the current trend is to design low power compact devices by eliminating bulky board level off-chip components. This resulted low power, small size and low cost wireless terminals for different applications such as RFID, Bluetooth, Zigbee, Wi-Fi, WLAN devices etc. [1, 2, 3]. The size and performance of such devices largely depend on the size and performance of their transceivers. Therefore performance enhancement of such wireless transceivers is very important.

An LNA is typically the first active amplification block of an RF receiver, as shown in Fig. 1. Its performance greatly affects the overall receiver performance. Main performance parameters of a typical LNA are: input matching S_{11} (dB), reverse isolation S_{12} (dB), gain S_{21} (dB), output matching S_{22} (dB), NF (dB), IIP3 (dBm), power dissipation (mW), Chip size (mm^2) etc. The type of mixture with which LNA is to be used is very important to determine the necessary trade off among the performance criteria. For example, the requirement for gain of the LNA, when used with active mixture, can be relaxed as such a mixer provides active gain while consuming some dc power. But its power consumption needs to be lowered to compensate for the power

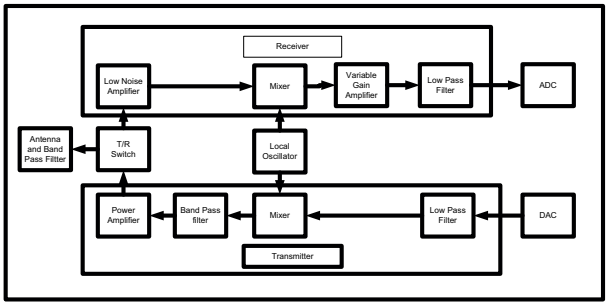

Figure 1: Analog front of a 2.45 GHz RF transceiver.

consumption from the active mixer. With a relaxed gain, the LNA should have good noise figure (NF) to avoid degrading the overall receiver NF.

LNA is a one of the crucial blocks of an RF receiver which deals with very low power signal. LNAs are usually designed in two common topologies: Common-Source LNA (CSLNA) and Common- Gate LNA (CGLNA) [3, 4]. These two topologies use passive inductors which results in larger chip area and thus increased cost. Generally, the parasitic effects and losses related to the substrate degrade the total performance of the LNAs. Therefore, various techniques have been used by the researchers to improve the LNA performance. Current-reuse technique in CGLNA is usually utilized to better the transconductance but the area becomes larger due to the usage of bulky passive inductors [5]. Noise cancelling techniques are also used to decrease the NF, but it suffers from high frequency effects [6, 7] and low voltage gain [8, 9].

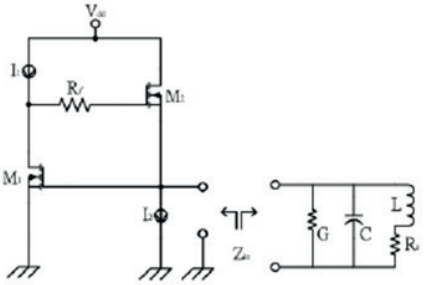

Figure 2: Typical single ended gyrator-C active inductor and its equivalent circuit [1].

To overcome the margins, active inductor based band pass filters have been introduced. Active inductors manage to constantly tune to protect temperature or process variations. Beyond that, active inductor only takes about 1% until 10% of passive active inductor area which can produce smaller chip area and cost [10]. Besides they also have higher inductance value, wide frequency tuning range and higher quality factor which are essential for different circuit designs [11]. However, inductor-less LNA although reduces chip size but can cause high power dissipation [12, 13]. Fig. 2 shows a typical single ended gyrator-C active inductor and its equivalent circuit.

In this paper, an LNA design with low power dissipation and high gain for 2.4 GHz ISM band RF receivers has been proposed in Silterra 130-nm CMOS process. The inductor-less approach made the LNA design compact and power efficient.

2 The active inductor based LNA

In LNA design, CGLNA is preferred for its excellent input impedance matching characteristics [14]. The conventional common gate amplifiers commonly utilize resistive feedback which experiences parasitic capacitance effect and relatively higher power dissipation at higher frequencies. The proposed LNA is structured in three interconnected modules, as illustrated in Fig. 3, Common gate amplifier, Active inductor and Common drain amplifier. The signal will first pass through a common gate amplifier and then to the active inductor and lastly into a common drain amplifier which will act as a buffer.

Figure 3: Modules of the active inductor based LNA.

2.1 Common Gate Amplifier

The proposed circuit of a common gate amplifier is shown in Fig. 4. Here, M11 acts as an active resistor instead of source resistor. The transconductance of the transistor M8 is the input impedance of the amplifier. The common gate amplifier topology is a good choice because of its high reverse isolation and good impedance matching characteristics and thus any extra impedance matching network is not required. Biasing voltage (V2) is applied to make sure that the transistor M8 is always in saturation mode.

2.2 Active Inductor

A double feedback active inductor used in the proposed LNA is shown in Fig. 5 [15].

The negative feedback action involves the long tail pair transconductor consisting of transistors M3, M_4 and sources J_2, J_3 whereas the source J_4 converts the input voltage to a current for the internal capacitor of transistor M2, c_{gs2} to be charged. While the transistor M_2 converts back the capacitor voltage to the input current. For positive feedback action, the long-tail

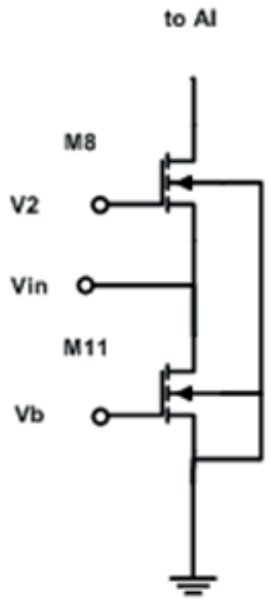

Figure 4: Common gate amplifier.

pair transconductor converts the input voltage into an oppositely directed current which enters the input node. It realizes a negative resistance of $-2/g_{m3}$ (where $g_{m3} = g_{m4}$) that is parallely tied with the inductor. For the proposed topology, the currents in the unwanted coupling routes have been balanced. For a voltage applied at the input of the inductor, the currents

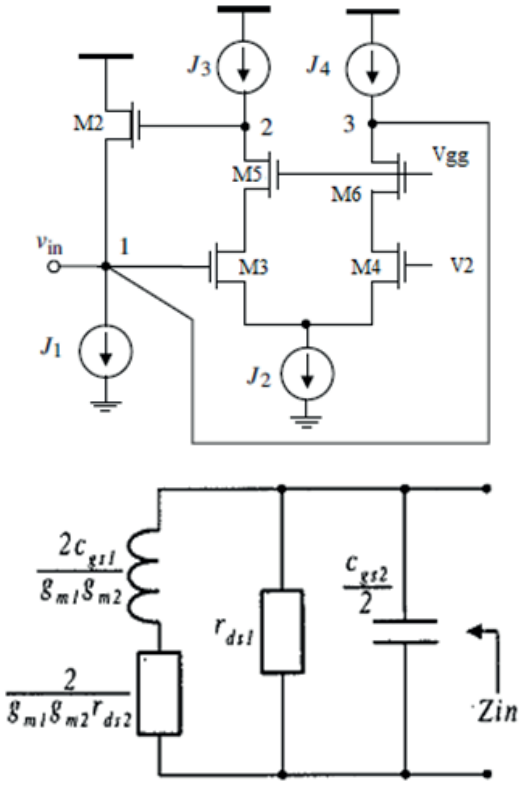

Figure 5: Double feedback active inductor and its equivalent circuit [15].

through c_{gs2} and c_{gs3} are combined at the common-source terminals of M3 and M4 which acts as virtual ground potential. This current follows the drain of the transistor M4 as the current flowing through c_{gs4} is insignificant because of the almost zero signal voltage across it. Consequently, the currents through the unwanted coupling paths are counterbalanced and therefore, the drain current of M_1 makes the input current and the inductor loss is taken out.

The Q-enhancement technique is applied in almost all modern on-chip inductor circuits in order to compensate their high losses. Generally, the Q factor of the regulated cascode active inductor circuit is relatively low because of its equivalent parallel resistive loss which is not compensated by the negative feedback operation. Therefore, in our proposed circuit, the currents in the undesirable coupling paths have been compensated. For an input voltage to the inductor, the currents flowing through cgsl and cgs2 are summed at the common-source terminals of M2 and M3 which exhibit virtual ground potential. This current will then flow out of the drain terminal of M3 because the current in cgs3 is negligible since the signal voltage across it is almost zero. Moreover, from the first-order small-signal analysis, it is evident that, if gm3 = gm2 and cg3 = cgs2, the active inductor will become lossless (infinite Q). But in practice, it is not possible for some factors like finite drain-source resistances, other parasitic capacitances of the transistors etc.

2.3 Common Drain Amplifier

The common drain amplifier is also known as source follower or a buffer. It is widely utilized in final stage of LNA design due its small output impedance to achieve a better output impedance matching for the LNA. A simple buffer is added to the final stage of the proposed LNA design. Its schematic is shown in Fig. 6 and transistor M9 is used as active resistor. Transistor M10 is used as a common drain amplifier.

2.4 Proposed Active Inductor Based LNA

Finally, all three sub-circuits are tied together and the whole schematic circuit of the proposed LNA is shown in Fig. 7. In this circuit, the enhanced active inductor has been formed by transistors M3 to M6. The common gate amplifier is formed by transistor M8. On the other hand, M0, M1 and M7 act as constant current source. Finally, M9 and M10 comprise the output buffer.

It is obvious that amplifiers add noise and distortion to the desired signal. Therefore, noise analysis is very important for every amplifier circuit. The noise figure gives a measure of the amount of noise added to a

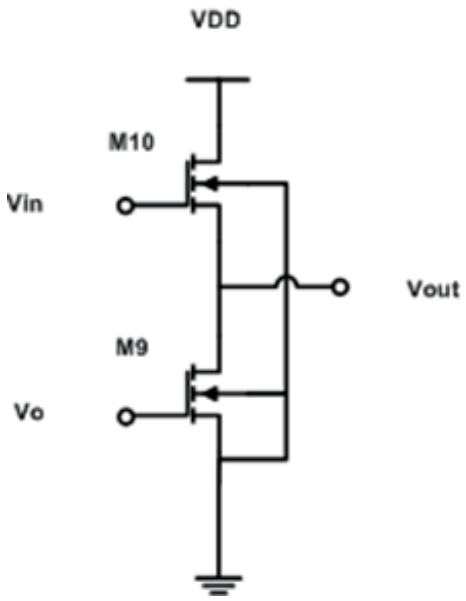

Figure 6: Common drain amplifier.

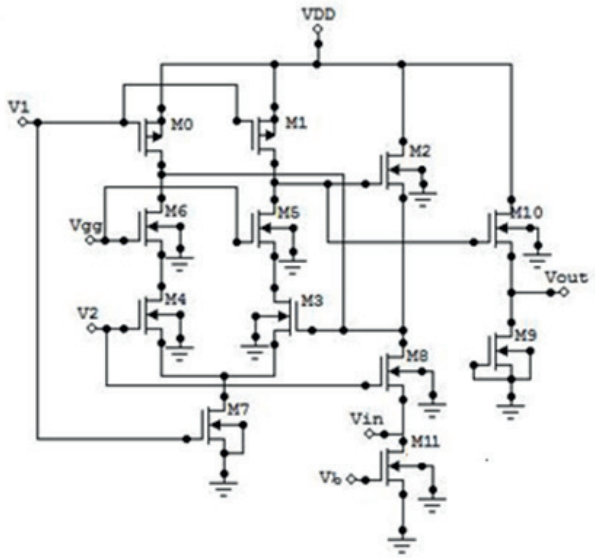

Figure 7: Schematic of the active inductor based LNA.

signal transmitted through the network. For any circuit, therefore, the noise figure minimization is also very important. But it is also inevitable that maximum gain and minimum noise cannot be obtained at the same time.

For the noise analysis of the active inductor, let us consider that it is terminated with a resistance, R, the value of which is greater than (1/gm1) and also neglecting the flicker noise of the transistors used, the spot noise figure can be approximately expressed as:

$$NF \approx 10\log\left[1+\frac{2}{3r}\left(\frac{1}{gm2}+\frac{1}{gm3}+\frac{1}{gm4}+\frac{gm5}{gm3^2}\right)\right] \quad (1)$$

It can be seen from (1) that the noise figure of the inductor can be minimised by maximising the small-signal transconductances of M2, M3 and M4 while the transconductances of M5 and M6 should be kept at minimum values. Increasing the transconductances of M2, M3 and M4 corresponds to the increasing of parasitic capacitances hence a trade-off between noise performance and frequency response. On the other hand, reducing the transconductances of M5 and M6 seems to be not a critical problem in compromising the performance since they serve as just current followers.

Generally, the noise effects in a common-gate topology include both the thermal and the flicker noise. Thus, the noise factor of the common-gate amplifier can be approximately showed as

$$NF \approx \frac{K}{C.f}\left(\frac{gm1\,1^2+gm8^2}{(WL)m8}+2\frac{gm2^2}{(WL)m2}\right)+ \\ +\ \frac{2}{3}\left(\frac{gm1\,1^2+gm8^2}{(WL)m8}+2\frac{gm1\,1+gm8+2gm2}{gm8^2}\right) \quad (2)$$

where K is a process-dependent constant, C is the gate capacitance of the MOSs, and f is the operating frequency of the amplifier.

The final stage is the common-drain configuration which is nothing but a source follower. The noise factor of this stage is derived as:

$$NF \approx \frac{2}{3}\left(\frac{1}{gm10}+\frac{1}{gm10^2.R}\right) \quad (3)$$

Where R is the resistance of the active resistor (M9).

If we consider all the transconductances (gm) same, it will be obvious that a higher value of gm can improve the noise figure but it will also increase the total power consumption. Moreover, the increased parasitic capacitances of the transistors will degrade the performance specially in high frequencies. Therefore, a trade off has been made.

3 Results and discussion

The proposed LNA circuit has been verified by using the simulation tool ELDO RF in Mentor Graphics environment. The process parameters for the transistors used in this work correspond to Silterra 130-nm CMOS technology. The power supply for the circuit is 1.2V.

The operating temperature of the circuit is 300K while the noise temperature is set to 290K for measuring the LNA noise figure. The voltage biases for the LNA are V1=0.59V, V2=0.40V and Vgg =0.79V. The transistor sizes are given in Table I.

Table 1: Components used in the LNA circuit

Transistor	Width (μm)	Length (μm)
M0, M1	1.27	0.13
M2	0.84	0.13
M3, M4	9.11	0.13
M5,M6	0.36	0.13
M7	12.15	0.13
M8	3.66	0.13
M9	25	0.13
M10	4.58	0.13
M11	8	0.13

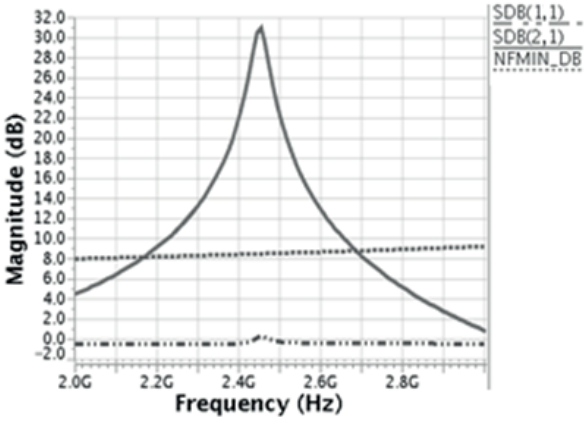

Figure 8: Gain (S21), reflection coefficient (S11) and minimum NF.

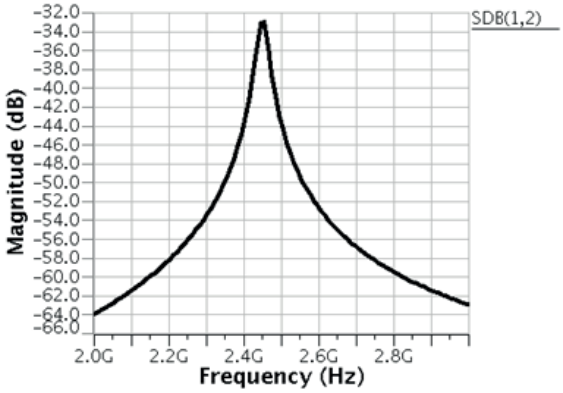

Figure 9: Simulation result for reverse isolation (S12).

The simulation results are shown in Fig. 8 and Fig. 9. At the center frequency of 2.45GHz, the LNA is able achieve 33dB of forward gain (S_{21}) and a minimum noise figure (NF) of 8.51dB. The reverse isolation (S_{12}) is -33.1dB whereas the reflection coefficient (S_{11}) is 0.2dB. The power dissipation of the LNA is measured to be 1.51mW. The IIP3 is measured to be 35.5dB. The bandwidth of the proposed LNA is 28 MHz. The transient output voltage is shown in Fig. 10.

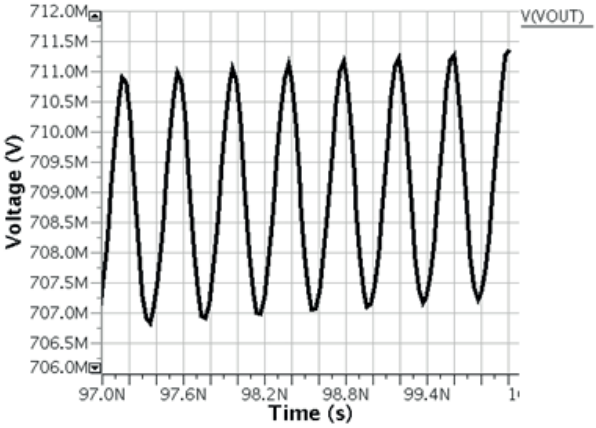

Figure 10: The transient output voltage waveform.

A transistor (M11) commonly seen to be used with the CG topology to stabilize the transconductance of the amplifying transistor is removed. The existence of that transistor shows no significant effect on the LNA performance during the simulation. The bias voltage for transistor M9 is best when it is grounded. By grounding the bias voltage of transistor M9, no changes on the center frequency is observed. However, an improvement in the LNA gain is observed.

All of the transistors are operating at saturation region except for transistor M9. By changing the transistor width of M2, M3, M4, M8 and M10, the LNA center frequency, gain and minimum NF can be tuned. However, the higher the center frequency, the lower the gain is. It is also observed that the minimum NF increases as the gain increases. But, the gain increases steeper than the minimum NF. The transistor widths are tuned to achieve maximum gain while maintaining an acceptable minimum NF.

The layout of the LNA is designed using Mentor Graphics IC Design environment. The transistor sizes are optimized to obtain a balance between chip area and performance. The transistors are positioned in such a way that it is as compact as possible to achieve a small chip area which is measured at 0.0004 mm^2. The layout of the LNA is shown in Fig. 11.

The proposed active inductor based LNA is compared with other previously published active inductor based LNA design in Table II. This work has the highest gain and lowest power consumption while also being the smallest LNA. It also shows better linearity as evident

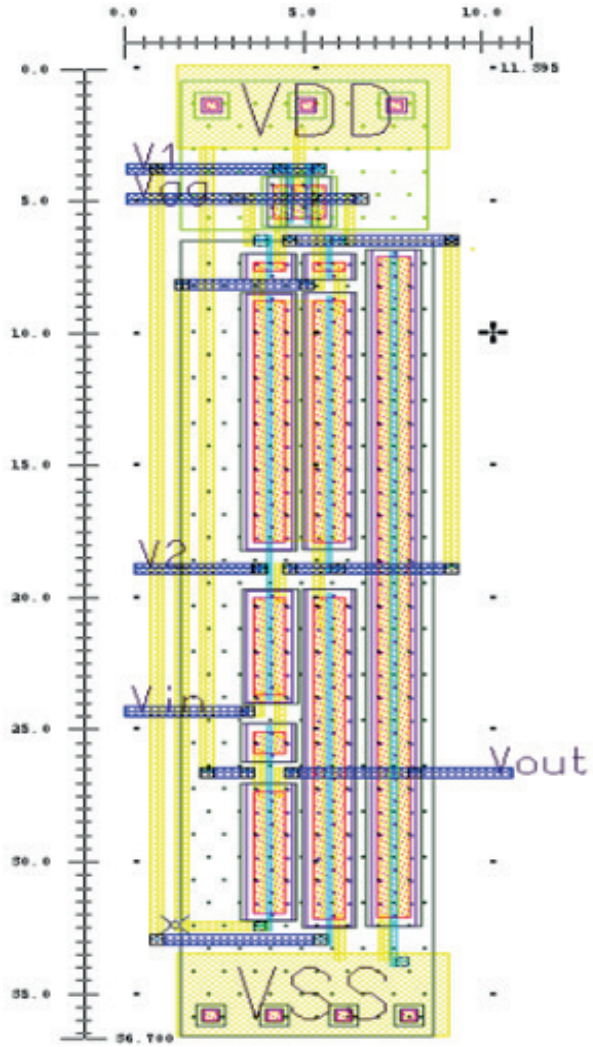

Figure 11: The core layout of the LNA (11.9 x 36.7) mm^2

from iip3 value. The low power consumption is due to the fact that less number of MOSFETs used in the design and the lower supply voltage when compared with other works. However, this work suffers from relatively higher noise figure due to the simple common gate topology used for the amplification and also for using smaller sized transistors.

Table 2: Performance comparison

	This work	[16]	[17]	[18]	[19]	[20]	[21]
Gain, S_{21} (dB)	30.7	11.2	22	14	11.8	19	15
Frequency (GHz)	2.45	2.0-11.2	0.8-2.5	0.37- 2.18	2.3-15.2	1-5	3.2-6.3
Noise Figure (dB)	8.51	2.0-4.0	3.02	3.55-4.5	1.9-3.8	2.1	0.95
Power Consumption (mW)	1.51	13.5	19.6	14.58	13.3	4.2	4.7
IIP3(dB)	35.5	-	-	-10	-	-	-
Supply Voltage	1.2	1.2	1.8	1.8	1.2	1.2	1.8
CMOS Process (nm)	130	130	180	180	130	180	180
Chip Area (mm2)	0.0004	0.09	0.03	0.04	0.093	-	-

4 Conclusion

In this paper, a low power compact design of LNA is proposed using Silterra 130-nm CMOS technology. It exhibits high forward gain (S_{21}) of 33dB, high reverse isolation (S_{12}) of -33.1 dB and high IIP3 of 35.5 dB at 2.45GHz. The LNA operates at supply voltage of 1.2V and consumes only 1.51mW of power. However, the LNA shows a competative NF of 8.51dB. In this design passive spiral inductors are avoided to keep the size very small at 0.0004 mm^2. Such an LNA will be suitable for high performance, fully integrated, low cost and low power RF receivers.

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