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Voltage-mode analog PID controller using a single z-copy current follower transconductance amplifier (ZC-CFTA)

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Abstract: This paper endeavours to design a proportional-integral-derivative (PID) controller based on the use of single z-copy current follower transconductance amplifier (ZC-CFTA). The developed PID controller consists of one ZC-CFTA, two truly grounded passive components and virtually grounded passive components. It does not require any passive component matching, and the realized controller parameters are adjustable electronically. The effects of parasitic elements and tracking errors of the ZC-CFTA are also investigated. Simulation results in PSPICE demonstrate the workability of the proposed PID controller.

Keywords: z-copy current follower transconductance amplifier (ZC-CFTA); proportional-integral-derivative (PID); analog controller; voltage-mode circuit

Analogni PID krmilnik v napetostnem režimu realiziran z enim dvo-izhodnim tokovnim sledilnikom, povezanim s transkonduktančnim ojačevalnikom (ZC-CFTA)

Izvleček: V tem članku si prizadevamo zasnovati proporcionalno-integralno-diferencialni (PID) krmilnik na osnovi enega samega dvo-izhodnega tokovnega sledilnika, povezanega s transkonduktančnim ojačevalnikom (ZC-CFTA). Razviti PID krmilnik je sestavljen iz enega ZC-CFTA, dveh zares ozemljenih pasivnih komponent in dveh navidezno ozemljenih pasivnih komponent. Parametri realiziranega krmilnika so elektronsko nastavljivi in ujemanje pasivnih komponent ni potrebno. Raziskani so tudi efekti parazitnih elementov in napake sledenja ZC-CFTA. Rezultati simulacij v PSPICE-u pokažejo izvedljivost predlaganega PID krmilnika.

Ključne besede: dvo-izhodni tokovni sledilnik, povezan s transkonduktančnim ojačevalnikom (ZC-CFTA); proporcionalni-integralni-diferencialni (PID) krmilnik; analogni krmilnik; vezje v napetostnem režimu

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1 Introduction

The ubiquitous proportional-integral-derivative (PID) controllers are the most widely-used controllers in process industries, and gained widespread industrial acceptance for many decades [1]. This is owing to the attribute that they offer many good features, such as simplicity of design, low cost, robustness and wide applicability, as well as easy tunability of their parameters [2]. The enormous literature on PID process controllers includes a wide variety of design approaches based on different high-performance active elements, such as operational transconductance amplifiers (OTAs) [3], current differencing buffered amplifiers (CDBAs) [4], current-controlled current conveyors (CCCIIs) [5], second-generation current conveyors (CCIIs) [6]-[8], and current feedback operational amplifiers (CFOAs) [9]. In [3]-[5], the signal flow graph synthesis procedures for realizing analog PID controllers were presented. In active circuit realizations, they contain too many active

and passive components. The CCII can also be applied to construct PID process controllers, as demonstrated in [6]-[8]. However, at least two CCIIs and five passive components are required for these realizations. The work in [9] proposed a PID controller using a single CFOA. Although the circuit employs only one active component, it does not exhibit the feature of electronic tuning, and the passive components used in its construction are floating.

In 2008, the conception of the z-copy current follower transconductance amplifier (ZC-CFTA) has been introduced [10]. This device is a modified version of the conventional current differencing transconductance amplifier (CDTA) [11] by replacing the current differencing unit with a current follower and complementing the circuit with a simple current mirror for copying the z-terminal current. Therefore, the ZC-CFTA element is a cascade connection of the dual-output current follower and the operational transconductance amplifier. As a result, the capability of applications based on ZC-CFTAs is extended [12]-[14].

Our purpose in this study is to present an alternative circuit configuration for realizing an analog voltage-mode PID controller based on the use of the ZC-CFTA as an active element. The configuration uses only one ZC-CFTA, cooperating with four grounded passive elements, i.e. two truly grounded passive components and two virtually grounded passive components. The circuit also does not need passive element matching. Three realized parameters of the presented PID controller can be tuned to the desired valued by the transconductance (g_m) of the ZC-CFTA. In addition, the ZC-CFTA non-ideality effects including finite parasitic elements and transfer errors on the controller behavior are examined in detail. Also, PSPICE simulations are performed to demonstrate the performance of the presented controller circuit, and to verify the theoretical expectations.

2 ZC-CFTA Principle and Realization

The ZC-CFTA is a versatile active circuit building block, which is made by the cascade connection of two essential circuit blocks, i.e. a dual-output current follower at the front end, and an operational transconductance amplifier at the rear end. Fig.1 shows the electrical symbol and equivalent circuit of the ZC-CFTA. As shown in Fig.1, this device consists of a low-input-impedance current terminal (f) and three high-output-impedance current terminals (z, zc and x). The characteristic of an ideal ZC-CFTA can be represented by the following expression [12]-[14] :

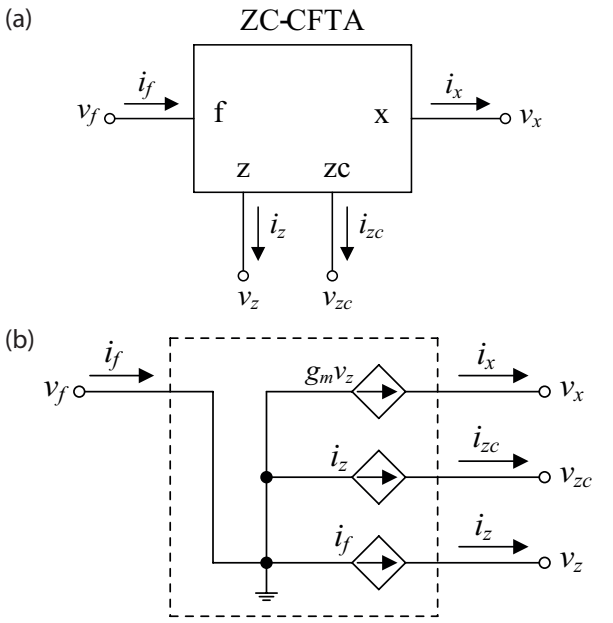

Figure 1: The ZC-CFTA.
(a) circuit symbol, (b) equivalent circuit.

$$i_{zc} = i_z = i_f \text{ and } i_x = g_m v_z \quad (1)$$

where g_m denotes the small-signal transconductance gain of the ZC-CFTA. In general, the value of g_m depends on the external supplied current.

The possible BiCMOS implementation of the ZC-CFTA used in this work is illustrated in Fig.2. Transistors Q_1-Q_7 act as a dual-output current follower that follows an input signal current (i_f) to output currents flowing through terminals z and zc (i_z and i_{zc}). Group of transistors Q_8-Q_{14} functions as an operational transconductance amplifier, which converts the impressed voltage at terminal z into the signal current at terminal x (i_x) by the transconductance g_m. From small-signal circuit analysis of this structure, the transconductance value g_m depends on an external biasing current I_O, and can be expressed as [14] :

$$g_m = \frac{I_O}{2V_T} \quad (2)$$

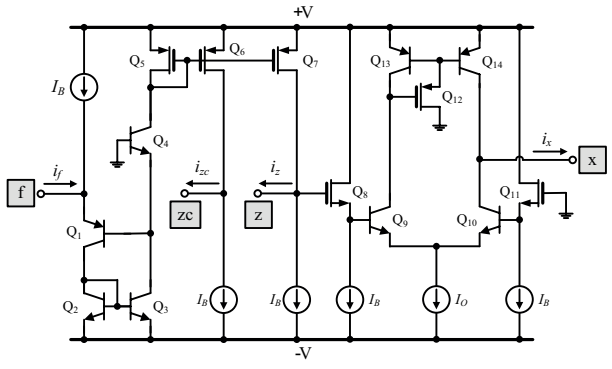

Figure 2: BiCMOS realization of the ZC-CFTA.

In addition, V_T is the usual thermal voltage, approximately 26mV at 27°C.

3 Proposed PID Controller Realization

The circuit implementation of the PID controller based on the use of the ZC-CFTA as an active component is shown in Fig.3. As can be seen, the proposed controller comprises one ZC-CFTA, two virtually grounded passive components (R_1 and C_1), and two truly grounded passive components (R_2 and C_2). These grounded passive elements can compensate for the parasitic impedances at their corresponding nodes. The circuit analysis of the proposed PID controller circuit in Fig.3 yields the following voltage transfer function :

$$\frac{V_{out}(s)}{V_{in}(s)}=\left(\frac{R_2}{R_1}+\frac{g_m R_2 C_1}{C_2}\right)+\frac{g_m R_2}{sR_1C_2}+sR_2C_1 \qquad (3)$$

In general, the voltage transfer function of an analog PID controller can be expressed as [15] :

$$\frac{V_{out}(s)}{V_{in}(s)}=K_p+\frac{1}{sT_i}+sT_d \qquad (4)$$

where K_p is the proportional gain, T_i is the integral time constant and T_d is the derivative time constant. Therefore, by comparing eq.(3) with eq.(4), the three parameters of the realized PID controller in Fig.3 are found out to be :

$$K_p=R_2\left(\frac{1}{R_1}+\frac{g_m C_1}{C_2}\right) \qquad (5a)$$

$$T_i=\frac{R_1C_2}{g_m R_2} \qquad (5b)$$

And

$$T_d=R_2C_1 \qquad (5c)$$

From eq.(5), the above three coefficients can be adjusted by appropriately setting the values of R_1, R_2, C_1, C_2 and g_m. It is further to be noted that the g_m-value can be used as a tool to tune the controller parameters for compensating the deviation from the ZC-CFTA non-ideality or the errors in passive component values.

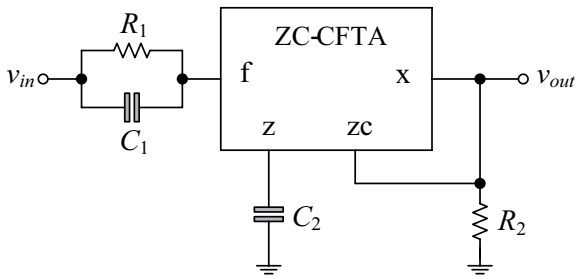

Figure 3: Proposed PID controller realization.

4 Non-ideal Performance Analyses

4.1 Tracking Error Effects

In non-ideal case, the current transfer from terminal f to terminals z and zc, as well as, the current at terminal x may differ from ideal values due to the current tracking error, and transconductance inaccuracy. Considering these errors, the terminal relationships of the non-ideal ZC-CFTA can be rewritten by :

$$i_{zc}=i_z=\alpha i_f \text{ and } i_x=\beta g_m v_z \qquad (6)$$

where α is the current tracking error, and β is the transconductance inaccuracy parameter. By repeating the analysis of the proposed PID controller circuit in Fig.3 and taking into account the parameters α and β of the ZC-CFTA, the controller parameters K_p, T_i and T_d can be obtained as :

$$K_p=\alpha R_2\left(\frac{1}{R_1}+\frac{\beta g_m C_1}{C_2}\right) \qquad (7a)$$

$$T_i=\frac{R_1C_2}{\alpha\beta g_m R_2} \qquad (7b)$$

And

$$T_d=\alpha R_2C_1 \qquad (7c)$$

As can be seen from eq.(7), the values of all PID controller parameters are slightly altered by the influences of the ZC-CFTA current tracking error and transconductance inaccuracy. To compensate for these small deviations, the g_m-parameter can be tuned by means of the ZC-CFTA bias current (I_O). On the other hand, if the controlled-gain current follower transconductance amplifier introduced in [16] is employed instead of the ZC-CFTA in Fig.3, the parameters α and β can be tuned by the controllable transfer gains to obtain the desired K_p, T_i and T_d values, or to compensate for the small errors that occur in their values. The inspection of eq.(7) indicates that the relative sensitivities of the three controller parameters with respect to the active and passive component values are found within unity in magnitude. In consequence, this controller circuit possesses low sensitivity performance.

4.2 Parasitic Element Effects

The practical model of the ZC-CFTA including essential parasitic elements is shown in Fig.4. As it is shown, the f-terminal exhibits the low-value serial parasitic resistance R_f and the z, zc and x-terminals exhibit large parasitic resistances R_z, R_{zc}, and R_x in parallel with low-value parasitic capacitances C_z, C_{zc} and C_x, respectively. When the circuit in Fig.3 is re-considered by taking the mentioned parasitic elements into account, the following assumptions can be made.

(a) Since the z-terminal is terminated by the external capacitor C_2, an extra parasitic pole ω_1 is introduced by R_z and C_2 (assuming $C_2 >> C_z$) at low frequencies, namely $\omega_1 \cong 1/R_zC_2$. For close to ideal operation at low frequencies, the operating frequency should be selected 10 times higher than ω_1. Thus, the low-frequency range of the proposed controller can be approximated as :

$$\omega \geq 10\omega_1 \cong \omega_L \tag{8}$$

(b) The external grounded resistor R_2 is connected in parallel with the parasitic impedances ($R_{zc}//C_{zc}$) and ($R_x//C_x$) of terminals zc and x. The extra pole ω_2, which is approximately equal to $\omega_2 = 1/(R_2//R_{zc}//R_x)(C_{zc}//C_x)$, appears only the high-frequency region of characteristic. Usually $R_2 << R_{zc}//R_x$, the pole ω_2 is located at about $\omega_2 \cong 1/R_2(C_{zc}//C_x)$. Thus, to obtain ideal response, the maximum operating frequency of the controller should be chosen as :

$$\omega \leq 0.1\omega_2 \cong \omega_H \tag{9}$$

(c) In conclusion, combining eqs.(8) and (9), the useful frequency range of the proposed PID controller circuit in Fig.3 can be defined simply as :

$$\omega_L \leq \omega \leq \omega_H \tag{10}$$

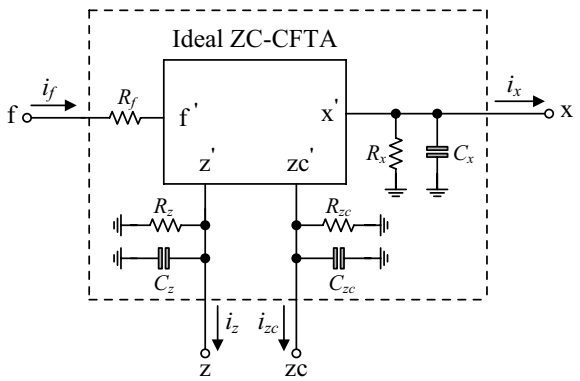

Figure 4: Non-ideal ZC-CFTA model including essential parasitic elements**.**

5 Simulation and Comparison of the Results

The performance of the proposed PID controller circuit in Fig.3 has been evaluated by means of PSPICE simulation. In simulations, the ZC-CFTA structure given in Fig.2 was characterized by 0.35-μm real BiCMOS process parameters. Transistor aspect ratios (W/L in μm/μm) were 7/0.35 and 14/0.35 for all the NMOS and PMOS transistors respectively. The circuit was biased with the following conditions: ±V = 1 V and I_B = 50 μA.

For our design example, the following active and passive component values were chosen: g_m = 1 mA/V (I_O = 52 μA), $R_1 = R_2$ = 1 kΩ and $C_1 = C_2$ = 1 nF. In this setting, the corresponding controller parameters were obtained as: K_p = 2, $T_i = 10^{-6}$ s and $T_d = 10^{-6}$ s. The total power consumption of the proposed controller is measured as approximately 23.7 mW. Fig.5 shows the ideal and the simulated frequency responses of the proposed PID controller circuit in Fig.3. As can be seen from the results, the ideal values and the simulation results are in agreement between 150 Hz and 1 MHz. It should be noted that the differences between the two responses in low- and high-frequency regions can be attributed to two extra parasitic poles ω_1 and ω_2, respectively.

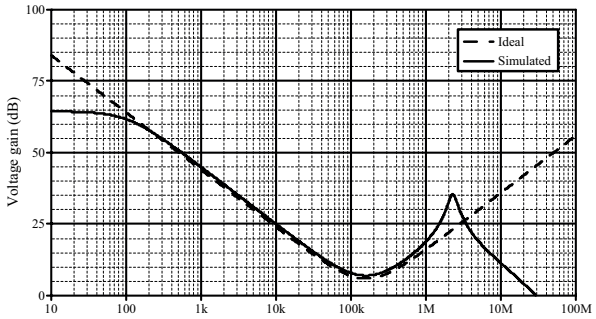

Figure 5: Ideal and simulated frequency responses of the proposed PID controller configuration of Figure 3.

To illustrate the time-domain characteristic of the proposed PID controller circuit, a 50-mV step signal voltage with 100-ns rise time is applied to the input of the circuit. Both ideal and simulated output voltage responses v_{out} are shown in Fig.6. From this result, an overall proportional action of the controller is obvious in the 0-100 ns period. At 100 ns, the sudden decrease in the controller output is due to the derivative action, since the input signal of the controller changes at a faster rate. After 100 ns, the action of the integral control mode is introduced. The controller output increases almost linearly since there is no change in the input for this period of time. As previously mentioned, the discrepancy between the ideal and the simulated results can be attributed to the parasitic impedances

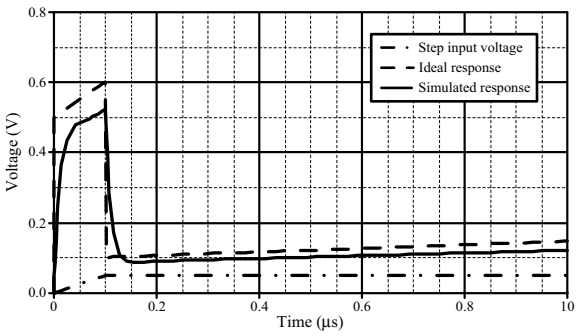

Figure 6: Step responses of the proposed PID controller configuration of Fig.3.

of the ZC-CFTA, most notably the finite port resistances R_z, R_{zc} and R_x.

6 Conclusions

In this paper, a simplified structure of the PID controller with single ZC-CFTA is introduced. The introduced PID controller has been realized using a minimum number of passive components, without requiring a passive component-matching constraint. The controller gains are adjustable by tuning the g_m-value of the ZC-CFTA. The effects caused by the parasitic elements and the transfer errors of the ZC-CFTA are also discussed. Simulation results confirm the theoretical analysis.

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