High -Frequency Tunable Grounded and Floating Incremental-Decremental Meminductor Emulators and its application as AM Modulator

Garima Shukla[1], Pratik Kumar[2], Sajal K Paul[1]

[1]Department of Electronics Engineering, Indian Institute of Technology (ISM), Dhanbad, Jhakhand, India
[2]Centre for Nano Science and Engineering, Indian Institute of Science, Bangalore, India

Abstract: This paper proposes new design for realizing grounded and floating meminductor emulators built with two operational transconductance amplifiers (OTAs) and two second-generation current conveyors. The proposed grounded and floating emulators claim that the circuits are much simpler in design and can be utilized in incremental and decremental topologies. The proposed circuits' performance has been verified with Cadence Virtuoso Spectre using standard CMOS 180nm technology. Furthermore, the layout of the proposed circuits has been designed, and post-layout simulations have been performed. The non-ideal and Monte Carlo analyses have been carried out in detail. This paper also proposes the application of a meminductor as an Amplitude Modulator (AM). Moreover, the experimental results are presented to verify the theoretical and simulation analyses of proposed meminductor emulator circuits.

Keywords: Current-mode circuits, Floating meminductor emulator, Grounded meminductor emulator, Incremental configuration, Decremental configuration, Pinched hysteresis loop

Visokofrekvenčni nastavljivi ozemljeni in plavajoči inkrementalno-dekrementalni meminduktorski emulatorji in njihova uporaba kot AM modulator

Izvleček: V članku je predlagana nova zasnova ozemljenih in plavajočih emulatorjev meminduktorjev, ki so zgrajeni iz dveh operacijskih transkondutančnih ojačevalnikov (OTA) in dveh tokovnih transporterjev druge generacije. Predlagani ozemljeni in plavajoči emulatorji omogočajo, da so vezja veliko enostavnejša pri načrtovanju in jih je mogoče uporabiti v inkrementalnih in dekrementalnih topologijah. Delovanje predlaganih vezij je bilo preverjeno s programom Cadence Virtuoso Spectre z uporabo standardne CMOS 180 nm tehnologije. Poleg tega je bila zasnovana postavitev predlaganih vezij. Podrobno so bile izvedene neidealne analize in analize Monte Carlo. V članku je predlagana tudi uporaba meminduktorja kot amplitudnega modulatorja (AM). Poleg tega so predstavljeni eksperimentalni rezultati za preverjanje teoretičnih in simulacijskih analiz predlaganih vezij emulatorja meminduktorja.

Ključne besede: tokovna vezja, emulator plavajočega meminduktorja, emulator ozemljenega meminduktorja, inkrementalna konfiguracija, dekrementalna konfiguracija, zanka s stisnjeno histerezo

* Corresponding Author's e-mail: garima29shukla@gmail.com

1 Introduction

Resistor, inductor, and capacitor were three traditional fundamental basic electrical elements; now, the memristor represents the fourth fundamental element. Chua postulated the memristor in 1971 [1] as the fourth ba- sic electrical element. In 1980 this postulation was then generalized to an infinite variety of basic circuit elements [2] and can be generalized into elements quadrangle. It was highlighted only after 2008 when HP fabricated a memristor based on thin-film TiO_2. From then onward, there has been a boom of research in this field.

Chua's circuit 4 element diagram was then extended to propose higher-order elements (which require two or more than two capacitors), such as memcapacitors (MCs) and meminductors (MLs). The meminductor provides a relationship between the charge q and the time integral of flux ρ. Unlike capacitors and inductors, meminductors can store information for a long time without power because of their non-volatility. Although the device is still a theoretical concept, some device-level memelements (mostly memristors) have been fabricated [3], and hence emulators are essential to analyze the characteristics and study their applications. The research on solid-state memelements is yet to mature completely, especially for MCs and MLs. Solid-state MCs have not been commercialized, and there has been no information on solid-state MLs. Some models, though directly labeled as "memristors" or "memcapacitors," are essentially practical memrestive emulators [3]. Therefore, a substantial number of circuit implementations have been proposed through the use of emulators. In [4], a relationship on the doubly periodic table of 4 element diagram, also called the four elements torus, is given in correlation with the basic circuit element quadrangle of all four basic electrical elements. Furthermore, an extension of the memristive system to capacitive and inductive elements whose properties depend on the state and history of the system is presented in [5]. Physical characteristics analysis of these memory-based elements and mathematical examples for memristors, meminductors, and memcapacitors are presented in [6, 7].

Several circuits for emulating memristor-less meminductors are proposed in [8-23], while meminductors formed using mutators are proposed in [24-28]. In [8], a memristor-less current and voltage-controlled meminductor emulator are reported using a second-generation current conveyor (CCII), adder, multiplier, and several passive components in the count. A charge-controlled meminductor emulator using an inductor, op-amps, multiplier, transistors, and several other passive components is reported in [9]. In 2014, a practical implementation of the meminductor using many active and passive components was reported [10]. It consists of four current feedback operational amplifiers (CFOAs), one buffer, two op-amps, one multiplier, and some passive components making the circuit quite complex and bulky. A flux-controlled meminductor is reported in [11] but consists of many active blocks and passive components. The meminductor reported in [12] is based on six op-amps and one multiplier, whereas the design in [13] employs three CFOAs, one op-amp, one operational transconductance amplifier (OTA), and one multiplier. The design reported in [14] is based on two voltage differencing transconductance amplifiers (VDTAs) and one multiplier. In 2017, a much simpler cir-

cuit for emulating a meminductor was reported using multioutput OTA [15], but it uses an inductor and has a low frequency of operation. All the reported circuits in [8-14] are complex as they employ a multiplier along with an excessive number of active blocks, and [15] has a low frequency of operation, which very much limits the practical use and, further, it realizes only grounded meminductor. The meminductor design in [16] is based on three OTAs and two capacitors. The design reported in [17] is based on two OTAs and one differential voltage current conveyor (DVCC), and the design in [18] is based on one OTA and one VDTA. The topology in [19] reports a meminductor employing two OTAs and one current differencing buffered amplifier (CDBA), whereas [20] is based on two OTAs and one current differencing transconductance amplifier (CDTA). Meminductor design in [21] employs two CCIIs and one OTA, whereas design [22] is based on two VDTAs. Moreover, [23] reports a design based on one modified voltage differencing current conveyor (MVDCC) and one OTA. However, all the designs reported in [8-12, 15-18, 20-23] realize only one type of meminductance emulator, i.e., the grounded or floating meminductor; only [19] realizes both grounded and floating meminductance emulator. Furthermore, the designs reported in [21-23] realize only one type of meminductance emulator and possess a low frequency of operation. Moreover, [22, 23] realize only the incremental type of configuration.

Another method of emulating meminductors is with mutators proposed in [24-28]. Mutators simulating second-order elements using their inherent relationship are reported in [24, 25] and represent the simplified meminductor emulator using the multiplier approach, but the memristor used here is bulky, complex, and has a low operating frequency. A mutator based on one CCII and three op-amps is reported in [26]. A universal mutator using many active and passive components is also available in [27]. Moreover, a mutator circuit based on two current buffered transconductance amplifiers (CBTAs) and one multiplier is reported in [28]. Apart from these mutators, the PSpice model of meminductor and its nonlinear model with its study on device parameter variations are available in [29, 30]. A detailed composite behavior in series and parallel meminductor topologies is reported in [31]. The applications of meminductors in chaotic oscillators and their dynamic studies are reported in [32-34], whereas application as a low-power filter design is available in [35].

This paper proposes two meminductor emulators, one grounded and other one floating, built with active blocks consisting of two OTAs and two-second generation current conveyors. The proposed meminductor emulators possess the following important features: (i) simple circuitry with no multipliers, (ii) option for both

incremental and decremental configurations to increase the range of values of meminductance (the value of meminductance can be increased and decreased from its base value in incremental and decremental types of topology respectively), and also application flexibility, (iii) high-frequency range of operation, (iv) electronic control of meminductance value in addition to the control by frequency and amplitude of the applied voltage signal across the emulator.

2 Employed analog building blocks and general meminductor model

Employed analog building blocks in proposed meminductor emulator circuits and a generalized model of a meminductive system are illustrated in this section.

2.1 Operational transconductance amplifier (OTA), second generation current conveyor (CCII) and cecond-generation current controlled current conveyor (CCCII)

OTA, CCII, and CCCII circuit symbols are shown in Figure. 1(a)-(c). CMOS implementation of OTA, CCII and CCCII are presented in Figure. 1(d), 1(e) and 1(f) respectively. V_B controls the OTA's transconductance gain (G_m), while I_b controls the internal resistance R_X of CCCII, making the circuits electronically tunable.

The port relationships of OTA are expressed as:

$I_{o\pm} = \pm G_m V_{in}$, $V_{in+} - V_{in-}$ = differential input = V_{in}

Where G_m is the transconductance of OTA. The routine analysis results in the following expression for G_m:

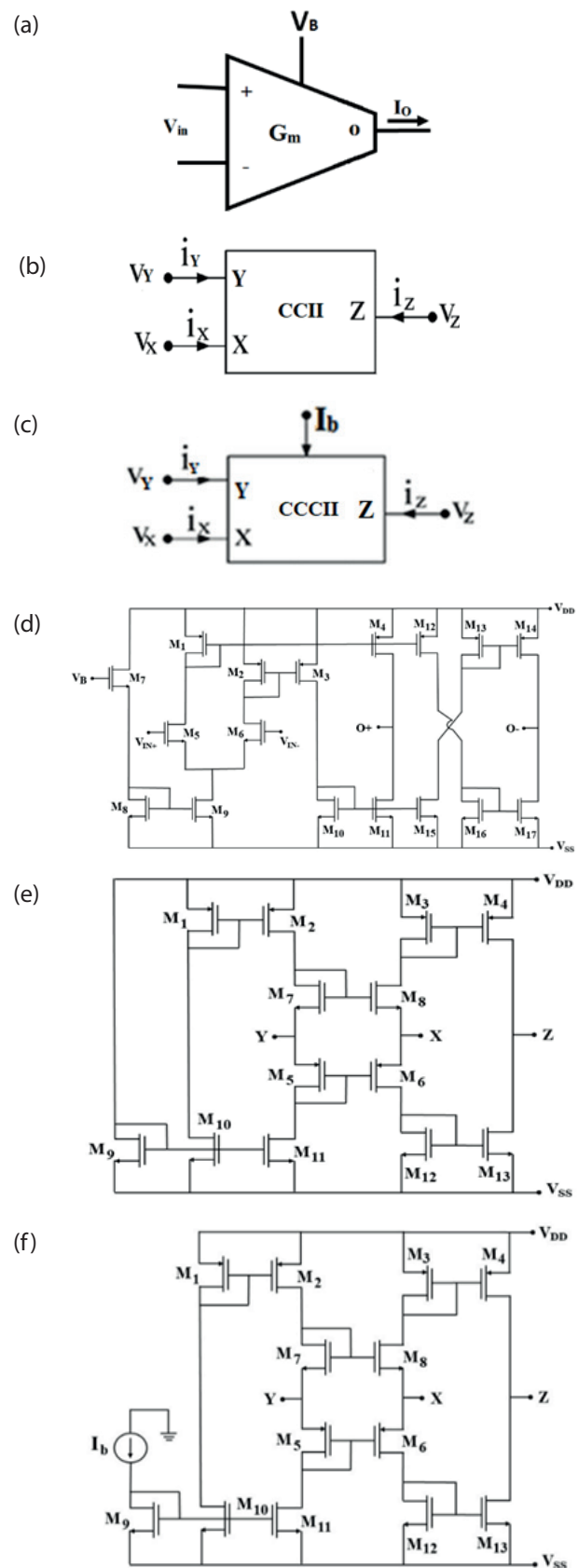$$G_m = \frac{k}{\sqrt{2}} \left(V_B - V_{ss} - 2V_{th} \right),\qquad(1)$$

Here, k is a parameter of the MOS device given by:

$$k = \mu_n C_{ox} \frac{W}{L}$$

The W, L, μ_n, C_{ox}, and V_{th} are, respectively, channel width, length, the mobility of the carrier, capacitance per unit area, and the threshold voltage of MOS.
The port relationship CCII± is given by:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$
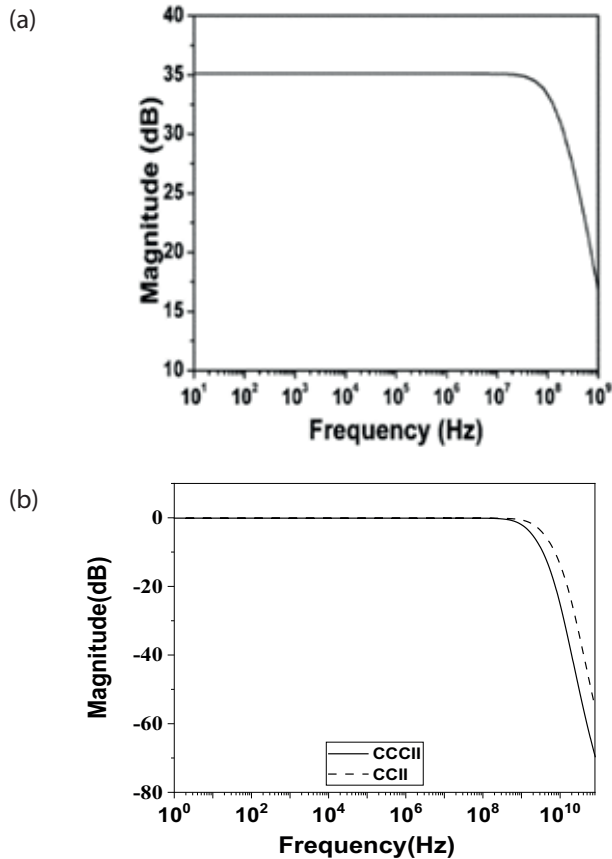

Figure 1: Symbolic representations of (a) OTA, (b) CCII, (c) CCCII; CMOS implementations of; (d) OTA, (e) CCII, (f) CCCII.

Similarly, port relationship CCCII± is given by:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_X & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

where, $R_X = \dfrac{1}{\sqrt{2I_b C_{ox}} \left(\sqrt{\dfrac{\mu_p W_p}{L_p}} + \sqrt{\dfrac{\mu_n W_n}{L_n}} \right)}$

Figure. 2(a-b) shows the OTA, CCII, and CCCII frequency responses. They result in a bandwidth of 80 MHz for OTA and 1 GHz and 800 MHz for CCII and CCCII, respectively.

(a)

(b)

Figure 2: Frequency response of (a) OTA, (b) CCII and CCCII.

2.2 Basic model of a meminductor emulator

Symbolic representation of meminductor is shown in Figure. 3. Meminductor is a mem-element with three constitutive variables as; φ(t), ρ(t), and I(t), where φ(t) is the flux, which is defined as the integral of input voltage i.e.

$$\Phi(t) = \int V_{in}(t)\,dt \qquad\qquad 2(a)$$

Figure 3: Symbolic representation of meminductor.

ρ(t) is the integral of φ(t), i.e.

$$\rho(t) = \int \Phi(t)\,dt \qquad\qquad 2(b)$$

The relation between input current I(t) and φ(t) of meminductor is defined as;

$$\frac{I(t)}{\phi(t)} = L_M^{-1} \qquad\qquad 3(a)$$

L_M^{-1} is inverse meminductance and the general representation of flux controlled meminductor having an initial value of inverse meminductance given by 'm' and decremental or incremental product term given by n is expressed as [14, 18];

$$\frac{I(t)}{\phi(t)} = m \pm n\rho(t) \qquad\qquad 3(b)$$

or, $I(t) = \big(m \pm n\rho(t)\big)\phi(t)$

It can be inferred from (3b) that a meminductor model contains 'm' as a fixed term and nρ(t) as a time varying term.

3 Proposed grounded and floating meminductor emulator circuit

Schematic diagrams of the proposed grounded and floating meminductor emulators are shown in Fig. 4 and Figure. 5, respectively. The Incremental and decremental nature of the meminductor can be configured by a switching mechanism between pins M, N, O, and P of circuits as given in Table 1. These mechanisms apply to both grounded and floating meminductor emulators.

Table 1: Connection topology for pins M, N, O, and P for two modes of operations.

S. No.	Switch Connections	Mode of operation
1	M-N; O-P	Incremental
2	M-P; O-N	Decremental

3.1 Grounded meminductor emulator
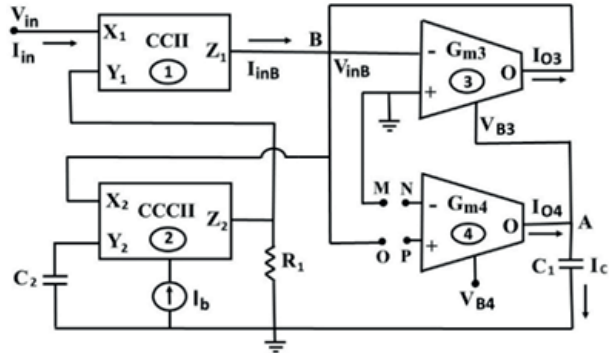
Figure 4: Schematic diagram of grounded meminductor emulator.

The proposed grounded meminductor emulator is shown in Figure. 4. Considering the incremental type of meminductor emulator, i.e., pins M, N and O, P are interconnected, the input current I_{in} is obtained as:

$I_{in}(t) = I_{X1} = I_{Z1}$ (using port relationship of CCII)

Again, $I_{in}(t) = -I_{inB}$ (4a)

Similarly, $V_{Y2} = V_{X2} - I_{X2}R_{X2}$,

(by the port relationship of CCCII)

$$V_{Y2} = V_{inB} = -\frac{I_{X2}}{sC_2} - I_{X2}R_{X2} = -I_{X2}(\frac{1}{sC_2} + R_{X2})$$ (4b)

Again, $I_{X2} = I_{Z2} = \dfrac{-V_{Y1}}{R_1} = \dfrac{-V_{in}}{R_1}$ (4c)

Since ($V_{Y1} = V_{X1} = V_{in}$)

Substituting (4c) in (4b)

$$V_{in} = V_{inB}\left(\frac{sR_1C_2}{1 + sC_2R_{X2}}\right)$$ (5)

Dividing (5) by (4a)

$$\frac{V_{in}}{I_{in}} = -\frac{V_{inB}}{I_{inB}}\frac{sR_1C_2}{1 + sC_2R_{X2}}$$ (6)

Bias voltage V_{B3} is given by

$$V_{B3} = \frac{1}{C_1}\int I_C(t)\,dt = \frac{G_{m4}}{C_1}\int V_{inB}(t)\,dt =$$

$$= \frac{G_{m4}}{C_1}\left(\frac{1 + sC_2R_{X2}}{SR_1C_2}\right)\int V_{in}(t)\,dt =$$ (7)

$$= \frac{G_{m4}}{C_1}\left(\frac{1 + sC_2R_{X2}}{sR_1C_2}\right)\phi_{in}$$

Where ϕ_{in} is the total flux obtained by the meminductor, and it is expressed as

$$\varphi_{in} = \int V_{in}(t)\,dt = \frac{V_{in}}{s}$$ (8)

Substituting (7) into (1), the transconductance G_{m3} is obtained as

$$G_{m3} = \frac{k}{\sqrt{2}}(V_{B3} - V_{ss} - 2V_{th}) =$$

$$= \frac{k}{\sqrt{2}}\left(\frac{G_{m4}(1 + sC_2R_{X2})\phi_{in}}{sC_1R_1C_2} - V_{ss} - 2V_{th}\right)$$ (9)

Also, $G_{m3} = \dfrac{-I_{O3}}{V_{inB}} = \dfrac{I_{inB}}{V_{inB}}$ (10)

Using (10) and (9) results in an expression

$$\frac{I_{inB}}{V_{inB}} = \frac{k}{\sqrt{2}}\left(\frac{G_{m4}(1 + sC_2R_{X2})\phi_{in}}{sC_1R_1C_2} - V_{ss} - 2V_{th}\right)$$ (11)

On substituting (11) in (6) and by incorporating the relation of (8), meminductance (L_M) of the proposed grounded incremental meminductor emulator is obtained as

$$L_M = \frac{\phi_{in}}{I_{in}} = \frac{R_1C_2}{\dfrac{k}{\sqrt{2}}(V_{ss} + 2V_{th}) - \dfrac{k}{\sqrt{2}}\left(\dfrac{G_{m4}(1 + sC_2R_{X2})\phi_{in}}{sC_1R_1C_2}\right)}\frac{1}{1 + sC_2R_{X2}}$$ (12)

Similarly, the switching connections to M-P and O-N changes the polarity of the time-variant part of the meminductance of (12), resulting in a decremental type meminductance as

$$L_M = \frac{R_1C_2}{\dfrac{k}{\sqrt{2}}(V_{ss} + 2V_{th}) + \dfrac{k}{\sqrt{2}}\left(\dfrac{G_{m4}(1 + sC_2R_{X2})\phi_{in}}{sC_1R_1C_2}\right)}\frac{1}{1 + sC_2R_{X2}}$$ (13)

Equations (12) and (13) can be combined and rewritten as

$$L_M = \frac{R_1 C_2}{\frac{k}{\sqrt{2}}(V_{ss}+2V_{th}) \mp \frac{k}{\sqrt{2}}\left(\frac{G_{m4}(1+sC_2 R_{X2})\phi_{in}}{sC_1 R_1 C_2}\right)} \frac{1}{1+sC_2 R_{X2}} \quad (14)$$

If the operating frequency is much lower than

$\dfrac{1}{2\pi C_2 R_{X2}}$ where R_{X2} is the resistance at input port X of CCCII and is usually kept low [40], then

we can write $(1+sC_2 R_{X2}) \approx 1$.

Hence, equation (14) can then be simplified in terms of the inverse of L_M as:

$$L_M^{-1} = \frac{\phi_{in}}{I_{in}} \approx \frac{k}{\sqrt{2}R_1 C_2}(V_{ss}+2V_{th}) \pm \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1 R_1^2 C_2^2}\right) \quad (15)$$

In equation (15), G_{m4} can be controllable by external bias voltage V_{B4}, which makes the proposed circuit electronically tunable. Equation (15) represents incremental and decremental meminductance, where for a fixed operating frequency $\dfrac{k}{\sqrt{2}R_1 C_2}(V_{ss}+2V_{th})$ is the

constant term and $\dfrac{k}{\sqrt{2}}\left(\dfrac{G_{m4}\phi_{in}}{sC_1 R_1^2 C_2^2}\right)$ is the time-varying

term as φ_{in} is the function of the time-varying input signal. For $\varphi_{in} = 0$ meminductance attains a constant value in both topologies (incremental and decremental), where for the operator $\pm$, the + is for decremental and – is for incremental configuration.

3.2 Floating meminductor emulator
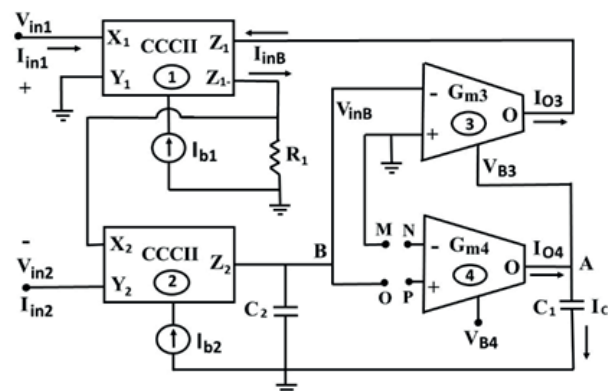
Figure 5: Schematic diagram of floating meminductor emulator.

The floating meminductor emulator is shown in Figure. 5. Considering incremental type meminductor emula-

tors, i.e., pins M, N, and pins O, P are interconnected. The currents from the port relationship are obtained as follows;

$$I_{in1} = I_{in} = I_{X1} = I_{Z1} = -I_{Z1-} \quad (16)$$

And $V_{in1} = V_{X1} = V_{Y1} + I_{X1} R_{X1} \quad (17)$

Hence, $V_{in1} = I_{in} R_{X1}$ [As V_{in1}=0] $\quad (18)$

Again, $V_{Z1-} = V_{Y2} = I_{Z1-} R = \dfrac{V_{in1}}{R_{X1}} R \quad (19)$

For $R = R_{X1}$, we get from (19),

$$V_{Y2} = V_{in1} \quad (20)$$

Further,

$$V_{in2} = V_{X2} = V_{Y2} + I_{X2} R_{X2} \text{ [from port relation]} \quad (21)$$

Hence from (20) and (21),

$$V_{in2} = V_{in1} + I_{X2} R_{X2} \quad (22)$$

As at node B, $I_{X2} = I_{Z2} = -sC_2 V_{inB} \quad (23)$

Hence from (22),

$$V_{in2} = V_{in1} - sC_2 V_{inB} R_{X2} \quad (24)$$

Or, $V_{in1} - V_{in2} = V_{in} = sC_2 V_{inB} R_{X2} \quad (25)$

From (25), $V_{in} = sR_{X2} C_2 V_{inB}$

0r, $V_{inB} = V_B = \left(\dfrac{V_{in}}{sR_{X2} C_2}\right) \quad (26)$

Also $I_{in} = I_{O3} \quad (27)$

Dividing (26) by (27), we get;

$$\frac{V_{in}}{I_{in}} = \frac{V_{inB}}{I_{O3}} sR_{X2} C_2 \quad (28)$$

Further, bias voltage V_{B3} using (26) results in;

$$V_{B3} = \frac{1}{C_1}\int I_C(t)\,dt = \frac{G_{m4}}{C_1}\int V_{inB}(t)\,dt =$$
$$= \frac{G_{m4}}{C_1}\left(\frac{1}{sR_{X2} C_2}\right)\int V_{in}(t)\,dt = \frac{G_{m4}}{C_1}\left(\frac{1}{sR_{X2} C_2}\right)\phi_{in} \quad (29)$$

Substituting (29) into (1), transconductance G_{m3} is obtained as;

$$G_{m3} = \frac{k}{\sqrt{2}}\left(V_{B3} - V_{ss} - 2V_{th}\right) =$$
$$= \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1 R_{X2} C_2} - V_{ss} - 2V_{th}\right) \tag{30}$$

Further from Fig. 5, $G_{m3} = -\dfrac{I_{O3}}{V_{inB}}$

So (30) becomes:

$$\frac{I_{O3}}{V_{inB}} = -\frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1 R_{X2} C_2} - V_{ss} - 2V_{th}\right) =$$
$$= \frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th} - \frac{G_{m4}\phi_{in}}{sC_1 R_{X2} C_2}\right) \tag{31}$$

Substituting (31) in (28) gives,

$$\frac{V_{in}}{I_{in}} = \frac{sR_{X2} C_2}{\dfrac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) - \dfrac{k}{\sqrt{2}}\left(\dfrac{G_{m4}\phi_{in}}{sC_1 R_{X2} C_2}\right)}$$

Hence, the meminductance of the proposed grounded incremental meminductor emulator is obtained;

$$L_M = \frac{R_{X2} C_2}{\dfrac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) - \dfrac{k}{\sqrt{2}}\left(\dfrac{G_{m4}\phi_{in}}{sC_1 R_{X2} C_2}\right)} \tag{32}$$

Similarly, the change of switch connections to M-P and O-N changes the polarity of the time-variant part of meminductance of (24), resulting in a decremental type meminductance;

$$L_M = \frac{R_{X2} C_2}{\dfrac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) + \dfrac{k}{\sqrt{2}}\left(\dfrac{G_{m4}\phi_{in}}{sC_1 R_{X2} C_2}\right)} \tag{33}$$

So, equations (32) and (33) can be combined and re-written as;

$$L_M = \frac{\phi_{in}}{I_{in}} = \frac{R_{X2} C_2}{\dfrac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) \pm \dfrac{k}{\sqrt{2}}\left(\dfrac{G_{m4}\phi_{in}}{sC_1 R_{X2} C_2}\right)}$$

$$L_M{}^{-1} = \frac{I_{in}}{\phi_{in}} = \tag{34}$$

$$\frac{k}{\sqrt{2}R_{X2} C_2}(V_{ss} + 2V_{th}) \pm \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1 R_{X2}{}^2 C_2{}^2}\right)$$

In equation (34), G_{m4} can be controllable by external bias voltage $V_{B4,}$ and R_{X2} is controlled by external current $I_{b2,}$ which makes the proposed circuit electronically tunable. In the inverse of the meminductance equation, the term $\dfrac{k}{\sqrt{2}R_{X2} C_2}(V_{ss} + 2V_{th})$ is constant, and

$\dfrac{k}{\sqrt{2}}\left(\dfrac{G_{m4}\phi_{in}}{SC_1 R_{X2}{}^2 C_2{}^2}\right)$ is the time-varying term as φ_{in} is the function of the time-varying input signal. For φ_{in} = 0, meminductance attains a constant value in both the topologies (incremental and decremental), where for the operator ±, the + is for decremental and – is for incremental configuration.

4 Comparison of meminductor emulators

A comparison of available meminductor emulators is given in Table 2. It is observed that most emulators use many analog building blocks for implementation and have frequency limitations. The emulator designs reported in [8-12, 26, 27] use many active building blocks and a large number of passive components and do not possess electronic tunability. Only the configurations [13, 14, 19] possess both grounded and floating types of meminductors, hence finding flexibility in applications. Moreover, the topologies [8-12, 15-18, 21, 25-27] are only grounded type, and [20, 23, 23, 28] are floating type of meminductors. Further, all these designs [8-14, 26-28] employ a multiplier in the configuration, which is undesirable as it increases circuit complexity. The design in [15] uses a floating inductor in the configuration, resulting only in grounded types of meminductor. Furthermore, the designs [8-13, 15, 21-26] exhibit low frequency of operation (few Hz to few kHz range). Meminductors [8-13, 22, 23, 28] can be operated only in incremental configuration.

The proposed work presents both grounded and floating types of meminductor realizations using simple basic blocks, two CCII/CCCII, and two OTAs with only two capacitors and one resistor. All the passive ele-

ments in both of the proposed meminductor circuits are grounded. Moreover, both the incremental and decremental properties are present in the proposed emulators. Further, the proposed grounded and float-ing meminductors are valid for frequencies of 1 MHz and 10 MHz, respectively. An important feature of the proposed meminductor emulator is its ability to control the meminductance value by controlling the

Table 2: Comparison of meminductor emulators.

Ref.	Number in count and type(s) of active building blocks used	Tech. used	Passive element (C/R/L)	All grounded passive elements	M /NM based	G/ F meminductor	Electronic tunability	Max. operating frequency shown	Inc/Dec or both	P. C (W)
[8]	3 CCII, 1 Multiplier, 1 Adder	CMOS	2/3/0	Yes	NM	G	No	20 Hz	Inc	NA
[9]	2 Op-Amp, 2 Current Mirrors, 1 Buffer, 1 Multiplier	CMOS	2/2/1	No	NM	G	No	300 Hz	Inc	NA
[10]	4 CFOAs, 1 Buffer, 2 Op-Amp, 1 Multiplier	CMOS	2/6/0	No	NM	G	No	36.9 Hz	Inc	NA
[11]	5 Op-Amp, 1 Multiplier	CMOS	2/10	No	NM	G	No	70 Hz	Inc	NA
[12]	6 Op-Amps, 1 Multiplier	BJT	2/13/0	No	NM	G	No	300 Hz	Inc	NA
[13]	1 OTA, 3 CFOA, 1 Op-Amp, 1 Multiplier	BJT	2/8/0	No	NM	Both (G+F)	Yes	5 kHz for both	Inc	NA
[14]	2 VDTAs, 1 Multiplier	CMOS	2/0/0	Yes	NM	Both (G+F)	Yes	1 MHz for both	Both	200 μ
[15]	1 MO-OTA	CMOS	1/1/1	No	NM	G	Yes	500 Hz	Both	120 μ
[16]	3 OTAs	CMOS	2/0/0	Yes	NM	G	Yes	10 MHz	Both	NA
[17]	2 OTAs,1 DVCC	CMOS	2/1/0	Yes	NM	G	Yes	10 MHz	Both	NA
[18]	1 OTA, 1 VDTA	CMOS	2/0/0	Yes	NM	G	Yes	3 MHz	Both	NA
[19]	2 OTAs, 1 CDBA	CMOS	2/0/0	Yes	NM	Both (G+F)	Yes	2 MHz for both	Both	NA
[20]	2 OTAs, 1 CDTA	CMOS	2/0/0	Yes	NM	F	Yes	1 MHz	Both	NA
[21]	2 CCIIs, 1 OTA	CMOS	2/2/0	Yes	NM	G	Yes	700 kHz	Both	14.3m
[22]	2 VDTAs	CMOS	2/0/0	Yes	NM	F	Yes	700 kHz	Inc	NA
[23]	1 MVDCC, 1OTA	CMOS	2/1/0	Yes	NM	F	Yes	300 kHz	Inc	NA
[25]	1 Microcontroller, 1 ADC, 1 Op Amp	CMOS	1/3/0	No	M	G	No	8 Hz	Both	NA
[26]	1 CCII, 6 Op-Amp, 1 Multiplier	CMOS	2/10/0	No	M	G	No	200 Hz	Both	NA
[27]	7 TOAs, 1 Op-Amp, 1 Multiplier, 3 Buffers	CMOS	2/11/0	No	M	G	No	21.1 Hz	Both	NA
[28]	2 CBTAs, 1 Multiplier	CMOS	2/2/0	No	M	F	Yes	1 MHz	Inc	NA
Our Work	2 OTAs, 1 CCCII, 1 CCII	CMOS	2/1/0	Yes	NM	G	Yes	1 MHz	Both	1.01 m
	2 OTAs, 2 CCCIIs	CMOS	2/1/0	Yes	NM	F	Yes	10 MHz	Both	1.03 m

Note: M: Mutator; NM: Non-mutator; G: grounded; F: Floating; Inc: Incremental; Dec: Decremental; P.C: Power consumption.

transconductance, G_{m4} with the bias voltage, $V_{B4;}$ hence both the emulator circuits are electronically tunable. Power consumption of the proposed circuits is greater than that of [14, 15], however smaller than that of [21] among the available literature.

5 Simulation results and discussion

This section deals with verifying the hysteresis loop between flux and the current, one of the fingerprints of the meminductor. Various simulations with 180 nm CMOS technology have been performed to verify the meminductive nature of proposed emulator circuits. Supply voltages of +1.2V and -1.2 V are used for V_{DD} and $V_{SS,}$ respectively, for grounded and floating meminductors. The aspect ratios of MOS transistors are given in Table 3, and they operate in the saturation region.

5.1 Grounded meminductor simulation result

The grounded meminductor emulator in Figure. 4 is simulated for different frequencies. The results for the pinched hysteresis loop obtained for a sinusoidal signal of amplitude (A_m=140 mV) with frequencies of 100 kHz, 200 kHz, 300 kHz, 400 kHz, and 500 kHz are shown in Figure. 6. Here, the product of the capacitor (C_2) value and frequency (f) is kept constant (75 x 10^{-6} FaradHz) and V_{B4}=450 mV. On increasing the frequency, the pinched hysteresis loop area of Φ-I curves decreases, which satisfies (14), suggesting that the time-varying nature of the loop decreases and ultimately vanishes at a specific frequency. Figure. 7 shows the relationship between charge q(t) and ρ(t), where $\rho(t) = \int \varphi(t)dt$ and $q(t) = \int i(t)dt$. Additionally, the current, $i(t)$ flowing in a meminductor can be expressed as per [6]. The single valued function q(ρ) has been illustrated in detail in [6]. This can also be verified graphically from Figure. 7 as a single valued curve is obtained, implicitly implying that the corresponding device is a meminductor.
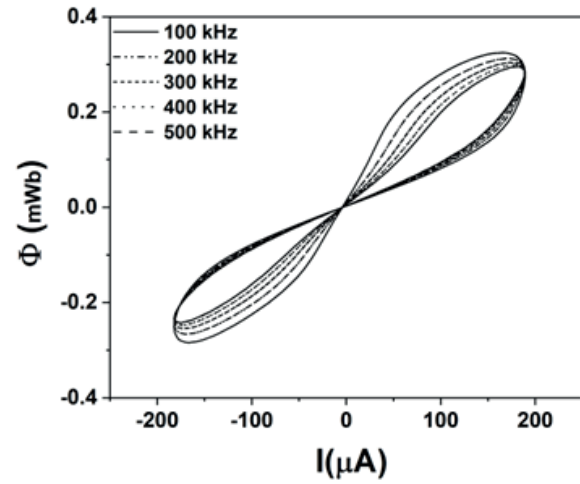
**Table 3:** Design Parameters for analog blocks in grounded meminductor

OTA

MOS Transistors	W(μm)	L(μm)
M_{1-4}	12	0.375
M_{10}	12	0.510
M_{5-9}, M_{11}	12	0.500

CCII/CCCII

MOS Transistors	W(μm)	L(nm)
M_1, M_{3-13}	12	0.500
M_2	2	0.200

Figure 6: Φ-I characteristic for grounded meminductor circuit at different operating frequencies for A_m = 140 mV, I_b=20 μA, V_{B4}= 0.45 V, C_1= 150 pF, R=10 Ω and constant C_2f =75 x 10^{-6} FaradHz.
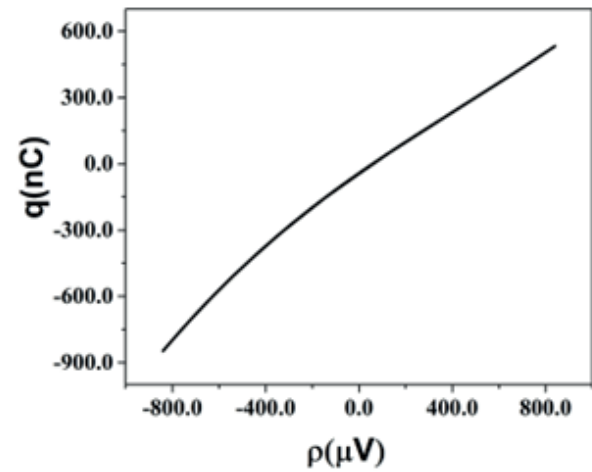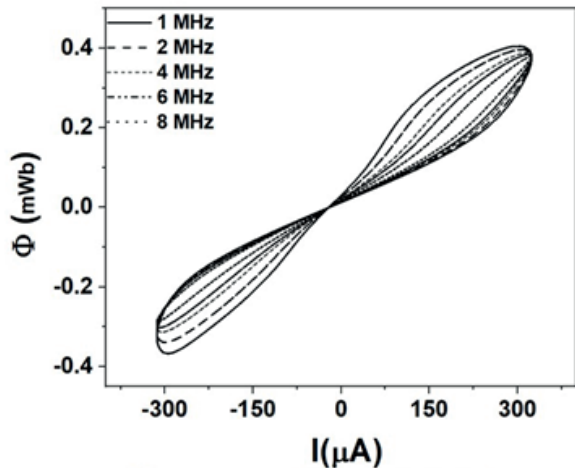

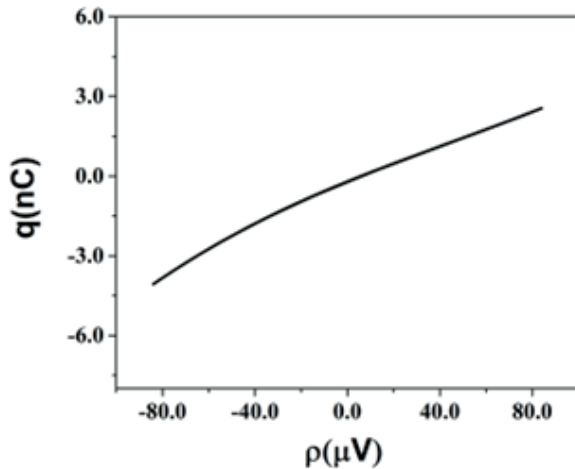**Figure 7:** Locus of q(t) and ρ(t) for grounded meminductor.

5.2 Floating meminductor simulation result

The floating emulator's simulation results for the pinched hysteresis loop obtained for frequencies of 1 MHz, 2 MHz, 4 MHz, 6 MHz, and 8 MHz are shown in Figure. 8. Here, the product of capacitor(C_2) value and frequency (f) is kept constant (75 x 10^{-6} FaradHz) with A_m=200 mV, V_{B4}=500 mV. On increasing the frequency, the pinched hysteresis loop area of Φ-I curves decreases; this validates the meminductive behavior of emulators as obtained in (34). Fig. 9 shows the relationship between charge q(t) and integral of flux, ρ(t). It shows that q(t) is a single-valued function of ρ(t). Therefore, the device current goes through a meminductor. On increasing the frequency, the pinched hysteresis loop area of Φ-I curves decreases, which satisfies (14), suggesting that the time-varying nature of the loop de-

creases and ultimately vanishes at a specific frequency. Figure 9 shows the relationship between charge q(t) and ρ(t). As discussed earlier for Figure 7, the curve in Figure 9 is also a single valued. Therefore, the device current flows through a meminductor.

Figure 8: Φ-I characteristic for floating meminductor circuit at different operating frequencies for A_m = 200 mV, I_{b2}=20 μA, V_{B4}= 0.5 V, C_1= 150pF, R=5 Ω and constant C_2f =75 x 10^{-6} FaradHz.

Figure 9: Locus of q(t) and ρ(t) for floating meminductor.

5.3 Effect of variation of bias voltage (VB4) of OTA on the pinched hysteresis loop

It is seen in (15) and (34) that the meminductance of emulators depends on transconductance G_{m4}, which is electronically tunable by the external bias voltage, V_{B4}. Figure. 10(a) shows the grounded meminductor's simulation results for signal frequency of 500 kHz, capacitor value C_1=C_2=150 pF, I_b=20μA, and A_m=140 mV at different values of V_{B4} (0.45 V, 0.4 V, and 0.35 V). Similarly, Figure. 10(b) shows the floating meminductor's simulation results for signal frequency of 500 kHz, capacitor value

of C_1=375 pF, C_2 =150 pF, I_{b1} =-48 μA, I_{b2} =-20 μA and A_m=140 mV at different values of V_{B4} (0.45V, 0.4V, and 0.35V). It is observed that the pinched hysteresis loop of Φ-I curves area increases with the increase of V_{B4} as expected as per position of G_{m4} in (15) and (34). It implies that the meminductance can be controlled by V_{B4}.
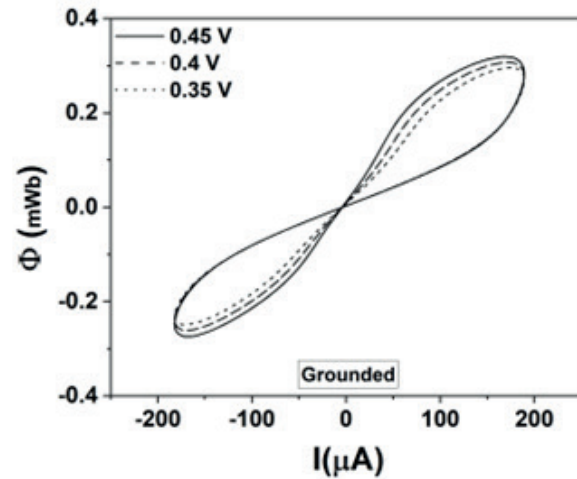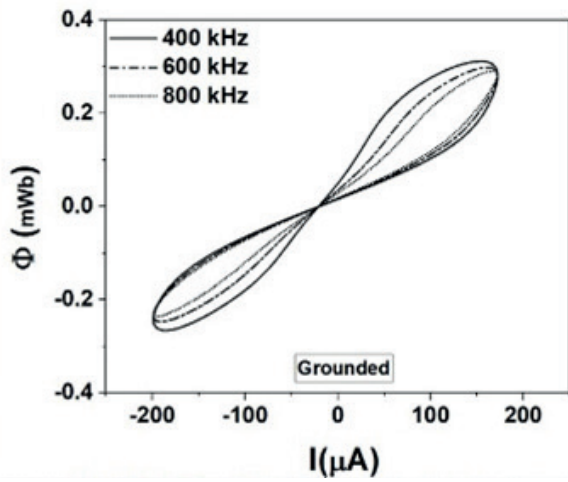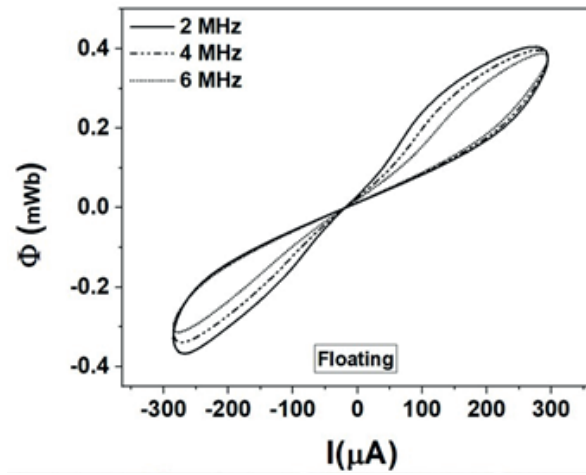

(a) Grounded
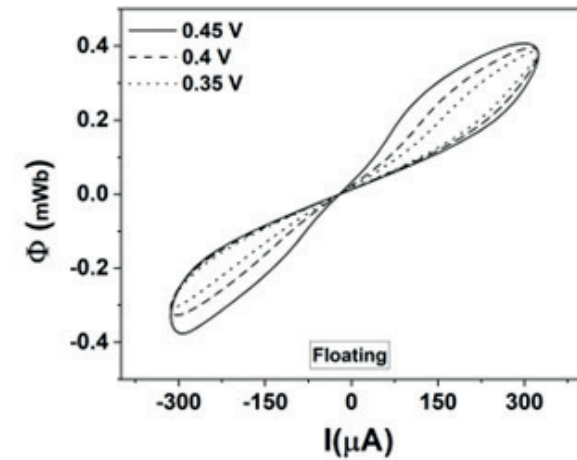
(b) Floating

Figure 10: Φ-I characteristic curves obtained with sinusoidal current signal with 500 kHz, A_m=140 mV, C_2=150 pF for (a) grounded meminductor circuit with C_1=150 pF, I_b=20 μA, and different V_{B4}, (b) floating meminductor circuit with C_1=375 pF, I_{b2}=20 μA, and different V_{B4}.

*5.4 Effect of varying frequency and capacitances on the pinched hysteresis loop*

The effect on Φ-I characteristics for variation of applied signal frequency for a fixed capacitance for both grounded and floating meminductor emulators are shown in Figures. 11(a) and 11(b), respectively. Figure. 11(a) shows that as frequency increases from 400 kHz – 800 kHz for a fixed capacitance value, the hysteresis
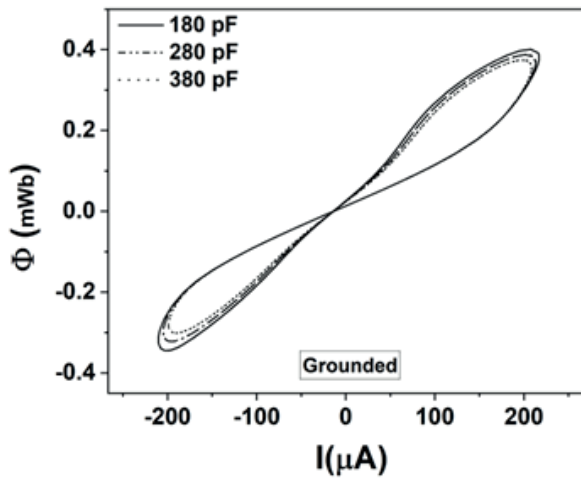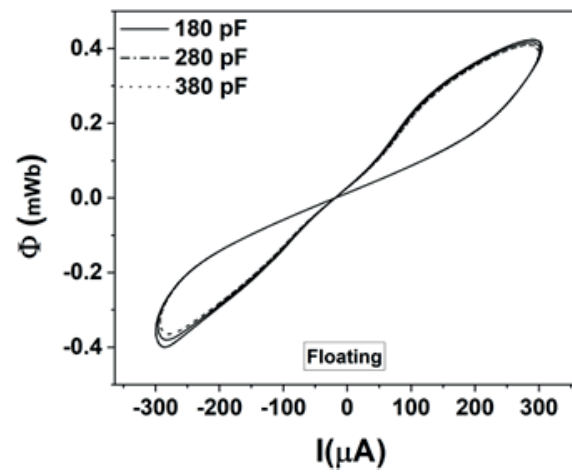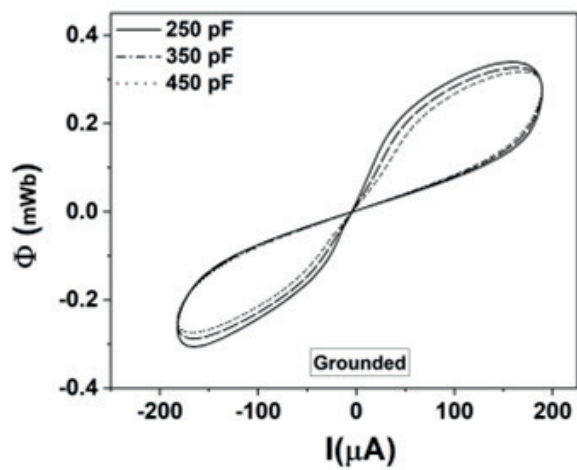
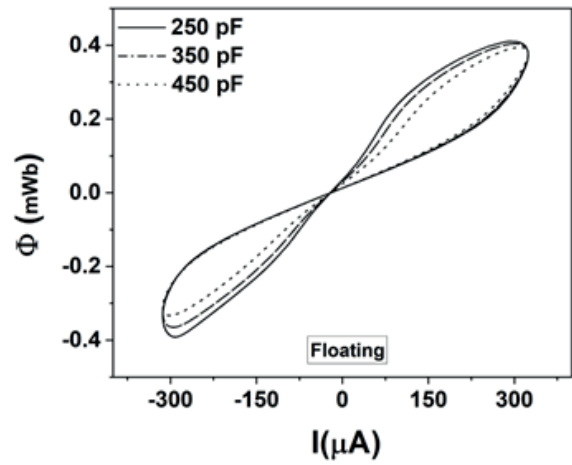**Figure 11:** Φ-I characteristic curves for a sinusoidal current signal of A_m=140 mV and V_{B4}=500mV for (a) grounded meminductor for the variable frequency with C_1=180 pF, C_2=150pF, I_b=20 µA, (b) floating meminductor for the variable frequency at C_1=375 pF, C_2=150pF, I_{b2}=20 µA, (c) grounded meminductor for variable C_2 at 500 kHz (d) floating meminductor for variable C_2 at 800 kHz frequency, (e) grounded meminductor for variable C_1 at 500 kHz frequency, (f) floating meminductor for variable C_1 at 800 kHz frequency.

loop becomes more and more linear, which satisfies (15), suggesting the time-varying nature of the loop decreases. Figure. 11(b) shows that as the frequency increases from 800k Hz – 4 MHz for a fixed capacitance value, the area under the hysteresis loop gradually decreases as predicted by (34). Similar to the effect of frequency variation, area of hysteresis loop of meminductance changes for the variation in capacitances (C_1 and C_2) and this can also be verified by observing these parameters in (15) and (34). On varying C_1 and C_2 with a fixed frequency of 500 kHz for grounded topology and 800 kHz for floating topology, the results are obtained as shown in Figure. 11(c-f).

## 6 Layout, post-layout simulations, and Monte Carlo analysis

Layouts are obtained, and post-layout simulations are carried out for both grounded and floating topologies to check the effect of parasitics on the hysteresis. Further, the simulation results of the Monte Carlo analysis of proposed emulator circuits are also presented.

6.1 Pre and post-layout results for grounded and floating meminductor emulators

Layouts of grounded and floating meminductor emulators are shown in Figure. 12. Layout areas occupied by grounded and floating meminductor emulators are 1845 μm^2 and 1874 μm^2, respectively. Figure. 13(a, b) shows the Φ-I characteristic curves for grounded me-

(a)

(b)
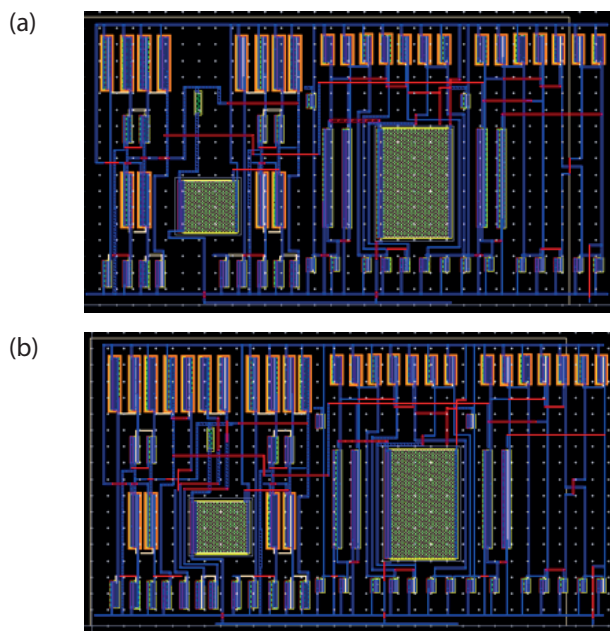
Figure 12: Layout of meminductor emulators (a) grounded (b) floating.

(a)

(b)

(c)

(d)
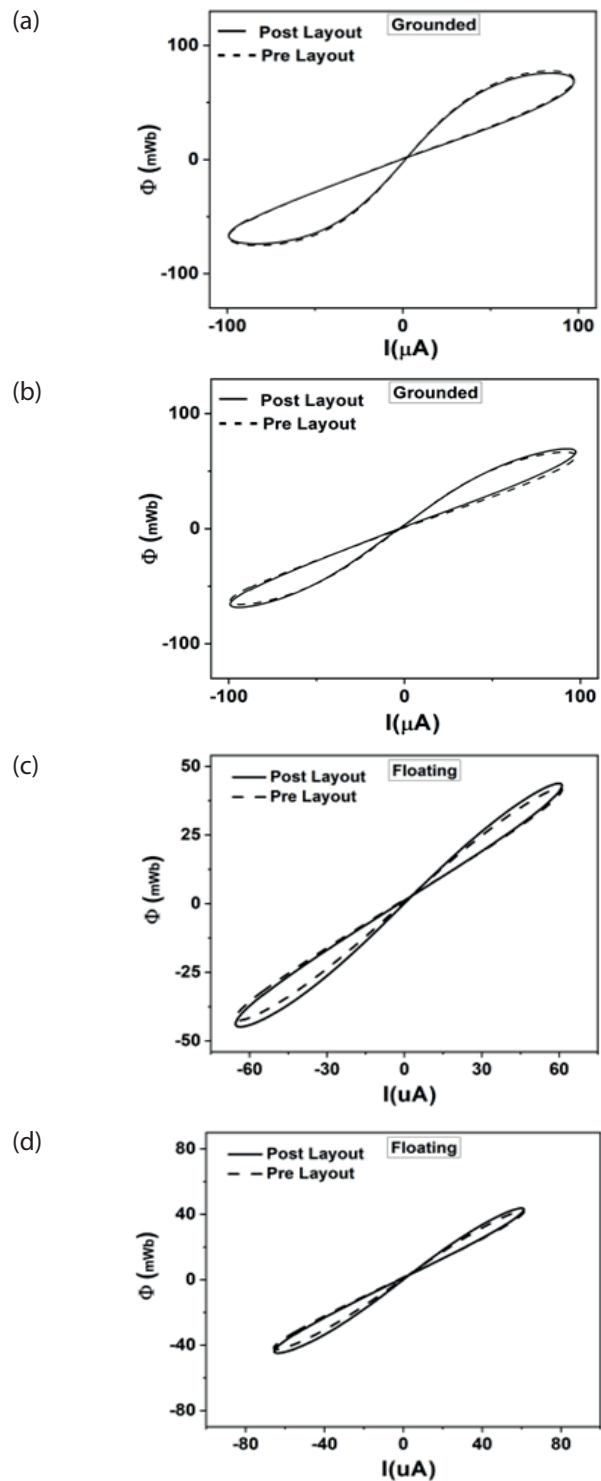
Figure 13: Pre and Post layout simulation results of Φ-I characteristic plot for (a) grounded meminductor emulator at 500 kHz for V_{B4} = 450 mV, A_m = 140 mV, C_1=48 pF, C_2= 80 pF and I_b=20 µA, (b) grounded meminductor emulator at 1 MHz for V_{B4} = 450 mV, A_m = 140 mV, C_1= 8 pF, C_2=13 pF and I_b=20 µA, (c) floating meminductor emulator at 100 kHz for V_{B4} = 500 mV, A_m = 200 mV, C_1=75 pF, C_2=150 pF and I_{b2}=18 µA, (d) floating meminductor emulator at 1 MHz for V_{B4} = 500 mV, A_m = 200 mV, C_1=18 pF, C_2=28 pF, and I_{b2}=18 µA.

minductor emulators at 500 kHz and 1 MHz, respectively. Similarly, Figure. 13(c, d) shows the Φ-I characteristic curves for floating meminductor emulators at 100 kHz and 1 MHz operating frequencies, respectively. It is observed in Figure. 13 that the pre and post-layout results are in close agreement except for slight deviations due to parasitics present in active blocks.

6.2 Monte Carlo analysis

Monte Carlo (MC) simulation for process mismatch at a frequency of 1 MHz for 200 simulation runs is performed for grounded topology. A similar MC analysis is performed for floating topology at a frequency of 200 kHz for 200 simulation runs. MC results for the hysteresis loop in both grounded and floating topology are shown in Figure. 14. Figure. 14 reveals that the proposed circuit is affected by process mismatch; however, the hysteresis loop closely retains the original form.

(a)

(b)
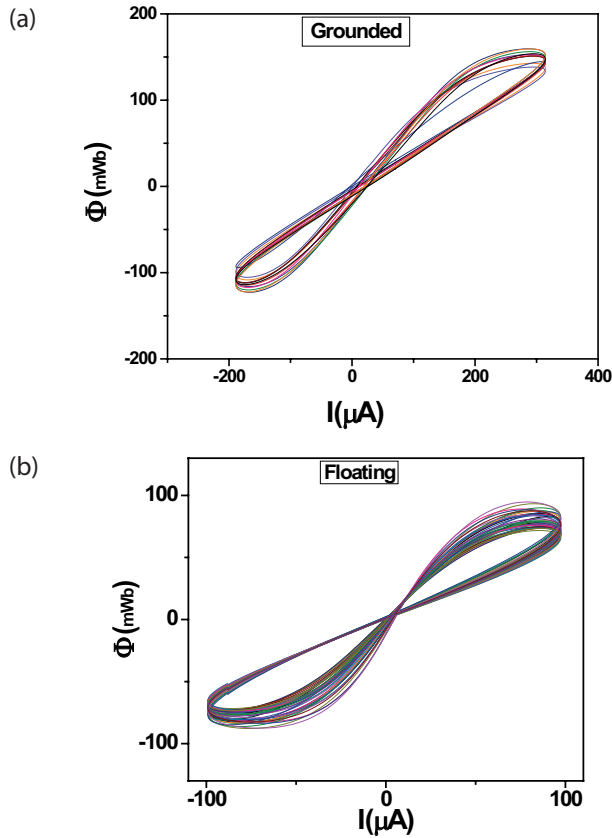
Figure. 14. Hysteresis loop of MC result for 200 simulation runs for (a) grounded topology and (b) floating topology.

7 Nonideality Analysis

Non-ideal transfer gains and parasitics of active building blocks affect the emulator's response. Sections 7.1 discusses the effect due to non-ideal transfer gains, and sections 7.2 and 7.3 discuss the effect due to OTA and CCII/CCCII parasitics.

7.1 Nonideality effect of OTA transconductance gain and CCII/CCCII current and voltage transfer gains

Due to the OTA's non-ideal transfer gain, the port relationship is modified as follows:

$$I_{0\pm} = \pm\gamma G_m \left(V_{in+} - V_{in-} \right) = \pm\gamma G_m V_{in} \tag{35}$$

γ is the non-ideal transconductance gain coefficient from the input terminal to the output terminal of OTA, which is ideally considered unity.

Similarly, the port relationships of CCII and CCCII due to non-ideal transfer gains become:

$$\begin{bmatrix} V_X \\ I_Z \\ I_Y \end{bmatrix} = \begin{bmatrix} \beta_1 & 0 & 0 \\ 0 & \alpha_1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \text{ and} \tag{36}$$

$$\begin{bmatrix} V_X \\ I_Z \\ I_Y \end{bmatrix} = \begin{bmatrix} \beta^{(j)} & R_X & 0 \\ 0 & \alpha^{(j)} & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}, \tag{37}$$

Where j=1 stands for the first CCCII and j=2 for the second CCCII. α and β and are current and voltage transfer gains from X to Z and Y to X terminals for CCII/CCCII, respectively. Ideally, α and β are unity.

The routine analysis of Figure. 4 considering non-ideal port relationships from (35), (36), and (37) for grounded meminductor configuration results in:

$$\frac{\phi_{in}}{I_{in}} = \frac{R_1 C_2 \beta^{(2)} \alpha_1 \alpha^{(2)}}{\frac{k\gamma_1}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) \mp \frac{k\gamma_1\gamma_2}{\sqrt{2}}\left(\frac{G_{m4}\left(1 + sC_2 R_{X2}\right)\phi_{in}}{\beta^{(2)}\alpha_1\alpha^{(2)} sC_1 R_1 C_2}\right)} \frac{1}{1 + sC_2 R_{X2}} \tag{38}$$

Similar analysis for the floating topology of Figure. 5 results in:

$$\frac{\alpha^{(1)}\beta^{(2)}V_{in1} - V_{in2}}{I_{in}} = \frac{sR_{X2}C_2}{\dfrac{k\gamma_1\alpha^{(2)}}{\sqrt{2}}\left(V_{ss}+2V_{th}\right)\mp\dfrac{k\alpha^{(2)}\gamma_1\gamma_2}{\sqrt{2}}\left(\dfrac{G_{m4}\alpha^{(2)}\int\left(\alpha^{(1)}\beta^{(2)}V_{in1}-V_{in2}\right)dt}{sC_1R_{X2}C_2}\right)} \tag{39}$$

[where $V_{in1} - V_{in2} = V_{in}$ and $\int(V_{in1} - V_{in2})dt = \varnothing_{in}$]

γ_1 and γ_2 are the transconductance gains of grounded and floating meminductors' first and second OTAs. It is observed from (38) and (39) that non-ideal transfer gains affect meminductance.

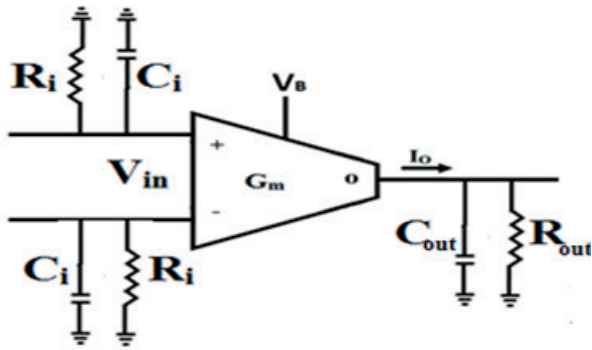*7.2 Nonideality effect due to device parasitics on grounded meminductor emulator*

Figure 15: Non-ideal model of OTA [36-37]

Figure. 15 shows the non-ideal model of OTA where (R_i, C_i) and (R_0, C_0) are input and output parasitic capacitances and resistances, respectively. The capacitances across the input ports are assumed to be equal.
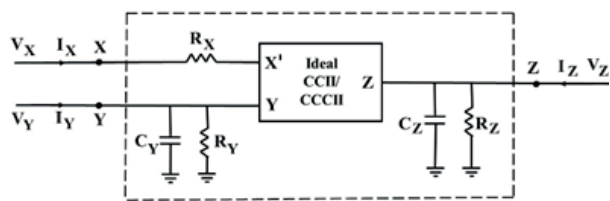

Figure 16: Non-Ideal model of the CCII/CCCII [38].

Figure. 16 shows the non-ideal model of CCII/CCCII. R_X represents a low-value parasitic resistance at the X terminal for CCII., whereas R_X for CCCII is a variable intrinsic resistance. At terminal Y and Z, the parasitic components are in parallel (i.e., $R_Y \| C_Y$ and $R_Z \| C_Z$), where R_Y and R_Z are of high value, and C_Y and C_Z are of low value. Fig. 17 shows the non-ideal model with device parasitics of proposed grounded meminductor emulators of Fig.4. Let the impedances be:
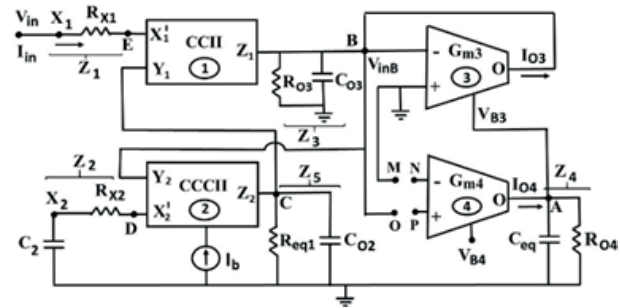

Figure 17: Non-ideal model of grounded meminductor emulator.

$$Z_1 = (R_{X1}),\quad Z_2 = (R_{X2}+X_{C2}),\quad Z_3 = (R_{03}\|X_{C03}),$$
$$Z_4 = (R_{04}\|X_{Ceq})\text{ and }Z_5 = (R_{eq1}\|X_{C02}) \tag{40}$$

where

$$C_{eq} = (C_1 + C_{out4}),$$
$$R_{03} = (R_{i3}\|R_{i4}\|R_{Z1}\|R_{Y2}\|R_{out3}),$$
$$R_{eq1} = (R_1\|R_{Y1}\|R_{z2}),$$
$$C_{03} = (C_{i3}\|C_{i4}\|C_{Z1}\|C_{Y2}\|C_{out3}),$$
$$C_{02} = (C_{Z2}\|C_{Y1})\text{ and }R_{o4} = R_{out4} \tag{41}$$

Where R_{i3}, C_{i3}, and R_{i4}, C_{i4} are parasitic resistances and capacitances at the inputs of the first OTA (G_{m3}) and second OTA (G_{m4}), respectively. Similarly, R_{out3}, C_{out3}, and R_{out4}, C_{out4} are parasitic resistances and cap acitances at the first OTA (G_{m3}) and second OTA (G_{m4}) output, respectively.

$$V_{Y2} = V_{inB} = V_{X2} - I_{X2}R_{X2} =$$
$$= -I_{X2}X_{C2} - I_{X2}R_{X2} = -I_{X2}Z_2\text{ (by port relationship)} \tag{42}$$

Also, on applying KCL at node C and by port relationship

$$I_{X2} = I_{Z2} = \frac{-V_{Y1}}{Z_5} = \frac{-(V_{X1})}{Z_5} = \frac{-(V_{in})}{Z_5} \tag{43}$$

Using (43) in (42) results in

$$V_{in} = \psi V_{inB}, \text{ where } \psi = \left(\frac{Z_5}{Z_2}\right) \qquad (44)$$

On applying KCL at node B

$$I_{in} = I_{Z1} = I_{O3} - \frac{V_{inB}}{Z_3} \qquad (45)$$

Using (44) and (45) results in

$$\frac{I_{in}}{V_{in}} = \left(\frac{1}{\psi}\right)\left(\frac{I_{O3} - \frac{V_B}{Z_3}}{V_B}\right) = \qquad (46)$$

$$\left(\frac{1}{\psi}\right)\left(\frac{I_{O3}}{V_B}\right)\left(1 - \frac{V_{inB}}{I_{O3}Z_3}\right)$$

Further analysis using (1) and $G_{m3} = \frac{-I_{O3}}{V_{inB}}$ results in the following;

$$\frac{I_{O3}}{V_{inB}} = \frac{k}{\sqrt{2}}(V_{ss} + 2V_{TH}) - \frac{kZ_4 G_{m4} V_{in}}{\sqrt{2}\psi} \qquad (47)$$

So, the inverse meminductance equation after substituting (47) in (46) becomes for both the incremental and decremental topologies

$$\frac{I_{in}}{V_{in}} = \frac{1}{\psi}\left(\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th}) \mp \frac{kZ_4 G_{m4} V_{in}}{\sqrt{2}\psi}\right)\left(1 - \frac{V_B}{I_{O3}Z_3}\right) (48)$$

Typical practical values of CMOS OTA parasitic obtained from routine analysis and [38] can be assumed to be approximately, $R_{i3} = R_{i4} = \infty$, $R_o = 1 M\Omega$, $C_i = 50$ fF, $C_o = 100$ fF. Similarly, values of CCII/CCCII obtained from routine analysis and [40] can be assumed to be a few ohms for Rx, a few hundreds of MΩ for R_y, and few MΩ for R_z, and the Cy, and Cz are in the range of a few femtofarads. If the operating frequency is within the range of a few MHz, then we may use:

$$Z_2 \approx R_{X2} + \frac{1}{sC_2}, \ Z_4 \approx 1/sC_1, \ Z_5 \approx R_1 = \text{few } \Omega,$$

$$\psi = \frac{sR_1 C_2}{1 + sC_2 R_{X2}}, \text{ and } Z_3 \approx \infty, \text{ and}$$

$$\left[\frac{V_{inB}}{I_{O3}Z_3}\right] \approx 0 \text{ as } (Z_3 \approx \infty).$$

The substitution of these values in (48) results in:

$$\frac{V_{in}}{I_{in}} = \frac{sR_1 C_2}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th}) \mp \frac{k}{\sqrt{2}}\left(\frac{G_{m4}(1 + sC_2 R_{X2})\phi_{in}}{sC_1 R_1 C_2}\right)} \frac{1}{1 + sC_2 R_{X2}} (49)$$

This is similar to (14). Hence, it can be concluded that the effect of parasitics on the proposed grounded circuit in the frequency range of a few MHz is negligible.

7.3 Nonideality effect due to device parasitic on floating meminductor emulator
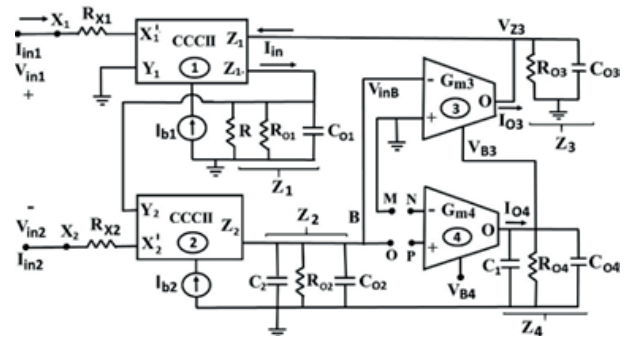
Figure 18: Non-Ideal model of proposed floating meminductor emulator.

In Figure. 18, let the equivalent impedances at nodes be given as,

$$Z_1 = (R_{01} \| X_{C01}) \| R, \ Z_2 = (R_{02} \| X_{C02}) \| X_{C2}, \qquad (50)$$
$$Z_3 = (R_{03} \| X_{C03}) \text{ and } Z_4 = (R_{04} \| X_{C04}) \| X_{C1}$$

and

$$C_{01} = (C_{Z1-} + C_{Y2}), \quad C_{02} = (C_{Z2} + C_{i3} + C_{i4}),$$
$$C_{03} = (C_{out3} + C_{Z1}), \quad C_{04} = (C_{out4}), \qquad (51)$$
$$R_{01} = (R_{Z1-} \| R_{Y2}), \quad R_{02} = (R_{Z2} \| R_{i3} \| R_{i4}),$$
$$R_{03} = (R_{Z1} \| R_{out3}), \ R_{04} = (R_{out4})$$

Also, $V_{Y2} = V_{z1-} = \frac{V_{in1}}{R_{X1}} Z_1$ (by port relationship) $\qquad (52)$

By applying the port relationship at the X_2 terminal of CCCII and using (52), we get:

$$V_{X2} = V_{in2} = V_{Y2} + I_{X2} R_{X2} = \frac{V_{in1}}{R_{X1}} Z_1 + I_{X2} R_{X2} (53)$$

Moreover, at node B,

$$-I_{Z2}Z_2 = V_{inB} \text{ , or, } I_{Z2} = I_{X2} = \frac{-V_{inB}}{Z_2} \tag{54}$$

Thus, from (53) and (54),

$$\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2} = V_{inB}\frac{R_{X2}}{Z_2} \tag{55}$$

Further as; $I_{in} = I_{Z1} = I_{O3} - \dfrac{V_{Z3}}{Z_3}$ (56)

Hence, from (55) and (56)

$$\frac{\dfrac{V_{in1}}{R_{X1}}Z_1 - V_{in2}}{I_{in}} = \frac{V_{inB}}{\left(I_{O3} - \dfrac{V_{Z3}}{Z_3}\right)}\frac{R_{X2}}{Z_2} \tag{57}$$

Or, $\dfrac{\dfrac{V_{in1}}{R_{X1}}Z_1 - V_{in2}}{I_{in}} = \dfrac{V_{inB}}{I_{O3}\left(1 - \dfrac{V_{Z3}}{I_{O3}Z_3}\right)}\dfrac{R_{X2}}{Z_2}$ (58)

Further, as $V_{B3} = Z_4 I_{O4} = Z_4 G_{m4} V_{inB}$ (59)

Hence from (55), by putting the value of V_{inB} in (59), V_{B3} becomes;

$$V_{B3} = \left(G_{m4}Z_4\right)\left(\frac{Z_2}{R_{X2}}\right)\left(\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2}\right) \tag{60}$$

Also, $G_{m3} = \dfrac{-I_{O3}}{V_{inB}}$ (61)

Further from (1) and (60),

$$G_{m3} = \frac{k}{\sqrt{2}}\left(V_{B3} - V_{ss} - 2V_{th}\right) =$$
$$= \frac{k}{\sqrt{2}}\left(\left\{\left(G_{m4}Z_4\right)\left(\frac{Z_2}{R_{X2}}\right)\left(\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2}\right)\right\} - V_{ss} - 2V_{th}\right)$$

Using (61) results in;

$$\frac{I_{O3}}{V_{inB}} = -\frac{k}{\sqrt{2}}\left(\left\{\left(G_{m4}Z_4\right)\left(\frac{Z_2}{R_{X2}}\right)\left(\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2}\right)\right\} - V_{ss} - 2V_{th}\right)$$

$$\frac{I_{O3}}{V_{inB}} = \frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th} - \left\{\left(G_{m4}Z_4\right)\left(\frac{Z_2}{R_{X2}}\right)\left(\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2}\right)\right\}\right) \tag{62}$$

On substituting (62) in (58) we obtain (both the incremental and decremental topologies) as;

$$\frac{\dfrac{V_{in1}}{R_{X1}}Z_1 - V_{in2}}{I_{in}} =$$

$$= \frac{\dfrac{R_{X2}}{Z_2}}{\dfrac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th} \mp \left(G_{m4}Z_4\right)\left(\dfrac{Z_2}{R_{X2}}\right)\left(\dfrac{V_{in1}}{R_{X1}}Z_1 - V_{in2}\right)\right)} \tag{63}$$

$$\left(1 - \frac{V_{Z3}}{I_{O3}Z_3}\right)$$

It is inferred from (63) that meminductance will be affected by parasitics, however, the typical values of CMOS OTA parasitics obtained from routine analysis and [38] are; $R_i = \infty$, $R_o = 1M\Omega$, $C_i = 50$ *fF*, $C_o = 100$ *fF*, while those of CCII/CCCII are as discussed previously in connection to grounded meminductor. If the operating frequency is within the range of a few MHz (say 10 MHz), then we may write: $Z_2 = X_{C2}$, $Z_4 = XC_1$, $Z_1 = R$, $R = R_{X1}$, $Z_3 \approx$ very high, and hence, $\left[\dfrac{V_{Z3}}{I_{O3}Z_3}\right] \approx 0$. The substitution of these terms in (63) for both incremental and decremental topologies results in:

$$\frac{V_{in}}{I_{in}} = \frac{sR_{X2}C_2}{\dfrac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) \mp \dfrac{k}{\sqrt{2}}\left(\dfrac{G_{m4}\phi_{in}}{sC_1R_{X2}C_2}\right)} \tag{64}$$

This is similar to (32) and (33). Hence it can be concluded that the effect of parasitics on the proposed floating meminductor in the frequency range of 10 MHz is negligible.

8 Application of meminductor as amplitude modulator (AM)

An AM modulation scheme with a meminductor is carried out as an application of the proposed meminductive device. Schematic of various circuits along with a floating meminductor emulator is shown in Figure. 19. In Figure. 19(a), a multifunction filter [39] using OTA is

given, which can implement both bandpass filter (BPF) and low pass filter (LPF) responses using the components, as given in Table 4, for Y_1, Y_2, Y_3, Y_4, and Y_5. Current mode (CM) BPF and LPF filters are used for modulation and demodulation, respectively. The meminductance of the meminductor shown in Figure. 19(b) is controlled by the low-frequency message signal $V_m(t)$, due to which message gets imposed on the high-frequency carrier signal $V_c(t)$. The output is filtered out by the bandpass filter in Figure. 19(a) centered at the carrier frequency to obtain an amplitude-modulated wave. The circuit in Figure. 19(c) is used to demodulate the AM signal to recover the message signal.

(a)

(b)

(c)
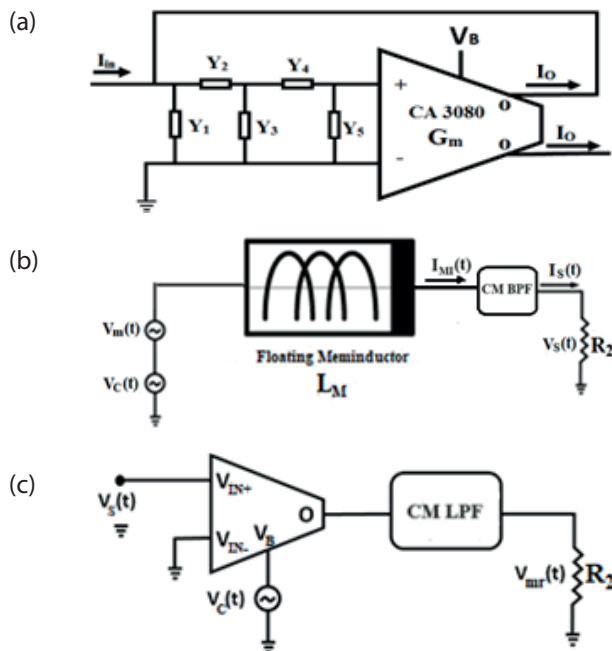
Figure 19: Block diagram of (a) current mode multi-function filter, (b) AM modulator circuit using floating meminductor emulator and filter, (c) coherent demodulator circuit using OTA.

Table 4. Specification for multimode filter components

	Y_1	Y_2	Y_3	Y_4	Y_5
Low pass	C1	R2	C3	∞	0
Band pass	R1	R2	C3	C4	R5

8.1 Analysis of amplitude modulator and demodulator

The voltage message signal $V_m(t)$ and carrier signal $V_c(t)$ are given by

$$V_m(t) = A_m \cos(\omega_m t),\ V_C(t) = A_C \cos(\omega_c t) \quad (65)$$

The flux imposed on the meminductor is given by

$$\varphi_{in} = \int V_{in}(t)\,dt = \int \left(V_m(t) + V_C(t)\right) dt =$$
$$= \frac{A_m \sin(\omega_m t)}{\omega_m} + \frac{A_C \sin(\omega_C t)}{\omega_C} \quad (66)$$

Also, $V_{in}(t) = A_m \cos(\omega_m t) + A_C \cos(\omega_c t)$ (67)

Thus, the output current of the meminductor, $I_{MI}(t)$, of Figure 19(b) results as:

$$I_{MI}(t) = V_B \frac{k}{\sqrt{2}} \left(\frac{G_{m4}}{C_1} \int V_B(t)\,dt - V_{ss} - 2V_{th} \right) \quad (68)$$

Now using (26), (66), and (67) in (68) and passing it through BPF yields;

$$I_s(t) = M_1 \sin\omega_c t + M_2 \left[\sin(\omega_c + \omega_m) + \right.$$
$$\left. + \sin(\omega_c - \omega_m) \right] + M_3 [\sin(\omega_c + \omega_m) -$$
$$- \sin(\omega_c - \omega_m)] \quad (69)$$

where,

$$M_1 = -\frac{k(V_{SS} + 2V_{th})A_C}{\sqrt{2}R_{X2}C_2\omega_C},$$

$$M_2 = \frac{A_C A_m G_{m4} k}{2\sqrt{2}C_1\omega_C} \left(\frac{1}{sR_{X2}C_2} \right)^2 \text{ and}$$

$$M_3 = \frac{A_C A_m G_{m4} k}{2\sqrt{2}C_1\omega_m} \left(\frac{1}{sR_{X2}C_2} \right)^2$$

It is evident that (69) is in the form of components of the upper sideband, lower sideband, and carrier of standard AM expression. In order to recover the message signal from the modulated signal, a coherent product demodulator is used. The demodulator circuit is realized with OTA as a multiplier cascaded with an OTA-based low pass filter, as shown in Figure. 19(c).

8.2 Simulation of amplitude modulator and demodulator

The parameters used for simulating the amplitude modulator (AM) and demodulator are given in Table 5. Figure. 20(a) shows the carrier signal ($V_C(t)$), modulating signal ($V_m(t)$), and the modulated signal, $V_S(t) = I_s(t)$ R_1 taken at the output of current mode band pass filter in Figure. 19(b). Figure. 20(b) shows the modulated

signal spectrum obtained by applying the rectangular window function. Figure. 20(c) shows the recovered message signal, $V_{mr}(t)$, obtained at the output of the coherent demodulator, as shown in Figure. 19(c). It confirms that the scheme of AM proposed in this section using meminductor circuit works as intended. It can further be shown that one can obtain under, over, and critical modulations by varying the amplitude of carrier and message signal. Figures 20(d) and 20(e) show amplitude-modulated waveform and its hysteresis loop for the one-time period, respectively. On analyzing Figure. 20(d) and Figure. 20(e) simultaneously, one can observe that the amplitude of the hysteresis loop formed between charge and voltage increases and decreases according to the increase and decrease in the amplitude of the message signal. So, the hysteresis loop itself changes its shape, size, and amplitude according to the message signal. For the first half cycle of the message signal, i.e., for time interval A-B in Fig. 20(d), the amplitude of the hysteresis loop in Fig. 20(e) decreases from point S to T in the positive half cycle, and point U to V in the negative half cycle of the modulated wave, simultaneously. This results in the mapping of message amplitude on the carrier signal. Similarly, for the second half cycle of the message signal, i.e., for time interval B-C in Figure. 20(d), the hysteresis loop of Figure. 20(e) increases from point T to S for the positive half cycle and point V to U for the negative half cycle of the modulated wave simultaneously leading to the mapping of message amplitude on the carrier signal. Thus, the hysteresis loop, resulted from one time period of AM signal is nothing but a meminductance slope, which is frozen i.e. it does not get affected by the peak

Table 5: AM circuit simulation parameter

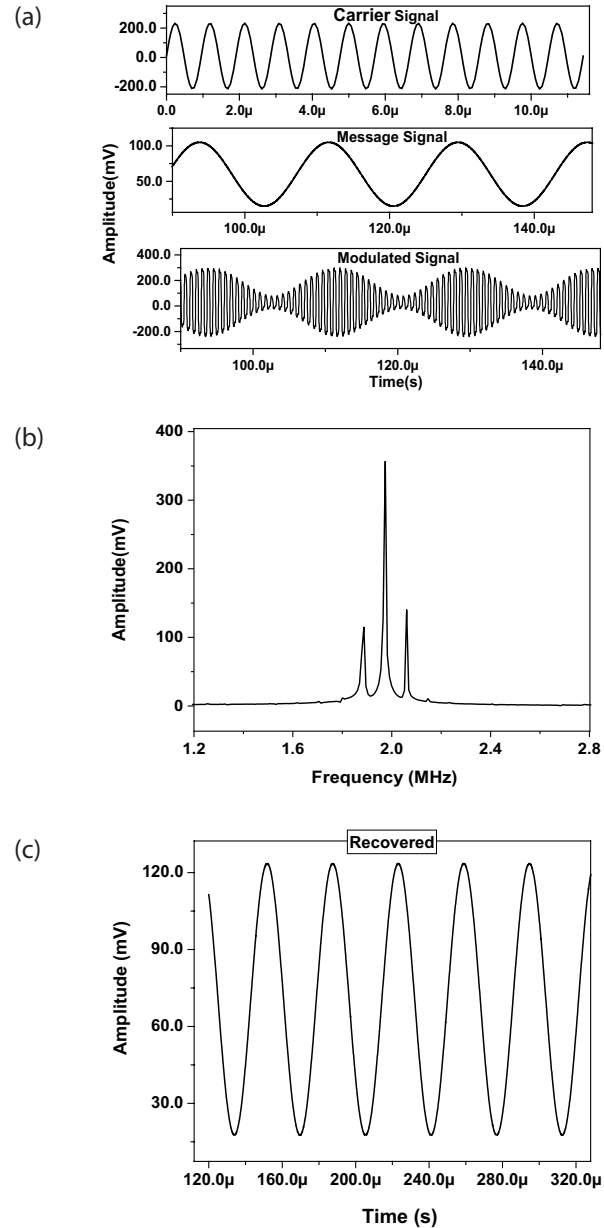| S.No.	Parameter	Value
1	Message signal amplitude Am	120 mV
2	Message signal frequency fm	50 kHz
3	Carrier signal amplitude Ac	240 mV
4	Carrier signal frequency fc	1 MHz
5	Band Pass filter center frequency	1 MHz
6	Band Pass Resistance (R1=R2=R5); these three resistances are being used in BPF as per Fig. 19(a) and Table 4	200 Ω
7	Band Pass Filter Capacitance (C_3=C_4)	150 pF
8	Capacitance C_1	32 pF
9	Capacitance C_2	150 pF
10	Local carrier amplitude	240 mV
11	Local carrier frequency fc	1 MHz
12	Low Pass filter cut-off frequency	50 kHz
13	Low Pass Resistance R_2	200 Ω
14	Low Pass Filter capacitance (C_1=C_3)	10 pF

amplitude variation of the carrier signal and follows the amplitude variation of the message signal. This means, the increment/decrement in hysteresis loop as visible in Figure 20(e) is corresponding to the variation in amplitude of message signal. From Figure. 20(e), we find that the hysteresis loops overlap each other on each half-cycle.
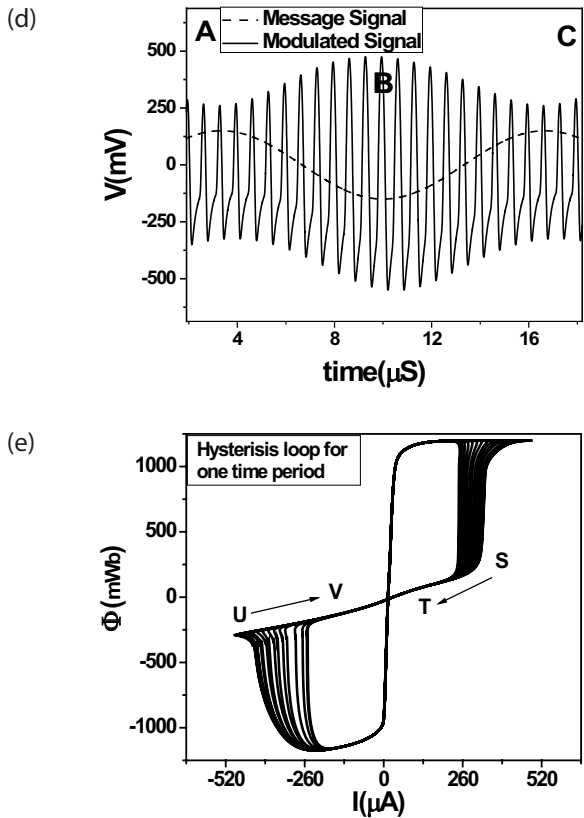
9 Experimental results

As monolithic implementations of the proposed meminductor are not available, the possible experimental realization of meminductors using commercially available ICs, AD844 and CA3080, is shown in Figure. 21 (a, b), followed by the assembled grounded meminductor

(a)

(b)

(c)

(d)

(e)

Figure 20: The plot of (a) carrier signal, message signal, and modulated signal, (b) spectrum of the modulated signal, (c) recovered message signal, (d) waveform of message and carrier for one period, (e) hysteresis loop of AM for one period.

emulator on a breadboard given in Figure. 21 (c). This circuit can broadly verify the functionality; however, detailed parameters are comparable with monolithic implementation. To verify experimentally, the proposed meminductor emulator is implemented with capacitance (C_1) as 40nF (in a parallel combination of four 10nF), resistance (R_1) of 100 Ω, and commercially available BJT-based OTA ICs (CA3080), and CFOA ICs (AD844). The pinched hysteresis loops of the emulator are obtained for the operating frequency of 820 kHz for a 4V peak-to-peak input signal, as shown in Figure. 22(a). Figure. 22(b) shows the pinched hysteresis loops for a floating meminductor (hardware implementation not shown) emulator at an operating frequency of 910 kHz for a 4V peak-to-peak input signal. Figure. 22(c) shows the time domain waveform for the grounded meminductor's current and charge (integral of current). Figure. 22(d) shows the time domain waveform for input phi (φ) and rho (ρ) (integral of phi) (using double integration in DSO) for the grounded meminductor. It can further be noted that both charge and rho (ρ) curves tend to increase as time increases which justifies that the proposed circuit is a meminductor. Figure.

22(e) shows the time domain waveform for flux and current for the grounded meminductor. Analysis of Figure. 22(e) reveals that the proposed circuit possesses a nonlinear relationship between flux and current and the relationship is not simultaneously zero all the time, just at one point simultaneously zero, thus verifying passivity.

(a)

(b)

(c)
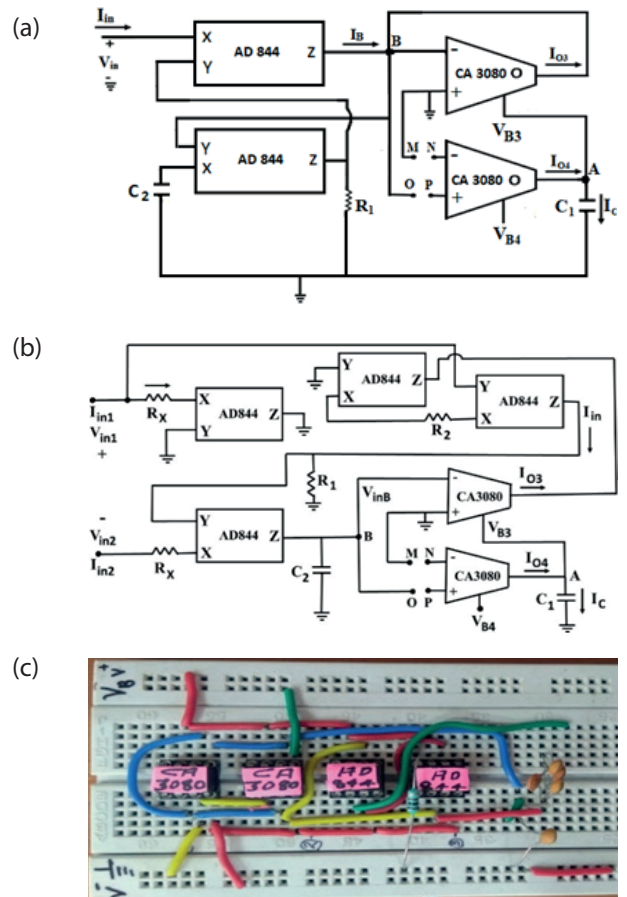
Figure 21: Meminductor emulator (a) Grounded Meminductor experimental circuit, (b) Floating Meminductor experimental circuit, (c) Prototype on a breadboard.

10 Conclusion

The proposed grounded and floating meminductor emulators show a pinched hysteresis loop and meminductive nature similar to an actual memindcutive device. Emulators have simple circuitry built with two OTAs and two CCII/CCCII. Proposed emulators are useful for a frequency of up to 1 MHz for grounded and 10 MHz for floating in both incremental and decremental topologies. The meminductance of the proposed emulators is electronically tunable with the bias voltage of OTA. The controllability of the pinched hysteresis loop and the meminductance nature of proposed emulators

for different frequencies of the input signal, capacitors, and external bias voltage is verified by simulation results. Layout, post-layout simulations, Monte Carlo, and detailed non-ideal analyses have also been carried out. Moreover, an AM modulator has been realized using the proposed meminductor emulator circuit as an application. Finally, a prototype of the proposed circuit

(a)

(b)

(c)

(d)

(e)

Figure 22: Experimental Results of meminductor emulator (a) hysteresis loop for grounded meminductor, (b) hysteresis loop for floating meminductor, (c) time domain waveform for Current (Green) and Charge (pink), (d) time domain waveform for phi (yellow) and rho (pink), (e) time domain waveform for phi (nonlinear) and current (sinusoidal).
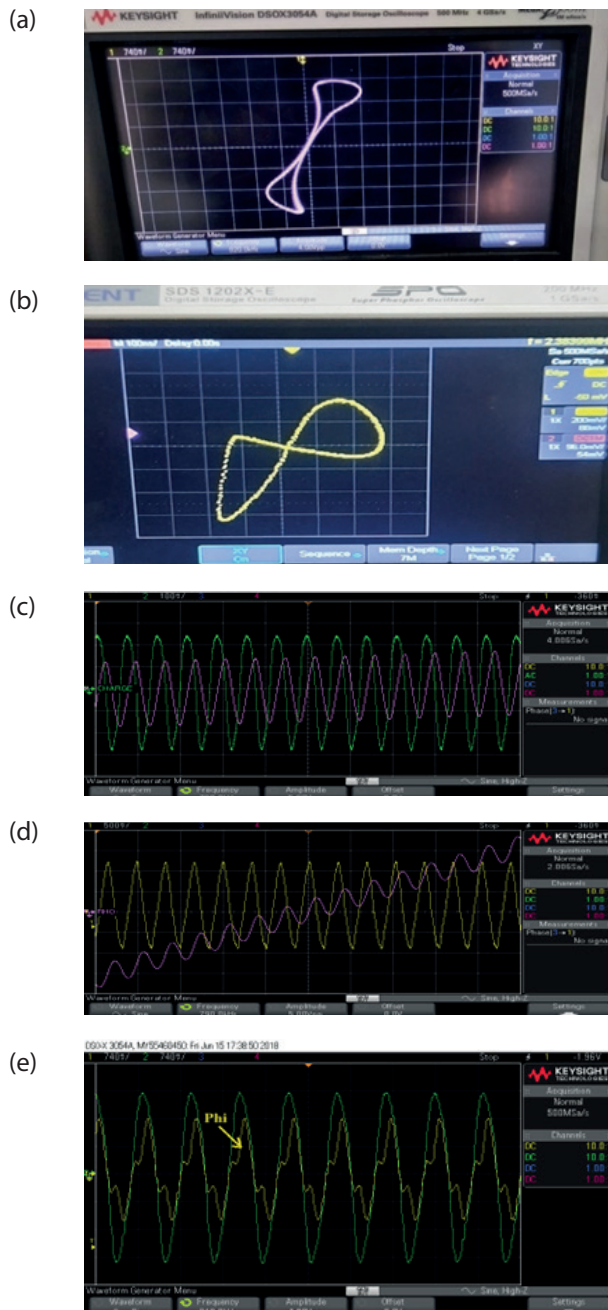
is assembled, and experimental results are given and discussed.

11 Conflict of interest

The authors declare no conflict of interest.

12 References

1. L. O. Chua, "Memristor- the missing circuit element," *IEEE Transaction on Circuit Theory*; vol. 18, no. 5, pp. 507-9, 1971. https://ieeexplore.ieee.org/abstract/document/1083337.
2. L. Chua, "Device modeling via nonlinear circuit elements," *IEEE Transactions on Circuits and Systems*; vol. 27, no. 11, pp. 1014-44, 1980. https://ieeexplore.ieee.org/abstract/document/1084742.
3. A. Scoli, R. Tetzlaff, and L. O. Chua, "The first ever real bistable memristors- Part II: Design and analysis of a local fading memory system," *IEEE Trans. Circuits Syst. II, Exp. Briefs;* vol. 63, no. 12, pp. 1096-1100, 2016. https://ieeexplore.ieee.org/abstract/document/7576621.
4. L. O. Chua, "Nonlinear circuit foundations for nanodevices. I. The four-element torus," *in IEEE proceedings, 2003, vol. 91, no.11, pp. 1830-59*. https://ieeexplore.ieee.org/abstract/document/1240074.
5. M. Di Ventra, Y. V. Pershin, L. O. Chua, "Circuit elements with memory: memristors, memcapacitors, and meminductors," in IEEE proceedings, 2009, vol. 97, no. 10, pp. 1717-24. https://ieeexplore.ieee.org/abstract/document/5247127.
6. Z. Yin, H. Tian, G. Chen, L. O. Chua, "What are memristor, memcapacitor, and meminductor?" *IEEE Transactions on Circuits and Systems II: Express Briefs.* vol. 62, no. 4, pp. 402-6, 2015. https://ieeexplore.ieee.org/abstract/document/7001208.
7. D. Biolek, Z. Biolek, V. Biolkova, "Pinched hysteretic loops of ideal memristors, memcapacitors, and meminductors must be 'self-crossing,'" *Electronics letters*, vol. 47, no. 25, pp. 1385-7, 2011. https://digital-library.theiet.org/content/journals/10.1049/el.2011.2913.
8. M. E. Fouda, A. G. Radwan, "Memristor-less current- and voltage-controlled meminductor emulators," in IEEE International Conference in Electronics, Circuits, and Systems (ICECS), 2014. https://ieeexplore.ieee.org/abstract/document/7049976.
9. M. P. Sah, R. K. Budhathoki, C. Yang, H. Kim, "Charge controlled meminductor emulator," *Journal of Semiconductor Technology and Science, vol.* 14, no. 6, pp. 750-4, 2014.

10. Y. Liang, H. Chen, D. S. Yu, "A practical implementation of a floating memristor-less meminductor emulator," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 61, no. 5, pp. 299-303, 2014. https://ieeexplore.ieee.org/abstract/document/6803850.

11. G. Y. Wang, P. P. Jin, X. W. Wang, Y. R. Shen, F. Yuan, X. Y. Wang, "A flux-controlled model of meminductor and its application in chaotic oscillator," *Chinese Physics B.* vol. 25, no. 9, pp. 090502, 2016. https://iopscience.iop.org/article/10.1088/1674-1056/25/9/090502/meta.

12. B. Xu, G. Wang , H. H. Iu, S. Yu, F. Yuan, "A memristor–meminductor-based chaotic system with abundant dynamical behaviors," *Nonlinear Dynamics*, vol. 96, no. 1, pp. 765-88, 2019. https://link.springer.com/article/10.1007/s11071-019-04820-1.

13. H. Sozen, U. Cam, "A novel floating/grounded meminductor emulator," *Journal of Circuits, Systems, and Computers, vol.* 29, no. 15, pp. 2050247, 2020. https://www.worldscientific.com/doi/abs/10.1142/S0218126620502473.

14. J. Vista, A. Ranjan, "High-frequency meminductor emulator employing VDTA and its application," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*; vol. 39, no. 10, pp. 2020-8, 2019. https://ieeexplore.ieee.org/abstract/document/8887199.

15. Y. Babacan, "An Operational Transconductance Amplifier-based Memcapacitor and Meminductor," *Electrica*; vol. 18, no. 1, pp. 36-8, 2018. https://dergipark.org.tr/en/pub/electrica/issue/35704/397840.

16. A. Raj, K. Kumar, P. Kumar, "CMOS realization of OTA based tunable grounded meminductor," *Analog Integrated Circuits and Signal Processing*, vol. 107, no. 2, pp. 475-82, 2021. https://link.springer.com/article/10.1007/s10470-021-01808-z.

17. A. Raj, S. Singh, P. Kumar, "Electronically tunable high-frequency single output OTA and DVCC based meminductor," *Analog Integrated Circuits and Signal Processing*, vol. 109, no. 1, pp. 47-55, 2021. https://link.springer.com/art-cle/10.1007/s10470-021-01913-z.

18. K. Kumar, B. C. Nagar, "New tunable resistor-less grounded meminductor emulator," *Journal of Computational Electronics*. vol. 20, no. 3, pp. 1452-60, 2021. https://link.springer.com/article/10.1007/s10825-021-01697-5.

19. N. Yadav, S. K. Rai, R. Pandey, "New high-frequency memristorless and resistorless meminductor emulators using OTA and CDBA" *Sādhanā*, vol. 47, no. 1, pp. 1-8, 2022. https://link.springer.com/article/10.1007/s12046-021-01785-z.

20. A. Singh, S. K. Rai, "OTA and CDTA-based new memristor-less meminductor emulators and their applications," *Journal of Computational Electronics*, pp. 1-2, 2022. https://link.springer.com/article/10.1007/s10825-022-01889-7.

21. N. Raj, R. K. Ranjan, F. Khateb, M. Kumngern, "Mem-elements emulator design with experimental validation and its application," *IEEE Access; vol.* 9, pp. 69860-75, 2021. https://ieeexplore.ieee.org/abstract/document/9425577.

22. A. Singh A, S. K. Rai, "VDCC-based memcapacitor/meminductor emulator and its application in adaptive learning circuit," *Iranian Journal of Science and Technology, Transactions of Electrical Engineering*; vol. 45, no. 4, pp. 1151-63, 2021. https://link.springer.com/article/10.1007/s40998-021-00440-x.

23. K. Bhardwaj K, M. Srivastava, "New grounded passive elements-based external multiplier-less implement emulator to realize the floating meminductor and memristor," *Analog Integrated Circuits and Signal Processing*; vol. 110, no. 3, pp. 409-29, 2022. https://link.springer.com/article/10.1007/s10470-021-01976-y

24. D. Biolek, V. Biolková, Z. Kolka, "Mutators are simulating memcapacitors and meminductors," in IEEE Asia Pacific Conference In Circuits and Systems (APCCAS), pp. 800-803, 2010. https://ieeexplore.ieee.org/abstract/document/5774993.

25. Y. V. Pershin, M. Di Ventra, "Memristive circuits simulate memcapacitors and meminductors," *Electronics Letters,* vol. 46, no. 7, pp. 517-8, 2010. https://arxiv.org/abs/0910.1583.

26. M. P. Sah, R. K. Budhathoki, C. Yang, H. Kim, "Mutator-based meminductor emulator for circuit applications," *Circuits, Systems, and Signal Processing*; vol. 33, no. 8, pp. 2363-83, 2014. https://link.springer.com/article/10.1007/s00034-014-9758-9.

27. D. Yu, Y. Liang, H. H. Iu, L. O. Chua, "A universal mutator for transformations among memristor, memcapacitor, and meminductor," *IEEE Transactions on Circuits and Systems II*: *Express Briefs*; vol. 61, no. 10, pp. 758-62, 2014. https://ieeexplore.ieee.org/abstract/document/6870446.

28. Z. G. Taşkıran, M. Sağbaş, U. E. Ayten, H. Sedef, "A new universal mutator circuit for memcapacitor and meminductor elements," *AEU-International Journal of Electronics and Communications*; vol. 119, pp. 153180, 2020. https://www.sciencedirect.com/science/article/abs/pii/S1434841119326196.

29. D. Biolek, Z. Biolek, V. Biolková, "PSPICE modeling of meminductor," *Analog Integrated Circuits and Signal Processing,* vol. 66, no. 1, pp. 129-37, 2011. https://link.springer.com/article/10.1007/s10470-010-9505-5.

30. H. Zhu, S. Duan, L. Wang, T. Yang, J. Tan, "The non-linear meminductor models with its study on the device parameters variation," *in 7th IEEE International Conference in Information Science and Technology (ICIST), 2017,* pp. 497-503. https://ieeexplore.ieee.org/abstract/document/7926811.

31. H. Yao, S. Duan, L. Wang, "Composite behaviors of series and parallel meminductor circuits," *in 5th IEEE International Conference in Information Science and Technology (ICIST), 2015,* pp. 439-444. https://ieeexplore.ieee.org/abstract/document/7289012.

32. Z. Hu, Y. Li, L. Jia, J. Yu, "Chaotic oscillator based on current-controlled meminductor," *In IEEE international conference Communications, Circuits, and Systems (ICCCAS), 2010,* pp. 820-823.

33. F. Yuan, G. Wang, X. Wang, "Chaotic oscillator containing memcapacitor and meminductor and its dimensionality reduction analysis," *Chaos: An Interdisciplinary Journal of Nonlinear Science*; vol. 27, no. 3, pp. 033103, 2017. https://ieeexplore.ieee.org/abstract/document/1083337.

34. B. Xu, G. Wang, Y. Shen, "A simple meminductor-based chaotic system with complicated dynamics," *Nonlinear Dynamics*; vol. 88, no. 3, pp. 2071-89, 2017. https://link.springer.com/article/10.1007/s11071-017-3363-y.

35. A. Arora, V. Niranjan, "Low power filter design using memristor, meminductor, and memcapacitor," in 4th IEEE Uttar Pradesh Section International Conference In Electrical, Computer, and Electronics (UPCON), 2017, pp. 113-117. https://ieeexplore.ieee.org/abstract/document/8251032.

36. Parveen, Tahira, "Textbook of Operational Transconductance Amplifier and Analog Integrated Circuits," IK International Pvt Ltd, 2013, pp. 5-6.

37. J. C. Whitaker, editor, "The electronics handbook," CRC Pres 8s; 1996, pp. 666-669.

38. T. Deliyannis, Y. Sun, J. K. Fidler, "Continuous-time active filter design," *CRC Press*; 1998, pp. 241-244.

39. B. Al-Hashimi, "Current mode filter structure based on dual output transconductance amplifiers,"*Electronics Letters*; vol. 32, no. 1, pp. 25-26, 1996. https://eprints.soton.ac.uk/251347/.

40. F. Khateb, N. Khatib, D. Kubanek, "Low-Voltage Ultra-Low-Power Current Conveyor Based on Quasi-Floating Gate Transistors," *Radioengineering*, vol. 21, no. 2, 2012. https://dspace.vutbr.cz/bitstream/handle/11012/37116/12_02_0725_0735.pdf?sequence=1.