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# Design and Optimization of Multiple-Channel Double Dynamic Switching Biased Op-Amp for Switched Capacitor Integrator Using FinFET Technology

*Morteza Babaeian Far[1], Mehmet Aytuğ Ormancı[1,2], Fırat Kaçar[1]*

*[1]Department of Electrical and Electronics Engineering, Istanbul University–Cerrahpaşa, Avcilar, Istanbul, Türkiye*
*[2]Department of Electronics and Communication Engineering, Istanbul Technical University, Maslak, Istanbul, Türkiye*

**Abstract:** This paper presents the design and optimization of a parametric multiple-channel Double Dynamic Switching Biased Complementary Folded-Cascode Amplifier with switched capacitor integrator application in 32nm FinFET technology. The LTspice simulations demonstrate that the amplifier can attain an open-loop DC gain of 44.8dB, and a phase margin of about 87.8° with ±0.5V supply voltages. Moreover, the amplifier power consumption is measured 246µW including bias circuitry and a Gain-Bandwidth Product (GBW) of 77.45MHz under a 5pF load capacitor. The circuit's stability enables it to offer diverse design capabilities tailored to specific application needs. This novel design is capable of reducing supply voltages and power dissipation.

**Keywords:** 32nm FinFET Technology, Complementary Folded-Cascode Amplifier, Double Dynamic Switching Bias, Self-Cascode, Switched Capacitor

# Načrtovanje in optimizacija večkanalnega dvojnega dinamičnega preklopnega optičnega ojačevalnika za stikalni kondenzatorski integrator z uporabo tehnologije FinFET

**Izvleček:** Članek predstavlja načrtovanje in optimizacijo parametričnega večkanalnega ojačevalnika z dvojnim dinamičnim preklopom, ki se opira na komponente z zloženo kaskodo, z uporabo integratorja s preklopnim kondenzatorjem v 32 nm tehnologiji FinFET. Simulacije LTspice kažejo, da lahko ojačevalnik doseže ojačenje z odprto zanko DC 44,8 dB in fazno rezervo približno 87,8° pri napajalnih napetostih ±0,5 V. Poleg tega je izmerjena poraba energije ojačevalnika 246 µW, vključno z napajalnim vezjem in GBW 77,45 MHz pri obremenitvenem kondenzatorju 5pF. Stabilnost vezja omogoča diverzno načrtovanje s prilagoditvami glede na potrebe aplikacije. Ta nova zasnova lahko zmanjša napajalne napetosti in porabo.

**Ključne besede:** 32nm FinFET tehnologija, komplementarni kaskodni ojačevalnik, Dvojno dinamično preklapljanje polarizacije, Preklopni kondenzator

* Corresponding Author's e-mail: fkacar@iuc.edu.tr

## 1 Introduction

In semiconductor technology, the constant search for smaller, faster, and more energy-efficient transistors has driven technological innovation. Recent advances at the nanoscale level and the advent of multi-gate transistors have ushered in a new era of complexity in the design process. One such breakthrough technology that has attracted significant attention in the integrated circuit (IC) design industry is FinFET transistors. These transistors offer promising solutions to the challenges of shrinking device dimensions and enable performance and efficiency in modern semiconductor devices.

On the other hand, the relentless pursuit of miniaturization and performance improvement in electronic circuits extends beyond transistors to encompass various facets. Market demands and the push for advancements in portable electronics have compelled the industry to develop circuits with low voltage (LV) requirements and often restricted power consumption, presenting a significant challenge. Many emerging products must operate at voltages of 3V or lower to stay competitive in an industry characterized by rapid turnover [1]. Implantable medical electronic devices, especially those incorporating analog and digital circuits, are prime examples of this scenario.

In this competitive landscape, numerous proven techniques are used in innovative circuit design as essential for market viability. For instance, companies are increasingly utilizing CMOS switched capacitor (SC) methods for implementing analog signal processing integrated circuits (ICs) due to their effectiveness. Previous research has demonstrated the effectiveness of utilizing SC techniques with CMOS operational amplifiers (Op-Amps) to implement analog functions such as filters [2-4]. However, using multiple Op-Amps often creates significant power consumption, potentially leading to operational instability. To mitigate power dissipation associated with Op-Amps, various strategies including reduced supply voltages, bulk-driven topologies, floating-gate transistors, self-cascode structures, and subthreshold designs have been explored [1, 5].

In achieving high-speed operation, it is crucial to carefully address design considerations regarding distortion alongside the increase in power dissipation. This necessity arises from the intrinsic capability of Op-Amps to process analog signals. On the other hand, prior research has introduced a CMOS Folded-Cascode (FC) Op-Amp with a Double Dynamic Switching Biased (DDSB) in a simplified configuration to ensure minimal power consumption while maintaining switching capability [2]. This amplifier exhibits high power dissipation and occupies significant physical space. Operating with a supply voltage of 3V and consuming 9.2mW of power, it is suitable for signal processing applications. However, integrating it as an element in new-generation devices may pose challenges.

This study discusses the development of a Complementary Folded-Cascode (CFC) Op-Amp, designed to operate with a supply voltage of 1V (±0.5V) and achieve operational performance with a power consumption level of 246µW. PTM 32nm FinFET technology was chosen for the designs to leverage its advantages, including lower power consumption, higher density, improved scaling, enhanced reliability, and compatibility with future advancements in semiconductor technology. In line with FinFET technology, the self-cascode structure was employed, enabling both an increase in output resistance and the ability to design at lower voltages. This feature enables the design to have parametric flexibility. Moreover, integrating the DDSB circuit in [2] helps reduce undesirable phenomena such as noise and process variations, consequently enhancing the overall performance and stability. The stability and performance of the proposed circuit under various conditions were analyzed using the SC integrator application, yielding the expected triangle behavior.

In this paper, Section 2 elaborates on the FinFET, the integration of the self-cascode structure with FinFET, and the development of the CFC Op-Amp with DDSB. Section 3 provides details on the SC integrator topology and its FinFET-based design. Additionally, this section discusses the performance evaluation of the integrator, while Section 4 summarizes the conclusions. Results obtained reveal that the novel design employed in the present study can reduce the amount of supply voltages and power dissipation.

## 2 Design of CFC Op-Amp

### 2.1 FinFET

The inception of FinFET-like structures traces back to the introduction of a Fully Depleted Lean Channel Transistor (DELTA) by Hisamoto et al. in 1989 [6, 7], highlighting the longstanding pursuit of enhanced transistor architectures. The distinctive three-dimensional structure of FinFETs, with a thin silicon body formed perpendicular to the wafer plane, enables superior electrostatic control and reduced leakage compared to traditional planar MOSFETs [8]. FinFET transistors, operating at nanoscale dimensions, exhibit reduced Drain-Induced Barrier Lowering (DIBL) and mitigated other Short-Channel Effects (SCEs), thereby enhancing overall performance and reliability [9]. This translates to higher on-state current, lower leakage, and faster switching speeds, making FinFETs an attractive option for many applications. Moreover, the fabrication process for FinFET transistors is compatible with conventional CMOS processes, enabling seamless integration into existing technologies.

Overall, FinFETs operate via three primary mechanisms: independent-gate (IG) connection, shorted-gate (SG) connection, and low-power (LP) mode [10]. As depicted in Fig. 1(a), the SG type features a three-terminal device. SG FinFETs present a promising alternative to MOSFETs, offering increased on-state current and faster transition speeds, thus enhancing performance. Moreover, robust gate control provides enhanced suppression against SCEs and gate-dielectric leakage. A thick masking oxide, $T_{mask}$, can be utilized to enable the operation of the devices as Double-Gate (DG) FinFETs, with sidewall gates providing electrical functionality exclusively.

The IG type eliminates the upper portion of the gate to create two separate gates, as shown in Fig. 1(b). Operating as a four-terminal device, this configuration allows the front and back gates to be coupled to dis-

tinct inputs. Consequently, the IG FinFET can function as a pair of parallel transistors, enhancing design flexibility and significantly reducing the number of transistors. LP mode is an exception to the typical behavior of the IG mode, effectively reducing threshold leakage by adjusting the back gate voltage, as noted in [8]. Further details on the operation modes can be found in [10].

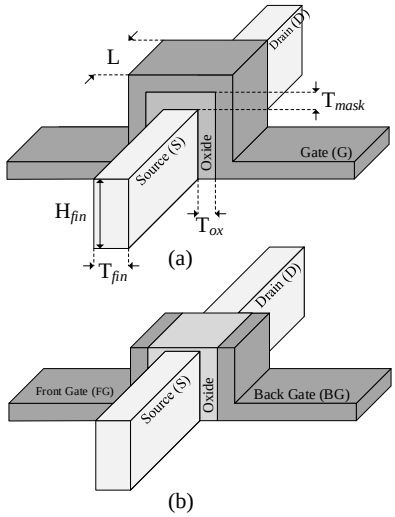


Figure 1: FinFET connection types: a): shorted-gate, b): independent-gate.

For a DG-FinFET, when the biasing condition is appropriate, current flows from the source to the drain under the influence of the corresponding sidewall gates, spanning the height $H_{fin}$ of each fin. Consequently, the width (W) of the FinFET structure depends on the height of the fins. For a single-fin DG-FinFET, the total width can be determined as in equation (1).

$$W = 2H_{fin} \tag{1}$$

This study presents an Op-Amp design utilizing IG FinFETs operating in LP mode. The simulations are based on the Predictive Technology Model (PTM) for 32nm FinFETs. PTM is selected as the simulation model due to its comprehensive coverage of physical effects and excellent scalability. This approach enables precise predictions and enhances efficiency in circuit design. Overall, the combination of the Op-Amp design with the self-cascode structure for IG FinFETs in LP mode, supported by PTM, presents a promising approach for optimizing circuit performance in advanced semiconductor technologies [8].

## 2.2 Self-Cascode Structure

The self-cascode configuration is depicted in Fig. 2 as a two-transistor setup, which can be viewed as an individual composite transistor. This composite structure exhibits a significantly extended effective channel length and output resistance. The lower transistor, referred to as $F_{2a}$, functions as an input-dependent resistor. To maintain optimal performance, the W/L ratio of $F_{2b}$ is set more significantly larger than that of $F_{2a}$, denoted as C>1 [5].

Fig. 3 illustrates the results obtained by adjusting the structure using the parameters Composite (C) and Multiplier (M). One notable observation is the increased output resistance compared to configurations utilizing a single FinFET as expected. Increasing the value of C, which solely enlarges the size of $F_{2b}$, leads to elevated output resistance. Similarly, increasing the value of M enlarges both FinFETs within the self-cascode structure, thereby increasing the current.

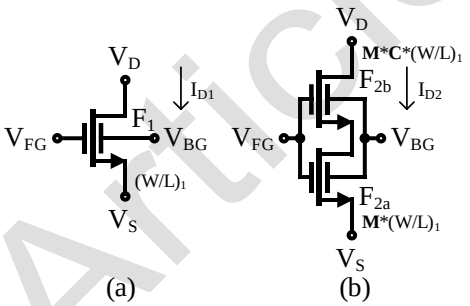


Figure 2: a) Single FinFET, b) Self-cascode structure.

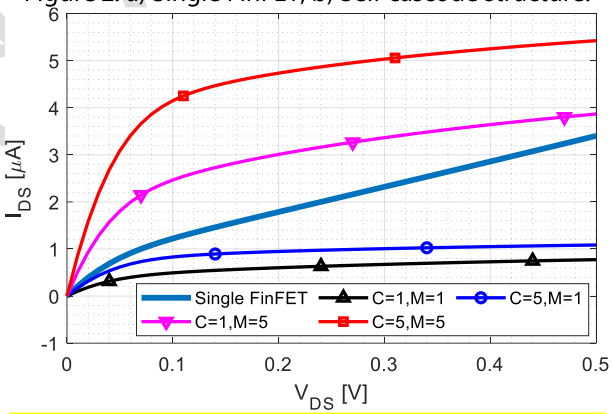


Figure 3: Operational outcomes for both single FinFET and self-cascode structures under various parameters (@$V_{FG}$=0.5V, @$V_{BG}$=$V_S$=GND, $W_1/L_1$=80nm/64nm).

## 2.3 Proposed CFC Op-Amp

Fig. 4 illustrates the proposed CFC Op-Amp configuration. The operational amplifier is biased with a DDSB circuit for low power consumption. To enhance input common mode voltage, a CFC is implemented, which consists of parallel-connected self-cascoded FinFETs $F_{1Aa}$-$F_{1Ab}$, $F_{2Aa}$-$F_{2Ab}$ and self-cascoded FinFETs $F_{1a}$-$F_{1b}$, $F_{2a}$-$F_{2b}$ differential input pairs. For the differential input, the current sources are self-cascoded FinFETs $F_{3Aa}$-$F_{3Ab}$ and $F_{3a}$-$F_{3b}$. Instead of a traditional cascode current mirror, a wide-swing cascode current mirror is selected to ensure a broad dynamic range, even at reduced supply voltages [6].

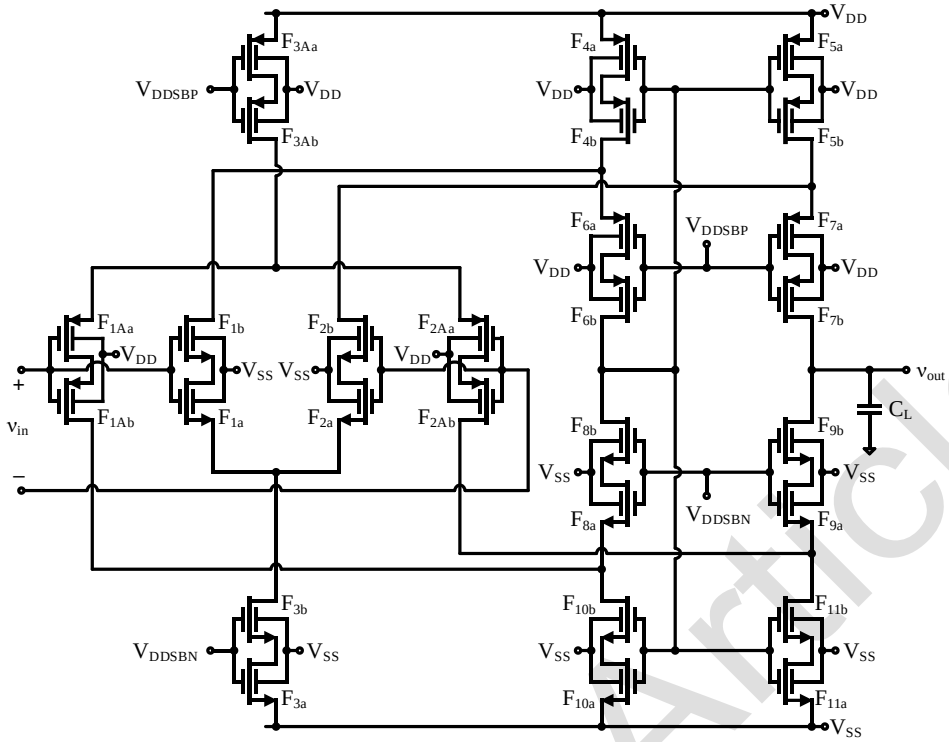


Figure 4: Proposed CFC Op-Amp configuration.

The low-frequency gain of the proposed circuit can be determined by $A_v = g_{mT}R_o$. Here $g_{mT}$ is the total transconductance of the input stage, which is given in (2).

$$g_{mT} = g_{mN} + g_{mP} = g_{m(2a-2b)} + g_{m(2Aa-2Ab)} \quad (2)$$

The output resistance, $R_o$, which indicates the small-signal resistance seen from the drain of $F_{7a}$-$F_{7b}$ and $F_{9a}$-$F_{9b}$, can be calculated using the parallel combination of (3a) and (3b) [6, 12].

$$R_{oN} = g_{m(9a-9b)}r_{o(9a-9b)}\left[r_{o(2Aa-2Ab)}r_{o(11a-11b)}\right] \quad (3a)$$

$$R_{oP} = g_{m(7a-7b)}r_{o(7a-7b)}\left[r_{o(2a-2b)}r_{o(5a-5b)}\right] \quad (3b)$$

Fig. 5 illustrates the configuration of the DDSB. In the circuit, the initial group of FinFETs $F_{B1}$-$F_{B4}$ manages the activation state of self-cascoded current source (i.e., $F_{3Aa}$-$F_{3Ab}$) and self-cascoded FinFETs $F_{6a}$-$F_{6b}$, $F_{7a}$-$F_{7b}$ within the CFC Op-Amp by regulating the bias voltage $V_{DDSBP}$. This modulation spans approximately –160mV to 320mV and is achieved through a designated control pulse, $\Phi_{BP}$. Similarly, the subsequent group $F_{B5}$-$F_{B8}$ oversees the activation status of self-cascoded current source (i.e., $F_{3a}$-$F_{3b}$) and self-cascoded FinFETs $F_{8a}$-$F_{8b}$, $F_{9a}$-$F_{9b}$ by adjusting the bias voltage $V_{DDSBN}$ within a range of approximately –120mV to –380mV, controlled by pulse designated as $\Phi_{BN}$.

The operating waveforms of DDSB clocks are depicted in Fig. 6a, while the output voltages are shown in Fig. 6b. As indicated by their shape, the Op-Amp is designed to turn off at 100ns and then turn on again simultaneously. This integration helps mitigate side effects and provides better stability with low power consumption [2] for the proposed Op-Amp. The transistor dimensions utilized in the DDSB CFC Op-Amp are provided in Table 1.

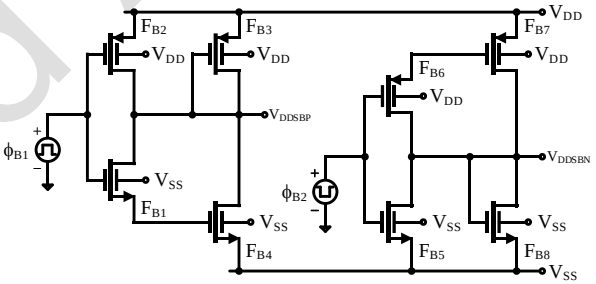


Figure 5: Configuration of the DDSB [2].

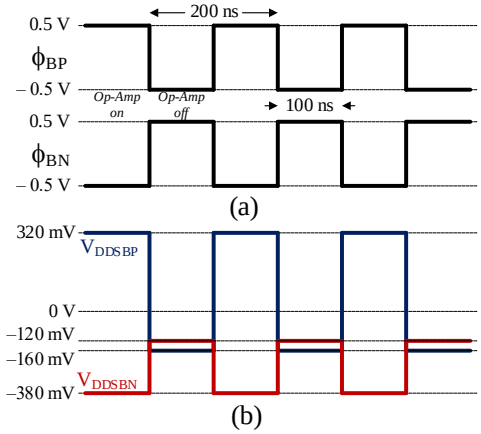


Figure 6: a) Operation waveforms of the DDSB clocks, b) DDSB outputs.

Table 1: Transistors' aspect ratios.

| FET | W/L (nm/nm) | FET | W/L (nm/nm) |
|---|---|---|---|
| $F_{1Aa}$ | (1520*M)/64 | $F_{7a}$ | (800*M)/64 |
| $F_{1Ab}$ | (1520*M*C)/64 | $F_{7b}$ | (800*M*C)/64 |
| $F_{1a}$ | (1520*M)/64 | $F_{8a}$ | (450*M)/64 |
| $F_{1b}$ | (1520*M*C)/64 | $F_{8b}$ | (450*M*C)/64 |
| $F_{2Aa}$ | (1520*M)/64 | $F_{9a}$ | (450*M)/64 |
| $F_{2Ab}$ | (1520*M*C)/64 | $F_{9b}$ | (450*M*C)/64 |
| $F_{2a}$ | (1520*M)/64 | $F_{10a}$ | (500*M)/64 |
| $F_{2b}$ | (1520*M*C)/64 | $F_{10b}$ | (500*M*C)/64 |
| $F_{3Aa}$ | (420*M)/64 | $F_{11a}$ | (500*M)/64 |
| $F_{3Ab}$ | (420*M*C)/64 | $F_{11b}$ | (500*M*C)/64 |
| $F_{3a}$ | (650*M)/64 | $F_{B1}$ | 200/64 |
| $F_{3b}$ | (650*M*C)/64 | $F_{B2}$ | 200/64 |
| $F_{4a}$ | (500*M)/64 | $F_{B3}$ | 64/64 |
| $F_{4b}$ | (500*M*C)/64 | $F_{B4}$ | 180/64 |
| $F_{5a}$ | (500*M*C)/64 | $F_{B5}$ | 250/64 |
| $F_{5b}$ | (500*M*C)/64 | $F_{B6}$ | 80/64 |
| $F_{6a}$ | (800*M*C)/64 | $F_{B7}$ | 200/64 |
| $F_{6b}$ | (800*M*C)/64 | $F_{B8}$ | 300/64 |

M: Multiplier, C: Composit

### *2.4 Simulation Results*

The performance of the DDSB CFC Op-Amp was evaluated through simulations using the LTspice software. Increasing the C value results in elevated output resistances, as depicted in Fig. 3, subsequently boosting the circuit's gain. Likewise, increasing the M value enlarges both FinFETs within the self-cascode structure, thereby raising the current and consequently expanding the bandwidth. Thanks to the stability maintained by DDSB, this structure proposed in the paper enables the design to be tailored to different purposes and needs. It is important to note that increasing the values of C and M enhances the circuit's performance, but it also leads to an increase in layout size and power dissipation. For C=5 and M=5, the results reveal a gain of 44.88dB, a bandwidth of 42.1kHz, a Unity Gain Frequency (UGW) of 77.45MHz, and a phase margin of 87.8° with 5pF load capacitance. The AC response of the circuit for four different scenarios, based on variations in C and M, is illustrated in Fig. 7. The circuit's Common-Mode Rejection Ratio (CMRR) and comprehensive input-referred noise characteristics across a wide frequency band are presented in Fig. 8. When the parameters are set to C=1 and M=1, the CMRR reaches 50.62dB. Noise analysis at these dimensions indicates that the circuit exhibits input noise voltage densities of 3.6μV/√Hz at 100Hz and 161.5nV/√Hz at 1MHz. Specifically, the input-referred noise voltage density increases with the rise in the C coefficient, while it decreases with the increase in the M coefficient at frequencies close to DC. By analyzing the frequency response diagrams for voltage gain, phase margin, CMRR, and noise, as shown in Figs. 7 and 8, the performance of the designed amplifier for different values of C and M is compared in Table 2.

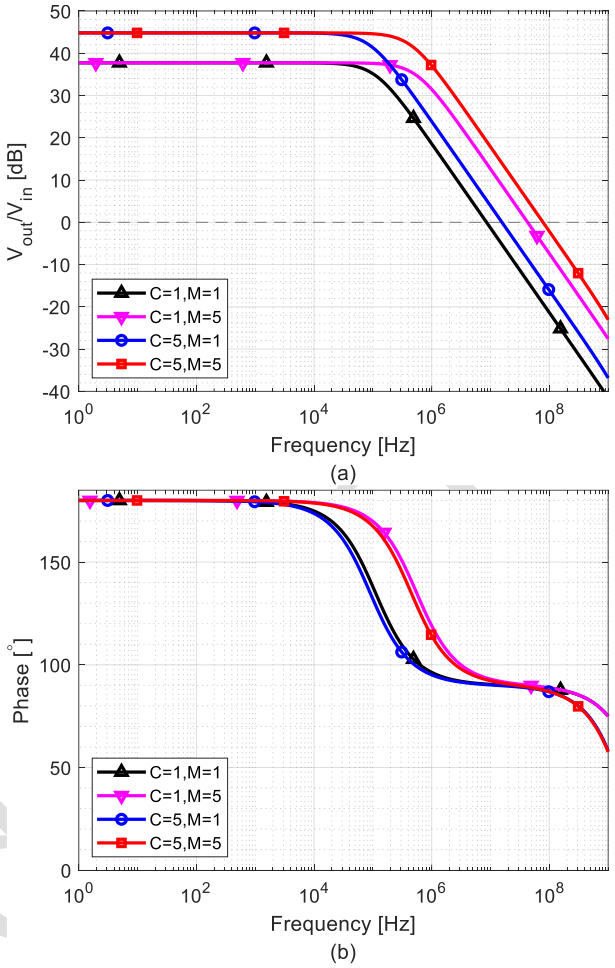


Figure 7: AC response of proposed Op-Amp: a) gain, b) phase.

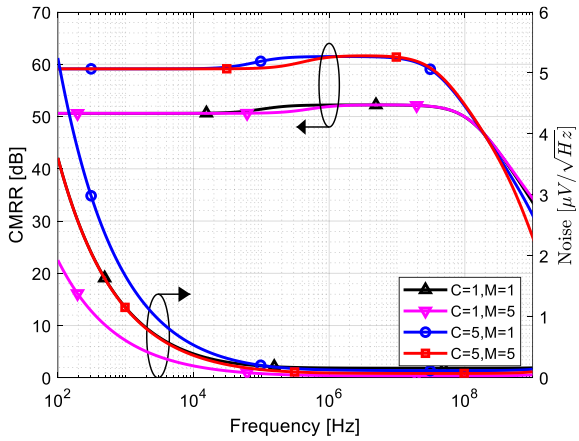


Figure 8: CMRR and input referred noise performance results of the proposed Op-Amp.

Figure 9 illustrates the variation in the Gain-Phase characteristics of the circuit with respect to $C_L$ and temperature. In Figure 9a, it is observed that for C=1 and M=1, increasing $C_L$ from 0.5pF to 5pF results in a UGW of 87.1MHz with a load of 0.5pF, maintaining stability with a phase margin of 89.4°. Further analysis shows that with $C_L$=10fF, the circuit achieves a UGW of 3.19GHz and a phase margin of 44.93°. When the para-

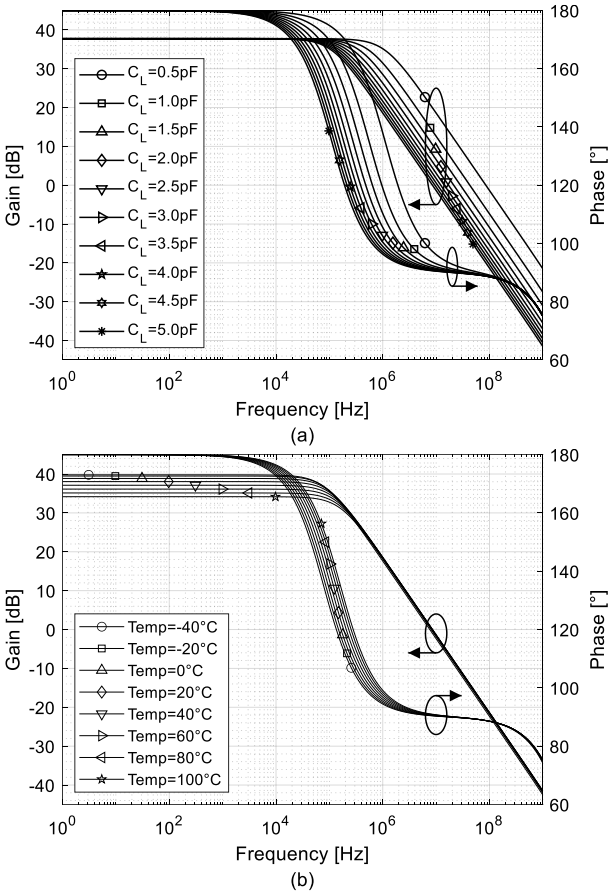


Figure 9: Gain-phase response variation (@C=1, M=1): a) with $C_L$, b) with temperature.

meters are set to C=5 and M=5, the circuit remains stable up to a load capacitance of approximately 220fF, providing a UGW of 1.38GHz and a phase margin of 45.5° for this load. The frequency response of the Op-Amp was analyzed over a wide temperature range from -40°C to 100°C, with simulations conducted at 20°C intervals as depicted in Fig. 9b. Under the conditions of C=1 and M=1, the gain and phase characteristics at -40°C are 39.8dB and 90.5°, respectively, while at 100°C they are 34.2dB and 90.1°. This indicates that the small-sized Op-Amp exhibits low sensitivity to thermal variations. This stability across the temperature range decreases as the Op-Amp size is increased.

In this paper, the slew rate (SR) was determined by using an 800mV peak-to-peak input (–400mV to 400mV) employing a 10-90% threshold. Fig. 10 shows the step response of the Op-Amp under varying load capacitances (CL) from 1 pF to 5 pF. The simulation results indicate that the circuit provides a stable output due to the high phase margin. The fluctuations in the transition band are caused by the operation of the DDSB, which continuously switches the circuit on and off. This behavior is also observed during rising and falling transitions and presents a disadvantage by reducing the SR. For a 1pF load capacitor, the measured

Table 2: Performances of the DDSB CFC Op-Amp.

| Parameters | Unit | C=1 M=1 | C=5 M=1 | C=1 M=5 | C=5 M=5 |
|---|---|---|---|---|---|
| Open Loop Gain (DC) | dB | 37.42 | 44.80 | 37.72 | 44.88 |
| Phase Margin | ° | 90.66 | 89.85 | 90.10 | 87.8 |
| UGW | MHz | 8.46 | 14.82 | 43.15 | 77.45 |
| CMRR | dB | 50.62 | 59.16 | 50.61 | 59.13 |
| Input Ref. Noise (a/b) | $\frac{nV}{\sqrt{Hz}}$ | 3607/ 161.5 | 5246/ 128.9 | 1930/ 36.4 | 3605/ 79.4 |
| Output Ref. Noise (a/b) | $\frac{\mu V}{\sqrt{Hz}}$ | 277.6 /1.37 | 912.4 /2.01 | 148.6 /1.36 | 627/ 5.66 |
| Power Dis. | mW | 0.083 | 0.097 | 0.179 | 0.246 |

$C_L$=5pF, [a]: @100Hz, [b]: @1MHz

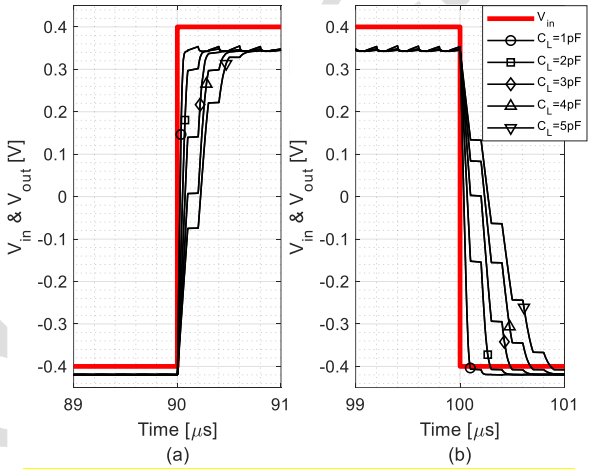


Figure 10: Step response of proposed Op-Amp for C=1, M=1: a) $SR^+$ b) $SR^-$.

$SR^+$ ($SR^-$) is 12.8 (9.3)V/µs for C=1, M=1, while for C=5, M=5, it increases to 97 (68.6)V/µs. When $C_L$ is increased to 5pF, the $SR^+$ ($SR^-$) values decrease to 2.41 (1)V/µs for C=1, M=1, and to 32.2 (14.3)V/µs for C=5, M=5.

Monte Carlo (MC) analysis, conducted in LTspice over 50 iterations, investigated the impact of three key parameters on the circuit's performance: threshold voltage ($V_{TH}$), oxide thickness ($t_{ox}$), and supply voltages ($V_{DD}$, $V_{SS}$). The analyses are provided insight into how minor deviations in these parameters influence the overall behavior and stability of the circuit. The results are depicted in the Fig. 11 for C=1 and M=1.

Table 3 compares Op-Amps from the literature using CMOS and FinFET technologies with the proposed DDSB CFC Op-Amp configurations (@C=1, M=1 and @C=5, M=5). To facilitate a comparison of truly low-power structures, the two Figures of Merit (FoM1,2), as utilized in [13], have been employed regarding small-signal and large-signal power.

$$FoM_1 = \frac{GBW \cdot C_L}{P_{diss}} \quad (4a)$$

$$FoM_2 = \frac{SR_a \cdot C_L}{P_{diss}} \quad (4b)$$

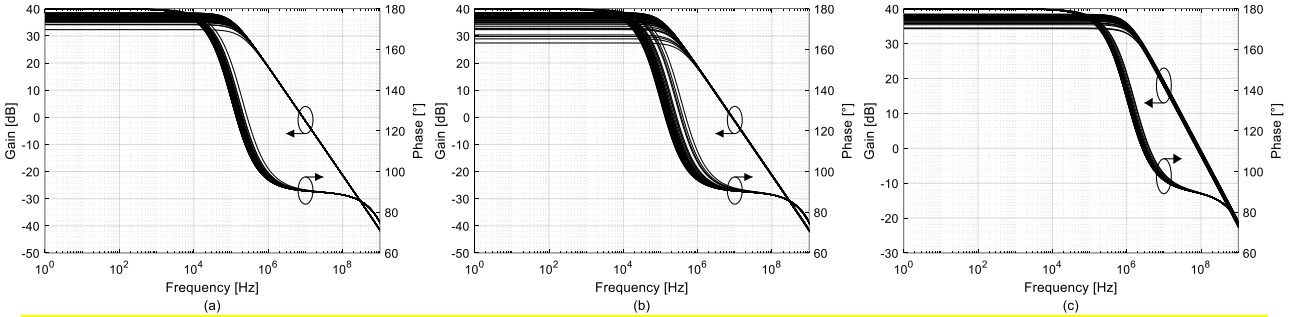


Figure 11: MC Analysis results: a) $t_{ox}$ with 3% variation, b) $V_{TH}$ with 1% variation, c) Power supplies ($V_{DD}$, $V_{SS}$) with 5% variation.

Table 3: Performance comparison of proposed Op-Amp with literature.

| Performance Parameters | Unit | This Work[2] | This Work[3] | [2] | [6] | [14] | [15] | [16] | [17] |
|---|---|---|---|---|---|---|---|---|---|
| Process | N/A | 32 nm (FinFET) | 32 nm (FinFET) | 1 µm (CMOS) | 0.6 µm (CMOS) | 0.18 µm (CMOS) | 20 nm (FinFET) | 55nm (FinFET) | 45nm (FinFET) |
| Power Supply | V | ±0.5 | ±0.5 | ±1.5 | 1.8 | 1.8 | ±0.5 | 1 | 1 |
| Power Dissipation | mW | 0.083 | 0.246 | 9.2 | 0.24 | 1.18 | 0.377 | 0.648 | 0.175 |
| $C_L$ | pF | 5 | 5 | 10 | 20 | 8 | 3 | 3 | 0.02 |
| Open Loop Gain (DC) | dB | 37.42 | 44.8 | 47.7 | 80.8 | 68 | 39.27 | 45.51 | 29.22 |
| GBW | MHz | 8.46 | 77.45 | 14.3 | 6.9 | 172.5 | 8.26 | 63 | 5.1 |
| Phase Margin | ° | 90.66 | 87.8 | 47.9 | 71 | 48.2 | 45.05 | 60.1 | 90 |
| Slew Rate ($SR^+/SR^-$)[1] | V/µs | 2.41/1 | 32.2/ 14.3 | 106 | 2.2 | 212.5 | 2.3 | 41.34 | 1830/ 1120 |
| FoM1 | $\frac{\text{MHz}\cdot\text{pF}}{\text{mW}}$ | 509.64 | 1574 | 15.54 | 575 | 1169 | 65.72 | 291.66 | 0.582 |
| FoM2 | $\frac{\text{V}\cdot\text{pF}}{\mu\text{s}\cdot\text{mW}}$ | 103.01 | 472.56 | 115.21 | 183.33 | 1440 | 18.30 | 191.38 | 168.57 |

[1]: For articles with a single SR, SRa=SR was considered, [2]: C=1, M=1, [3]: C=5, M=5.

Where SRa=($SR^+$+$SR^-$)/2 represents the average value of slew rates of rising and falling edges of the output. It should be noted that $FoM_1$ and $FoM_2$ relate small-signal gain bandwidth and slew rate to dissipation power.

When comparing the data in Table 3, it can be observed that the proposed circuit (C=5, M=5) outperforms other published circuits in terms of FoM1, providing 1574(MHz·pF)/mW. Regarding FoM2, the value of 1440(V·pF)/(µs·mW) from reference [14] stands out. The advantage of this study lies in its design, which includes a slew rate enhancement block aimed at achieving a high slew rate. However, the low phase margin value of 48.2° achieved by this circuit with 8pF load capacitance is a significant factor, and the likelihood of unstable operation increases with lower capacitive loads.

## 3 SC integrator application

Switched capacitor (SC) circuits are fundamental components in the construction of integrated circuits that find extensive application in a variety of domains, including voltage regulators, filters, and analog-to-digital converters. The principle behind SC circuits involves capacitors' periodic charging and discharging to perform specific signal-processing tasks. A SC circuit comprises a core network of capacitors, switches, and operational amplifiers. Switches control the connection and disconection of capacitors in the circuit and enable charge transfer between them. By opening and closing these switches at precise intervals, the circuit effectively mimics the behavior of resistors or other analog components. The history of SC circuits dates back to the middle of the 20th century, stemming from the need for more efficient analog signal processing methods. SC circuits use discrete components such as relays and mechanical switches to implement switching [18]. As discussed previously, the substitution of a resistor can be achieved by utilizing two FinFETs and a capacitor connected at a single node. The insensitive SC integrator, utilizing FinFETs as shown in Fig. 12An independent, non-overlapping clock signal controls each gate pin of the two FinFETs. This system operates under the assumption that the output is sampled at the conclusion of the $\phi_2$ clock phase. Under this assumption, the transfer function of the integrator can be derived as given in (5) [19, 20].

$$\frac{v_o}{v_i} = \frac{C_1/C_2}{j\omega T}\left[\frac{\omega T}{2\sin\left(\frac{\omega T}{2}\right)}\right] \quad (5)$$

Here $T$ represents the period of sampling. The operation waveforms of the SC clocks are depicted in Fig. 13.

The total equivalent resistance in the circuit is set to 250kΩ. The capacitors used in the circuit, $C_1$ and $C_2$, each have a capacitance of 40pF. The dimensions W and L of the FinFETs were chosen as 80nm and 32nm, respectively. The integrator receives a sinusoidal input signal with a frequency of 3.33kHz and a peak voltage of 50mV. As expected, the output displays a cosine waveform. The analysis of Total Harmonic Distortion (THD) was derived from the 20ms transient response of the integrator. The performance characteristics of SC integrators designed with two different Op-Amp configurations are provided in Table 4. The operating waveforms of the SC integrator designed with C=1 and M=1 Op-Amp are shown in Figure 14.

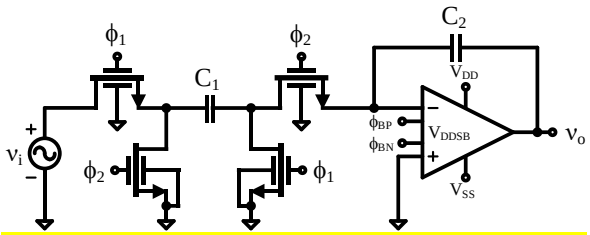


Figure 12: Configuration of the insenstive SC integrator utilizing FinFETs.

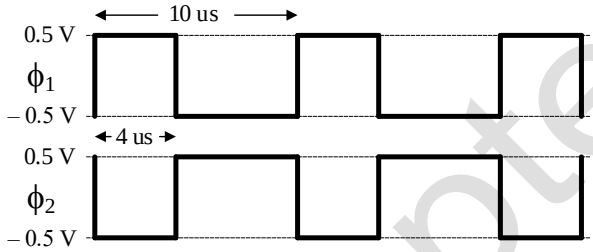


Figure 13: Operation waveforms of the switched capacitor clocks.

Table 4: Performance Comparison of SC Integrators.

| Performance parameters | Unit | This Work(1) | This Work(2) |
|---|---|---|---|
| Power Supply Voltages | V | ±0.5 | ±0.5 |
| Switching Frequency | kHz | 10 | 10 |
| Input Signal Amplitude | mV | 50 | 50 |
| THD (*fin*=3.33 kHz) | N/A | 0.336% | 0.251% |

(1): C=1, M=1, (2): C=5, M=5

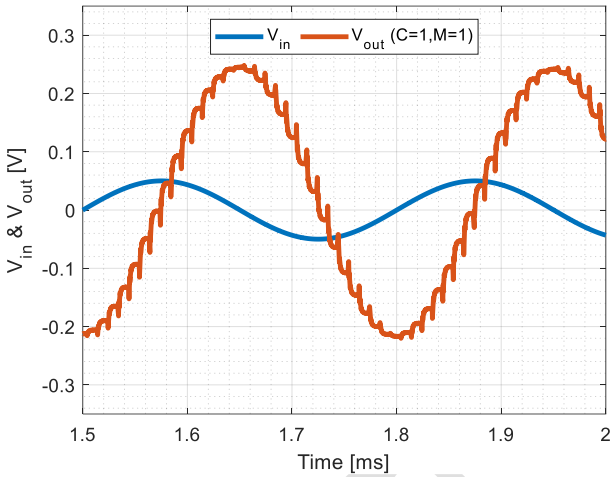


Figure 14: Input and output waveforms of the SC integrator (@C=1, M=1).

## 4 Conclusions

In this paper, a design of Complementary Folded-Cascode Op-Amp is presented using PTM 32nm FinFET technology. The circuit's stability at low voltages is achieved through the integration of DDSB and wide-swing cascode current mirror topologies. The dimensions of the circuit, parameterized by M and C, can be scaled down to nanoscale dimensions (C=1, M=1) according to application requirements, reducing power consumption to as low as 83µW. In this scenario, it can provide a DC gain of 37.42dB and a bandwidth of 8.46MHz. When C=5, M=5 the circuit simulations demonstrate a superior performance in terms of FoM1. In this case, with its provided 44.8dB voltage gain, 42.1kHz bandwidth, and 246µW power dissipation, it is highly suitable for low-power wide-band signal processing applications.

## 5 Conflict of Interest

The authors declare no conflict of interest

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