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A Low-Power and Low-Noise 4-12 GHz Buck CMOS Low-Noise Amplifier with Current-Reused Technique

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Abstract: In this paper, a wideband fully integrated low-power and low-noise amplifier (LNA) is presented. It features an 8 GHz (from 4 GHz to 12 GHz) bandwidth and an excellent noise figure (NF) using 65 nm CMOS technology. This LNA was designed utilizing a current-reused technique and a cascode gain boost technique. In addition, the interstage inductors use series peaking to reduce the roll-off of high frequency gain and achieve high broadband gain. The proposed LNA circuit achieved high and flat power gain of 23.5±1 dB with input return loss less than -8 dB within the bandwidth of interest (4-12 GHz). The flat NF is 3.3±0.5 dB and the NF_{min} is a staggering 2.8 dB. Achieving the above performance, the third-order input point (IIP3) also reached -10.78 dBm, which is considered excellent. The LNA consumes 6.07 mW from a 1.2 V supply and occupies a layout area of 0.53x0.55 mm^2.

Keywords: low-noise amplifier (LNA); noise figure (NF); Current-reused; CMOS

Ojačevalnik 4-12 GHz CMOS z nizko porabo energije in nizkim šumom s tehniko ponovne uporabe toka

Izvleček: V članku je predstavljen širokopasovni popolnoma integriran ojačevalnik (LNA) z nizko porabo energije in nizkim šumom. Ima 8 GHz (od 4 GHz do 12 GHz) pasovno širino in odlično šumno število (NF) z uporabo 65 nm tehnologije CMOS. LNA ojačevalnik je bil zasnovan z uporabo tehnike ponovne uporabe toka in tehnike kaskodnega povečanja ojačitve. Medstopenjske dušilke uporabljajo zaporedno ojačitev za zmanjšanje visokofrekvenčnega ojačenja in doseganje visokega širokopasovnega ojačenja. Predlagano vezje LNA je doseglo visoko ojačenje 23,5±1 dB z vhodno povratno izgubo, manjšo od -8 dB, znotraj pasovne širine (4-12 GHz). Ravna NF je 3,3±0,5 dB, NF_{min} pa je 2,8 dB. Pri doseganju zgornje zmogljivosti je vhodna točka tretjega reda (IIP3) prav tako dosegla -10,78 dBm. LNA porabi 6,07 mW pri napajanju z napetostjo 1,2 V in zavzema površino 0,53 × 0,55 mm^2.

Ključne besede: ojačevalnik z nizkim šumom (LNA); Vrednost šuma (NF); Ponovna uporaba toka: CMOS

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1 Introduction

With the rapid development of wireless communication, integrated wireless communication chip is widely used in the whole Ball positioning system, Internet of things, smart home, sensor and other industries, has been widely used and has penetrated into thousands of households and brought great and profound changes to the way of human work and life The development of integrated circuits [1-2]. Therefore, the LNA in UWB system has become a research hotspot. Because the performance of the first stage in the only communication system LNA amplifier directly affects the performance of the communication system, high gain and low noise figure become very important. In recent years, CMOS has become the mainstream of RF integrated circuit

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design. Its main advantages are low cost and easy integration [3-5].

As defined by the Federal Communications Commission (FCC), the frequency range 4-12 GHz is considered as UWB applications [6]. The low noise amplifier (LNA) is the first stage of the receiver system, and its performance affects the entire receiver system. Since it receives weak signals from the entire bandwidth range (4–12 GHz) and provides an adequate signal-to-noise ratio for subsequent signal processing, the LNA performance is crucial. If the noise is too large, the signal will be 'submerged' by the noise, thus affecting the performance of the entire receiving system. Therefore, it is critical for the LNA to have a low noise factor (NF), a high and flat power gain, and good input impedance matching performance. Several techniques have recently been proposed for research design of UWB LNA [6-8]. Additionally, with the wide application of UWB, a large number of excellent papers have been reported [9-10]. One of them is in [9], A two-stage LNA based on 90 *nm* CMOS is reported, with the first stage being a current reuse stage and the second stage being a cascode stage. Although a relatively low power consumption of 7.2 *mW* and a flat gain of 12.5 *dB* are achieved, NF 5.2 *dB* and low gain are still unsatisfactory. In [10], this paper reports a single-stage cascode topology fabricated in 0.13 *um* CMOS. Although the gain is relatively flat, it is too low to be acceptable for processing weak signals. What is more unsatisfactory is that only 4.25±0.4 *dB* NF is achieved with 30 *mW* power consumption.

In the process of analog integrated circuit design, designers need to follow the octagon principle of circuit design, and need to make a compromise between noise and gain, power consumption and matching, which requires constant debugging to achieve optimal performance. In order to compensate for the shortcomings of previous reports, this paper uses a two-stage topology. The first stage uses a Complementary common source stage and uses negative feedback to reduce gain sensitivity, the second stage uses a cascode stage to compensate for the lack of gain, and uses an inducer parallel peaking between stages to make up for the roll off of high-frequency gain. At the same time, the current multiplexing technology is used to effectively utilize the current to achieve low power design of the LNA, and all MOS are operating in the saturation region to achieve excellent performance.

The paper is structured as follows. The section 2 mainly focuses on circuit signal analysis including but not only input impedance and gain analysis. How do conventional structured small-signal analysis and matching devices affect input matching and noise figure. Section 3 introduces the proposed wideband LNA and the design process and current-reused technique. Section 4 is mainly devoted to the simulation results of the key indicators of LNA under different process voltage temperature (PVT). Finally, Section 5 draws the conclusions.

2 Circuit basic principle analysis

In the circuit design process, the designer may use the traditional common source stage as the first stage of the LNA. This is because the input matching and noise matching can be achieved by adding peripheral devices. Figure. 1(a) and Figure. 1(b) respectively are the traditional common source stage schematic diagram and small signal equivalent circuit whose gain expression is as follows:

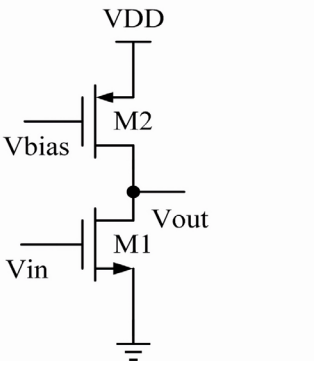

Figure 1(a): Common source stage circuit diagram.

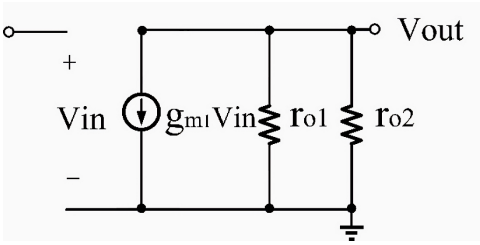

Figure 1(b): Common source stage small signal equivalent circuit.

$$A_V = -g_{m1}(r_{o1} \parallel r_{o2}) \tag{1}$$

Where gm_1 is the transconductance of the input transistor M_1, r_{o1} and r_{o2} are the small-signal equivalent resistances of the input transistor (M_1) and the current source transistor (M_2), respectively. From the gain expression, it can be seen that the traditional common source stage can improve the gain by increasing the small signal resistance, which is related to the current. Therefore, the small current can achieve high gain but will bring large noise, which is not consistent with the characteristics of LNA itself. Figure. 2(a) illustrates the noise equivalent circuit for noise analysis. The noise equivalent to the input is given by Expression (2) as follows:

$$\overline{V_{n,in}^2} = 4kT\gamma\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2}\right) \quad (2)$$

Figure 2(a): Common source stage noise equivalent circuit.

Here k is Boltzmann's constant, T is the temperature and is the noise factor of the MOSFET. By observing Expression 2, it is not difficult to find that only the transconductance of gm_1 is small to achieve relatively low noise, The expression for g is given by (3) as follows:

$$g_m = \sqrt{2I\mu c_{ox}\frac{W}{L}\left(V_{gs} - V_{th}\right)} \quad (3)$$

Through expression (3), it can be proved that g_m will become smaller when the current decreases, and through expression (2), it is not difficult to find that the noise will become larger, which means that too small current will bring relatively large noise. Here μ and C_{ox} are the mobility and gate oxide capacitance of the MOSFET, V_{gs} and V_{th} are the gate-source voltage and threshold voltage of the MOSFET and $\frac{W}{L}$ is the aspect ratio usually determined by the designer.

The first stage of this paper adopts the complementary common source stage and the following is the principle analysis. Figure. 2(b) shows the first level circuit schematic diagram and Figure. 3(a) is the calculation of its input equivalent circuit used as the input impedance.

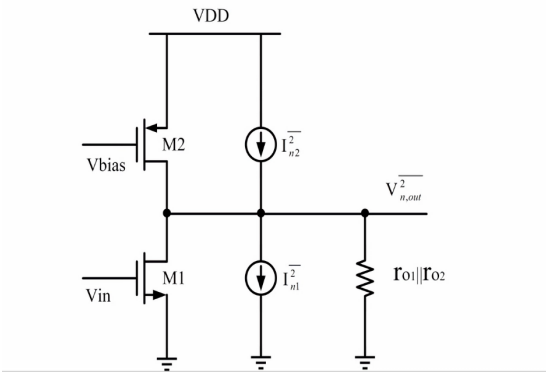

Figure 2(b): The first level of a circuit schematic.

The proposed of the LNA input impedance of the small-signal equivalent circuit according to Figure. 3(a) can be proved by Expression 3 as follows:

$$Z_{in} = \frac{s^2R_1C_{gs1}L_1 + R_1 + s^2C_1}{s^3R_1C_{gs2}C_{gs1}L_1 + s^2L_1C_{gs1} + sR_1\left(C_{gs1} + C_{gs2}\right) + 1} \quad (4)$$

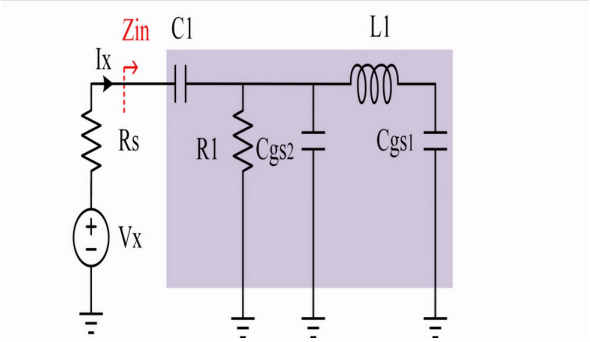

Figure 3(a): Input equivalent circuit of the LNA first stage.

Here are all the equivalent resistances seen by the node in Figure. 3(a), C_{gs1} and C_{gs2} are the MOSEFET gate-source parasitic capacitors of M_1 and M_2, respectively. Figure. 3(b) is the equivalent circuit of the first stage to analyze the gain of the first stage circuit, whose gain can be given by the following expression (5) by calculation.

$$A_{v1} = \frac{V_{out}}{V_{in}} = \frac{1 - g_mR_1 + s^2L_1\left(1 - g_{m1}R_1\right)}{\left(1 + s^2L_1\right)\left(1 + sR_1\right)} \quad (5)$$

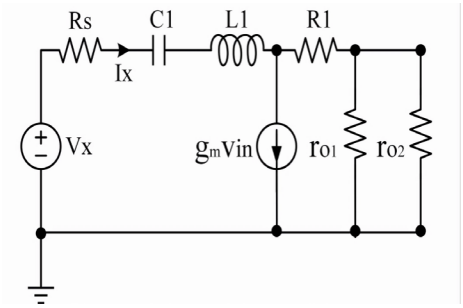

Figure 3(b): The first-stage small-signal equivalent circuit is used for gain analysis.

In order to maximize the transmission power of the receiving antenna, the LNA needs to design 50-ohm impedance matching. Figure. 4(a) shows the process of impedance matching. The matching process can be clearly seen from the Smith circle diagram. When the capacitor C_1 is added, the radius of the impedance circle is continuously reduced, as shown by the blue arrow in Figure. 4(a). When the inductor L_1 is added, the impedance curve is close to the center of the 50-ohm point circle, as shown by the green curve in the figure. The final circuit input impedance matching is shown by the red curve in the figure, achieving a good input matching.

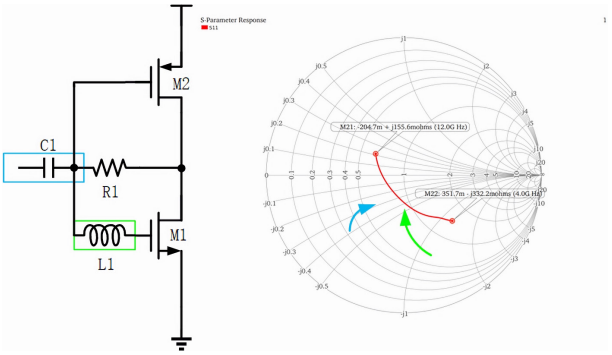

Figure 4(a): Smith Chart of impedance matching process.

3 Circuit design

With the continuous development of 5G millimeter-wave technology, the working frequency band is becoming higher, and the process requirements are also increasing. This demands MOSFETs with a higher cutoff frequency (f_t), faster speeds, and greater carrier mobility. After comprehensive consideration, this paper uses 65 *nm* CMOS technology to design a two-stage LNA applied to ultra-wide system, as shown in Figure. 4(b). The first stage uses a complementary common source stage which has a higher gain than the traditional common source stage. Because the first stage uses a feedback resistor to reduce the gain sensitivity, at the same time, it matched the noise with L1 to reduce the noise of the first stage, the second stage still uses a high gain cascode stage to improve the gain. The cascode stage not only has high gain but also has excellent input-output isolation characteristics which improve the isolation performance of the circuit. In essence, excellent isolation is achieved by negative feedback. When the output of M_4 fluctuates, it will also produce the same fluctuation at its source, which will cause the gate-source voltage of M_4 to change. Where to control the drain current. Therefore, the designed LNA achieves high gain and high linearity without passing through. Current reuse is reflected in the fact that the DC current flowing through M_4 and M_2 is multiplexed by M_1 and M_3 respectively so that no additional drive current is required to achieve lower power consumption.

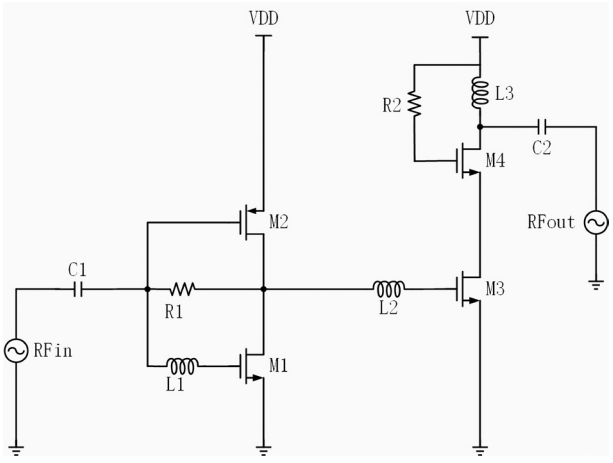

Figure 4(b): The Schematic of the proposed UWB LNA.

The wideband matching is not only reflected in the input impedance matching, but also in the frequency band of interest to avoid the attenuation of gain. In this paper, an inductor L_2 is added between the two stages. Using series inductive peaking can prevent the bandwidth degradation caused by the parasitic capacitor C_{gs3}, which is brought about by the large transistor M_3. By selecting a suitable inductance value for L_2 and resonating with the parasitic capacitance of the M_3 transistor, the high-frequency gain can be improved, and the bandwidth can be expanded. At the same time, the noise matching with the second stage can be realized to ensure the low noise characteristics of the LNA. Figure. 5 (a) shows that the LNA designed in this paper simultaneously achieves high and flat power gain and excellent noise characteristics within the frequency band of interest. In order to verify the effect of interstage inductance L_2, Figure 5(b) shows the results with and without series inductive peaking. It can be seen from Figure 5(b) that, with the series inductive peaking, the gain at the higher frequency increases from 12.4 *dB* to 23 *dB*, and the overall increase is nearly 11 *dB*. When there is no interstage inductance L_2, the gain will be greatly reduced in the high frequency part, which is the result we do not want to see. Therefore, the final choice of L_2 is equal to 2 *nH*. The former inductor L_3 and capacitor C_2 are designed to resonate with the parasitic capacitance of the leakage end of M_4 to achieve output matching, while the latter is a direct isolating capacitor to avoid the current of V_{DD} flowing to the output end of the amplifier.

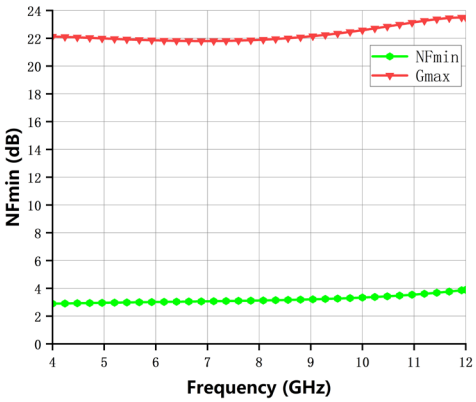

Figure 5(a): Verification of high and flat maximum gain and excellent noise characteristics in the frequency band of Interest.

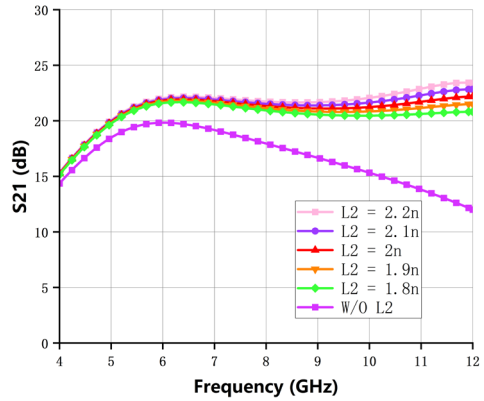

Figure 5(b): Comparison of simulation results of with or without inducer.

4 Performance summary

The proposed UWB LNA design has been implemented in 65 *nm* CMOS process, verified in Cadence Virtuoso platform, post-layout simulation of parasitic parameters extracted by Cadence Calibre, and imitation of netlist after import in Cadence Virtuoso, Figure. 6(a) shows the layout of the proposed LNA.

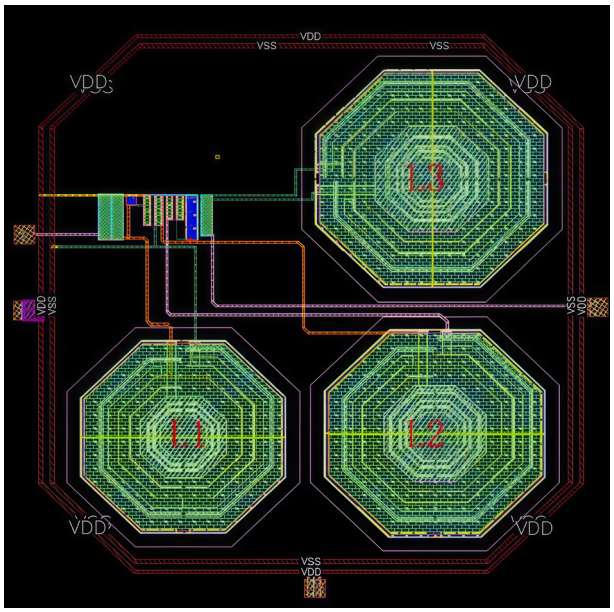

Figure 6(a): Layout of the proposed LNA

Figure. 6(b) shows the simulation results of the reflection coefficient of input return loss under different temperatures, different voltages and different process angles (PVT). The reflection coefficient of ff process Angle is the smallest and S11 is less than -10 *dB* in almost the whole frequency band. The minimum value of S11 is about -12 *dB*. Meet the impedance matching requirements. The simulation results of the UWB LNA under PVT conditions are illustrated in Figure. 7(a). The peak gain of 27 *dB* demonstrates exceptional performance compared to other published papers [11-16], while maintaining excellent S21 gain flatness across the entire UWB range with a minimal fluctuation range of only 1 *dB*. This characteristic enables effective amplification of in-band RF signals. Furthermore, even under the worst process angle (ss), it achieves a high gain ranging from 14-20 *dB*.

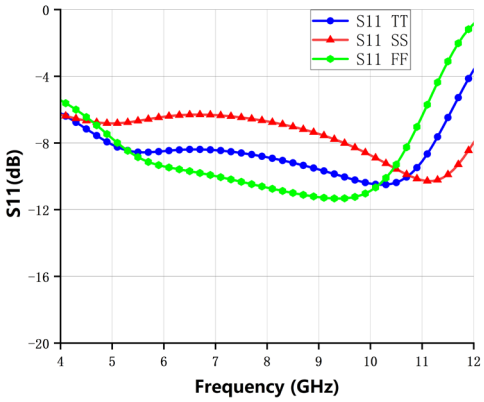

Figure 6(b): Simulated S_{11}.

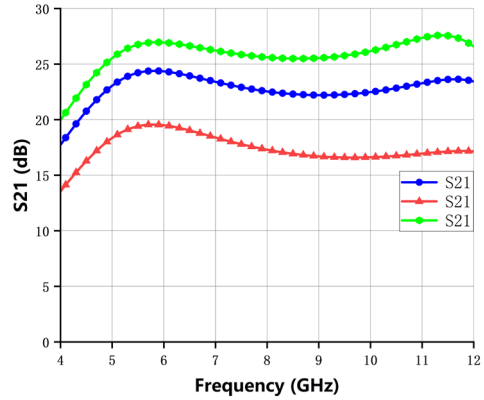

Figure 7(a): Simulated S_{21}.

The simulation curve of input-output isolation under PVT is depicted in Figure. 7(b). The reverse isolation exhibits a gradual increase across the entire frequency range, yet remains below -20 *dB*. within the UWB band. Notably, the reverse isolation index remains consistent across all three corners, indicating excellent performance of the UWB LN. Figure. 8(a) shows the noise characteristics of the proposed LNA. In the communication system, the LNA needs to deal with the energy from the antenna, so the output signal of the LNA is required to have a high enough signal-to-noise ratio NF to measure its performance. The proposed LNA exhibits an amazing 2 *dB* NF and achieves lower than 4 *dB*. NF over the entire frequency band even in the worst case, which is a very excellent result. The simulation results in Figure. 8(b) depict the third-order intermodulation

curve, which serves as an indicator of the linearity of UWB. Distortion arises from poor linearity in the output signal of an LNA, consequently leading to subpar performance of the entire communication system. In comparison with other research papers, this paper LNA exhibits exceptional linearity at approximately -10.78 *dBm* [17-19].

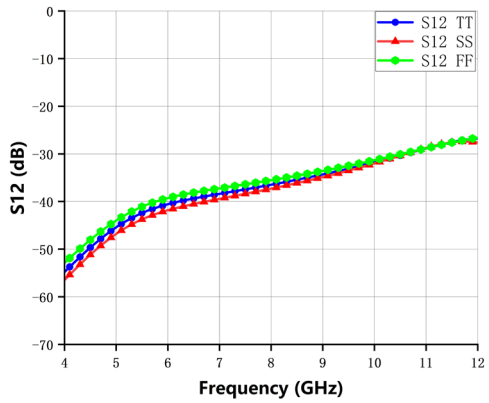

Figure 7(b): Simulated S_{21}.

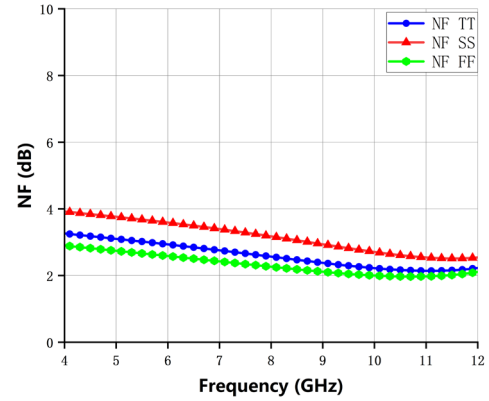

Figure 8(a): Simulated NF.

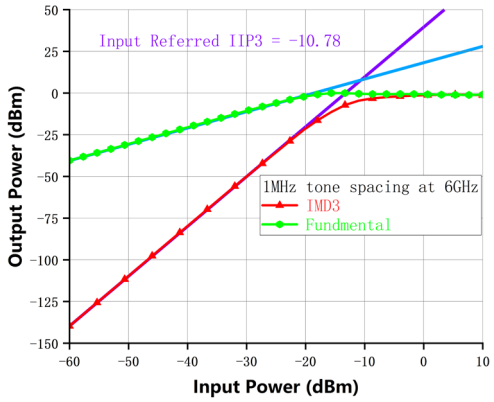

Figure 8(b): IIP3 of the proposed LNA

Figure. 9（a）shows the simulation results of the mismatch of NF. In the case of running 200 points, the mismatch of NF is very small and can almost be ignored. One value is 61 *m* and values are only 180 *m*, reflecting that the random mismatch of the device has very little influence on the LNA NF. The simulation results of S11 in Figure. 9(b) demonstrate a small mismatch ratio when running 200 points, primarily distributed around -8 *dB*. The value of one is 470 *m*, and the value of mismatch 1.4, indicating that the random device mismatch has a relatively negligible impact on the S11 performance of LNA. Its deviation remains within an acceptable range without affecting the overall UWB performance. Figure. 10(a) shows the simulated mismatch results for S21 gain. In the case of running 200 points, the mismatch of S12 is relatively small, with a value of 1, as the mismatch mainly concentrates on the gain greater than 23 *dB*. Even if there is a little mismatch, it is only a few points that have a minimal impact on the performance of the LNA. The minimum gain of the mismatched LNA is also greater than 20 *dB*, indicating that the LNA has excellent performance.

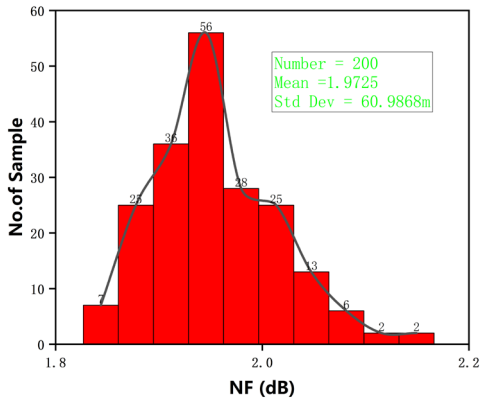

Figure 9(a): Monte Carlo results of NF

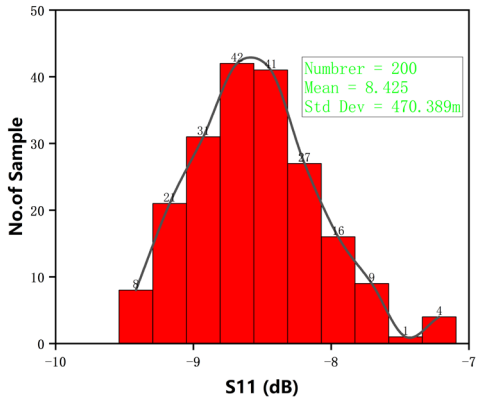

Figure 9(b): Monte Carlo results of S_{11}

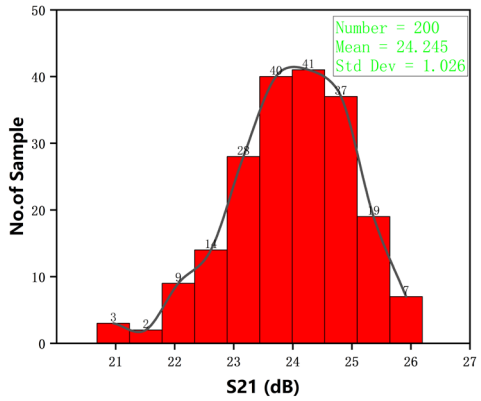

Figure 10(a): Monte Carlo results of S_{21}.

5 Conclusion

This article comprehensively describes the detailed analysis and design ideas of an LNA that adopts a two-stage structure implemented on 65 *nm* CMOS technology. The proposed two-stage LNA uses inter-stage matching to achieve broadband matching and high gain. Most importantly, noise matching is achieved to obtain a low NF, and at the same time, the current-reused technology is used to effectively reduce power consumption. Finally, the Monte Carlo and process-corner simulations confirm that the proposed design is suitable for the UWB system. The proposed LNA achieves a peak gain of 24.7 *dB*, with its 3- *dB* bandwidth ranging from 5 to 12 GHz and an NF of 2.8 *dB* at 11 GHz, while consuming 6.07 *mW* of DC power. The core area of the LNA is optimized to only 0.292 mm^2.

6 Conflict of interest

The authors declared no potential conflict of interest with respect to the research, authorship, and publication of this article.

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Table 1: Summarized performance and comparison with The-Starte-Of-The-Art.

Ref	Tech (nm)	Freq (GHz)	BW (GHz)	S_{21} (dB)	NF (dB)	Power (mW)	IIP3 (dBm)	Area (mm^2)
[3]	65	3.1-5	NA	13.8-14.6	5.4-6	1.49	-10.5	NA
[5]	130	3-12.3	NA	12-15	4-4.6	8.5	-7	0.86
[14]	180	0.4-10	9.6	12.4	4.4-6.5	12	-6	0.42
[15]	65	26-30	NA	13.68	3.84	11.6	-7.15	0.17
[16]	65	15.8-30.3	14.5	10.2	3.3-5.5	12.4	NA	0.185
[17]	65	0.5-7	NA	16.8	2.87-3.77	11.3	-4.5	0.044
[19]	180	3-10	7	12.2-15.2	2.2-2.4	18	-0.2	0.39
This Work	65	4-12	7	22.5-24.8	2.8-3.8	6.07	-10.78	0.292

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