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Design of a New MISO Mixed-Mode Universal Biquad OTA-C Filter in 130nm CMOS Technology

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Abstract: This paper presents the design of a MISO (multiple-input single-output) universal biquad filter in 130 nm CMOS UMC technology. The proposed filter consists of three operational transconductance amplifiers (OTAs), two grounded capacitors and one inverter stage. The topology, which has three inputs and one output, operates in all modes: voltage, transconductance, current, and transresistance. In addition, the filter generates all types of transfer functions (LP, HP, BP, BS, and AP). First, the filter topology with an inverter at the output is designed and analyzed in detail. Next, an improved topology with a differential amplifier as the output stage is proposed. The designed filter has a cutoff frequency of approximately 250 MHz and a current consumption of 4.5 mA. The impact of process, temperature, and voltage variations is examined through corner analysis.

Keywords: universal biquad filter, operational transconductance amplifier, OTA-C filter, analog IC design

Oblikovanje novega MISO univerzalnega biquad OTA-C filtra z mešanim načinom v 130 nm tehnologiji CMOS

Izvleček: V tem članku je predstavljena zasnova univerzalnega biquad filtra MISO (multiple-input single-output) v 130 nm tehnologiji CMOS UMC. Predlagani filter je sestavljen iz treh operacijskih transkonduktančnih ojačevalnikov (OTA), dveh ozemljenih kondenzatorjev in ene inverterske stopnje. Topologija, ki ima tri vhode in en izhod, deluje v vseh načinih: napetostnem, transkonduktančnem, tokovnem in tranzistorskem. Poleg tega filter ustvarja vse vrste prenosnih funkcij (LP, HP, BP, BS in AP). Najprej je zasnovana in podrobno analizirana topologija filtra z inverterjem na izhodu. Nato je predlagana izboljšana topologija z diferencialnim ojačevalnikom kot izhodno stopnjo. Zasnovani filter ima mejno frekvenco približno 250 MHz in porabo toka 4,5 mA. Vpliv procesnih, temperaturnih in napetostnih sprememb je preučen z analizo vogalov.

Ključne besede: univerzalni biquad filter, operacijski transkonduktančni ojačevalnik, filter OTA-C, MISO, zasnova analognih integriranih vezij

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1 Introduction

Analog active filters are essential building blocks for various analog signal processing systems. The design of second-order or biquad universal filters, which provide all five filtering responses, low-pass (LP), band-pass (BP), high-pass (HP), all-pass (AP), and band-stop (BS), has been shown to be appealing in recent years. OTA-C or OTA-Gm universal filters are advanced analog filters capable of achieving versatile filtering functions [1]. They are highly valued for their ability to realize multiple filter responses within a single circuit configuration [2]. OTA-C filters offer several advantages, including low power consumption, wide frequency range operation, and the ability to operate in various signal modes (voltage, current, transresistance, and transconductance) [2]. They are particularly useful in applications requiring compact, efficient, and reconfigurable filtering solutions, such as biomedical devices, communication systems, and sig-

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nal processing circuits [2]. The design of OTA-C universal filters involves optimizing various parameters, such as sensitivity, frequency performance, parasitic effects, dynamic range, noise, low-voltage operation, power consumption, and chip area [1]. By carefully selecting the constituent devices and filter structure, OTA-C filters can achieve high performance and reliability in integrated circuit applications [1].

There are several types of universal OTA-C filters. One notable example is the single-input multiple-output (SIMO) universal OTA-C filter. These filters can manage multiple outputs from a single input signal, using OTAs and capacitors to perform various filtering functions [3]. Paper [3] introduces a universal SIMO filter composed of eight OTAs and two grounded capacitors. This filter has five outputs, enabling the realization of different filter functions in voltage mode. It achieves a center frequency of 2.89 MHz and a quality factor of 1.

Paper [4] presents a universal multiple-input multiple-output (MIMO) filter. The circuit consists of eight single-ended OTAs and two grounded capacitors. It can operate as a two-input and four-output filter or a three-input and single-output filter. The quality factor can be adjusted using capacitors, while the center frequency can be controlled with the OTA's transconductance without disturbing the quality factor. The filter achieves a center frequency of 2.89 MHz and a quality factor of 1.

Paper [5] introduces a multiple-input, single-output (MISO) universal OTA-C filter. This filter contains six OTAs and two grounded capacitors. It operates in voltage mode with four inputs and one output. The quality factor can be adjusted without affecting the center frequency.

Paper [6] presents a universal active MISO filter employing three OPAs, two capacitors, and seven resistors. This filter is capable of realizing three filter functions: BP, LP, and HP. It features one input and four outputs. The inclusion of resistors contributes to a more complex design compared to OTA-C filters. In contrast, filters [3]-[5] offer additional functionalities, including BS and AP functions, demonstrating their superior versatility.
Two additional topologies are presented in [7]. Both topologies operate in mixed-mode regimes (voltage, current, transconductance and transresistance mode) and can realize all filter functions from a single topology. The first proposed circuit consists of four OTAs and two grounded capacitors, while the second topology contains five OTAs and two grounded capacitors. The center frequency is 1.59 MHz.

Paper [8] introduces a mixed-mode universal MISO OTA-C filter. The circuit consists of six single-output and one dual-output OTA in combination with two grounded capacitors. This filter can realize all filter functions and can be driven with voltage or currents. It offers the ability to adjust the center frequency and quality factor independently. Two working modes (current and voltage) are presented.

Paper [9] presents a voltage-mode MISO OTA-C filter. This filter uses five single-output OTAs and two grounded capacitors and can realize all filter functions. The MIMO filter described in paper [10] consists of four OTAs, two grounded capacitors, and one resistor.

This paper builds upon a universal MISO biquadratic filter presented in [11] that operates in all four modes and realizes all five filter functions. This topology employs a minimal number of active and passive components to realize a mixed-mode universal biquad OTA-C filter, resulting in reduced area and power dissipation. The main issue in this approach is the high sensitivity of the output inverter stage to process, voltage, and temperature (PVT) variations, which causes changes in the inverter characteristics and the DC output voltage. This can be seen as significant fluctuation of the filter response in the current and transconductance modes. This paper addresses this challenge comprehensively and proposes a new topology using a simple OTA instead of the inverter. The circuit uses only three additional transistors while significantly reducing sensitivity to PVT variations. In addition, the filter center frequency has been considerably increased compared with the results presented in [11].

The rest of the paper is organized as follows: Section 2 describes in detail the proposed filter topology, its building blocks, and enhancements. The post-layout simulation results, including the corner analysis, are presented in Section 3. Section 4 provides a summary of the paper's main conclusions.

2 Proposed filter topology

The initial MISO multi-mode universal biquad OTA-C filter topology, with the minimum number of active and passive components [11], is shown in Figure 1. The filter comprises four amplifier stages and two grounded capacitors; the first stage is an OTA with two inputs, the second and third stages are OTAs with four inputs, and the final stage is an inverter (used as a transconductance amplifier).

This filter has one output and three inputs: V_1, V_2, and V_3 in voltage and transconductance mode and I_1, I_2, and I_3 in the current and transresistance mode. V_{out} repre-

sents the voltage and transresistance mode output, while I_{out} represents the current and transconductance mode output. The inverter is essential for the current and transconductance modes.

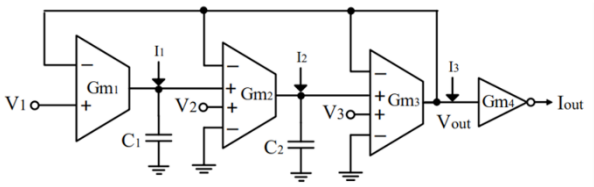

Figure 1: The filter topology proposed in [11]

The first filter stage consists of differential OTA, as shown in Fig. 2 [12]. The second and third stages are OTAs with four inputs (two pairs of differential input), Fig. 3 [11]. The initial filter uses a standard CMOS inverter circuit, Fig. 4.

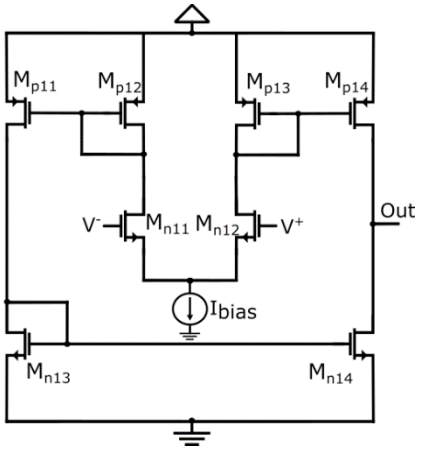

Figure 2: The first filter stage – differential OTA [11]

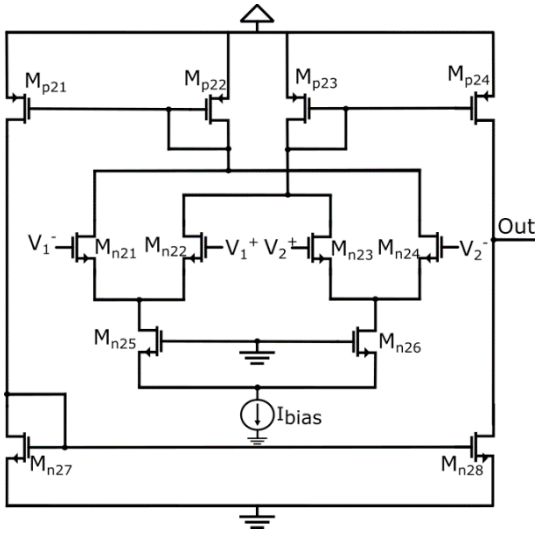

Figure 3: The second and third filter stage – OTA with four inputs [11]

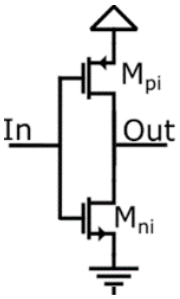

Figure 4: The filter output stage: inverter [11]

The filter transfer function in the voltage mode is as presented in [11]

$$V_{out} = \frac{Gm_1Gm_2(V_1)}{D(s)} + \frac{SC_1Gm_2(V_2)}{D(s)} + \frac{S^2C_1C_2(V_3)}{D(s)} \quad (1)$$

The filter transfer function in the current mode is as described in [11]

$$I_{out} = -\left(\frac{Gm_2Gm_3Gm_4(I_1)}{D(s)} + \frac{SC_1Gm_3Gm_4(I_2)}{D(s)} + \frac{S^2C_1C_2(I_3)}{D(s)}\right). \quad (2)$$

The filter transfer function in the transresistance mode is as presented in [11]

$$V_{out} = \left(\frac{1}{Gm_3}\right)\left(\frac{Gm_2Gm_3(I_1)}{D(s)} + \frac{SC_1Gm_3(I_2)}{D(s)} + \frac{S^2C_1C_2(I_3)}{D(s)}\right). \quad (3)$$

The filter transfer function in the transconductance mode is as defined in [11]

$$I_{OUT} = -\left(\frac{Gm_1Gm_2Gm_4(V_1)}{D(s)} + \frac{SC_1Gm_2Gm_4(V_2)}{D(s)} + \frac{S^2C_1C_2Gm_4(V_3)}{D(s)}\right). \quad (4)$$

The polynomial in the denominator is represented by

$$D(s) = S^2C_1C_2 + SC_1Gm_2 + Gm_1Gm_2. \quad (5)$$

The quality factor is given by [11]

$$Q = \sqrt{\frac{C_2Gm_1}{C_1Gm_2}}. \quad (6)$$

The center frequency is described by [11]

$$\omega_0 = \sqrt{\frac{Gm_1Gm_2}{C_1C_2}}. \quad (7)$$

By examining Equations (6) and (7), it can be observed that both the center frequency and the quality factor are determined by the same parameters (transconductances and capacitances). If the transconductances are of equal value ($G_{m1} = G_{m2} = G_m$), the center frequency can be ad-

justed by changing the transconductance values without affecting the quality factor (see Equations (8) and (9)).

$$Q = \sqrt{\frac{C_2}{C_1}} \tag{8}$$

$$\omega_0 = G_m \sqrt{\frac{1}{C_1 C_2}} \tag{9}$$

The filter realizes various transfer functions (LP, BP, HP, BS, and AP) in four different modes, as presented in Table 1. Additional details about the transfer functions and modes can be found in [11]. This filter topology faces challenges related to PVT variations in transconductance and current modes. Detailed analysis has shown significant fluctuations in the inverter output DC voltage during corner analyses, resulting in substantial gain variation. These changes considerably affect the filter characteristics in the current and transconductance modes. Therefore, this paper proposes a modified topology, as shown in Fig. 5. The final stage (G_{m4}) is replaced by a simple OTA circuit or a standard differential amplifier with a current source as the load, operating in unity feedback, Fig. 6. The complete biasing circuit, which provides the biasing (reference) currents for all filter stages, is shown in Fig 7. It is based on the self-biasing reference presented in [14] and includes additional current mirrors, consisting of transistors M_4–M_7, which generate the biasing currents, I_{bias1}, I_{bias2}, I_{bias3}, and I_{bias4}, for the filter stages. The proposed filter topology employs three more transistors than the initial circuit but substantially improves the sensitivity of the filter (see the post-layout simulation results in the following section).

Table 1: The filter frequency response in different modes [11]

Filter type	Mode					
(noninverting)	Voltage			Transresistance		
	V_1	V_2	V_3	I_1	I_2	I_3
LP	V_{in}	0	0	I_{in}	0	0
BP	0	V_{in}	0	0	I_{in}	0
HP	0	0	V_{in}	0	0	I_{in}
BS	V_{in}	0	V_{in}	I_{in}	0	I_{in}
AP	V_{in}	V_{in}	V_{in}	I_{in}	I_{in}	I_{in}
(inverting)	Current			Transconductance		
	I_1	I_2	I_3	V_1	V_2	V_3
LP	I_{in}	0	0	V_{in}	0	0
BP	0	I_{in}	0	0	V_{in}	0
HP	0	0	I_{in}	0	0	V_{in}
BS	I_{in}	0	I_{in}	V_{in}	0	V_{in}
AP	I_{in}	I_{in}	I_{in}	V_{in}	V_{in}	V_{in}

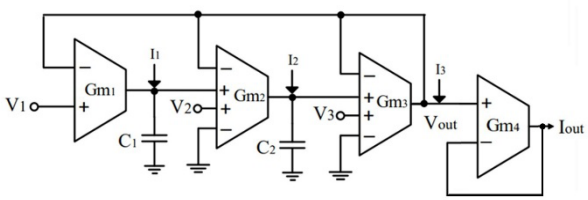

Figure 5: The proposed filter topology

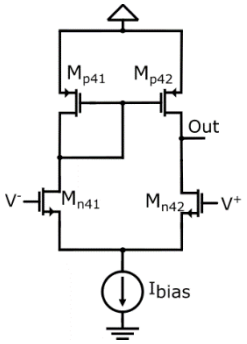

Figure 6: The proposed filter output stage (G_{m4}) – a differential amplifier with a current source as load [13]

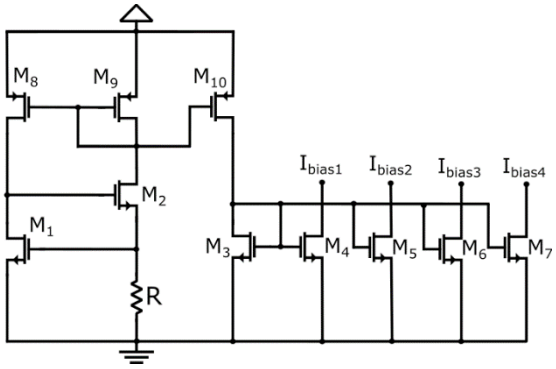

Figure 7: The proposed filter biasing circuit

3 Post-layout simulation results and discussion

The proposed filter topology is designed using the UMC 130 nm MM/RF CMOS process with Cadence Virtuoso Tools. The transistor gate widths are presented in Table 2. All filter stages are designed with the minimum gate length of 120 nm, while the devices in the current mirrors have gate length of 200 nm. The resistor value is 5.65 kΩ. The proposed circuit layout is shown in Fig. 8. The integrated filter occupies a die area of 230 µm x 130 µm.

To demonstrate the advantages of the proposed topology, this section presents the post-layout simulation results for both topologies, which have been simulated using the Spectre Simulator from Cadence Design Sys-

Table 2: The transistor gate widths

Transistor	Fingers	Number of devices	W [µm]
M_{p11}, M_{p14}	4.0	6.0	2.0
M_{p12} M_{p13}	4.0	2.0	2.0
M_{n11}, M_{n12}	4.0	4.0	3.5
M_{n13}, M_{n14}	4.0	1.0	0.9
M_{p21}, M_{p24}	4.0	8.0	2.0
M_{p22}, M_{p23}	4.0	2.0	2.0
M_{n21}, M_{n22} M_{n23}, M_{n24}	4.0	4.0	3.5
M_{n25}, M_{n26}	4.0	6.0	2.0
M_{n27}, M_{n28}	4.0	1.0	1.1
M_{p1}	4.0	1.0	4.0
M_{n1}	4.0	1.0	2.0
M_1, M_2	4.0	4.0	2.0
M_3	4.0	2.0	2.0
M_4	4.0	6.0	2.0
M_5, M_6	4.0	12.0	2.0
M_7	4.0	2.0	2.0
M_8, M_9, M_{10}	4.0	1.0	2.0

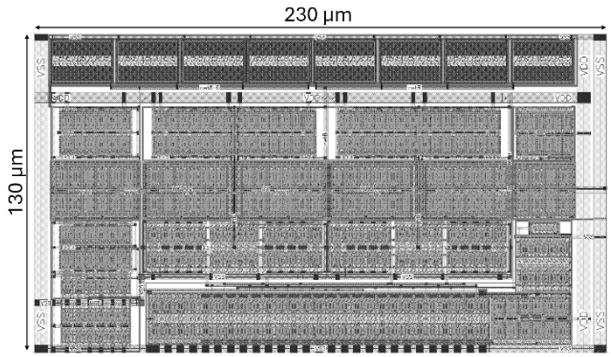

Figure 8: The proposed filter layout

tems. A corner analysis has been conducted for each topology to evaluate performance under various process, voltage, and temperature conditions. Only the most critical results have been presented for the initial topology, whereas a more detailed analysis has been provided for the proposed circuit. It should be emphasized that in this work, much higher center frequency values were achieved compared to the results obtained in [11]. Unfortunately, this was achieved at the expense of higher transconductance values and, consequently, increased overall circuit power consumption.

The transconductance values of the OTA circuits are $G_{m1} = G_{m2} \approx 4$ mS. The capacitance values are $C_1 = C_2 = 2.6$ pF. The symmetrical power supply of ±0.6 V is used. The center frequency at the nominal corner is 251 MHz with a quality factor of 1. The total current consumption of the proposed filter is 4.5 mA. The bias currents are $I_{bias1} = 150$ µA, $I_{bias2} = I_{bias3} = 300$ µA, and $I_{bias4} = 50$ µA.

Figures 9, 10, 11, and 12 demonstrate the post-layout simulation results for the initial filter topology (Fig. 1). In these figures, the initial topology is labeled as T1, while the proposed topology is denoted as T2 (in the following figures). Process variation corners including typical-typical (TT), fast-fast (FF), slow-slow (SS), slow-fast (SF) and fast-slow (FS) of NMOS and PMOS transistor parameters has been simulated. Process and voltage variations are presented for transconductance mode in Figs. 9 and 10, and for current mode in Figs. 11 and 12, respectively.

The nominal center frequency is 251 MHz. These results highlight the critical corners associated with the DC voltage shift at the inverter output and the gain changes due to voltage and process variations. The critical process variations are FS and SF corners.

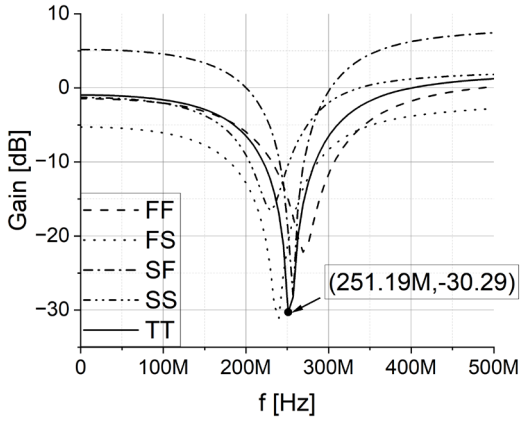

Figure 9: Post-layout simulations for process variations in transconductance mode (T1)

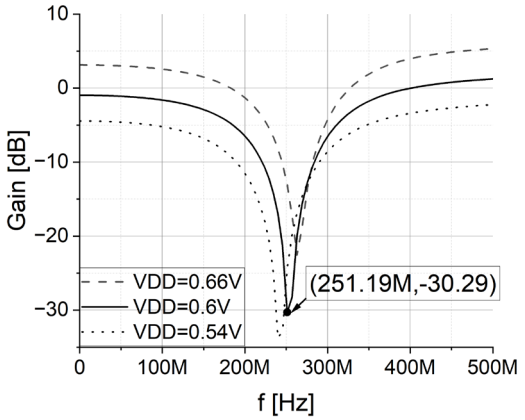

Figure 10: Post-layout simulations for voltage variations in transconductance mode (T1)

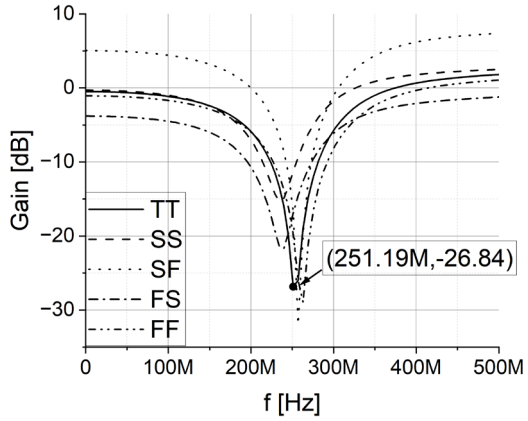

Figure 11: Post-layout simulations for process variations in current mode (T1)

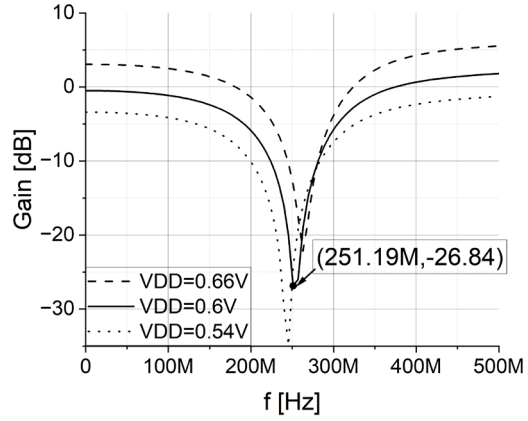

Figure 12: Post-layout simulations for voltage variations in current mode (T1)

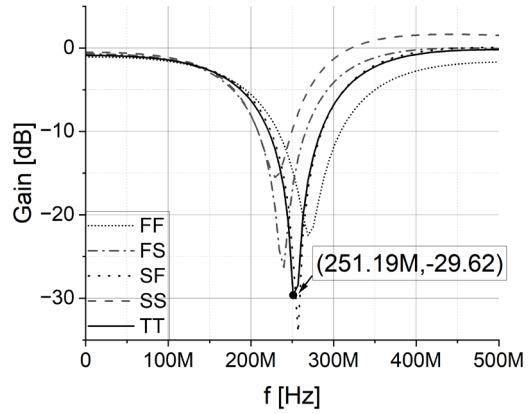

Figure 13: Post-layout simulations for process variations in transconductance mode (T2)

Figures 13, 14, 15, and 16 illustrate the post-layout simulation results for the proposed filter topology (Fig. 5). Process and voltage variations for the transconductance mode are shown in Figs. 13 and 14, while those for the current mode are displayed in Figs. 15 and 16, respectively. These results present critical corners for voltage and process variations in both sensitive modes,

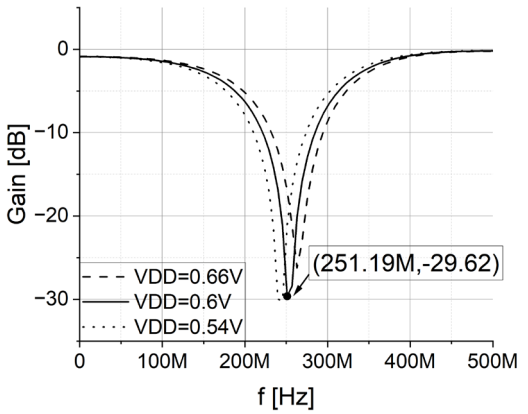

Figure 14: Post-layout simulations for voltage variations in transconductance mode (T2)

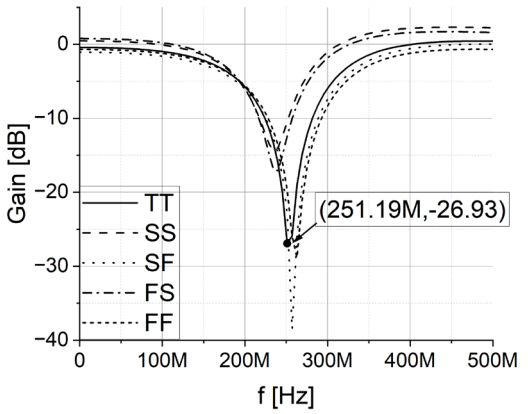

Figure 15: Post-layout simulation for process variations in current mode (T2)

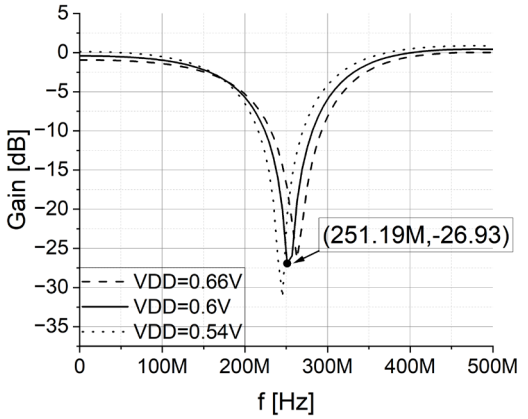

Figure 16: Post-layout simulation for voltage variations in current mode (T2)

demonstrating significant improvements in the proposed filter topology by eliminating gain variations. Additionally, it can be observed that the changes in the characteristics across all operating modes are smaller compared to those in the previous circuit.

Figures 17, 18, 19, and 20 present the post-layout simulation results for all transfer functions (LP, HP, BP, AP and BS) of the proposed MISO universal OTA-C filter while showcasing the nominal results for all modes

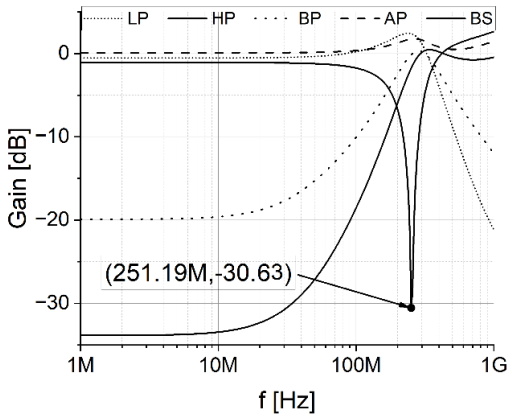

Figure 17: Post-layout simulation results for voltage mode (T2)

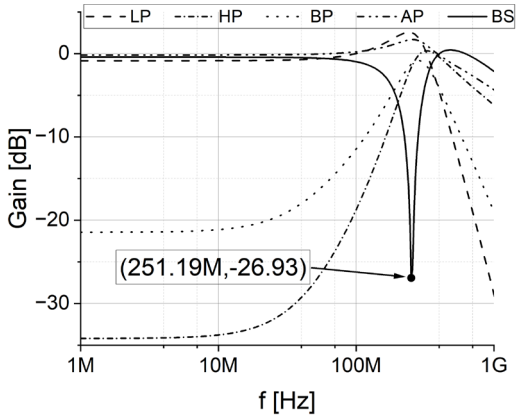

Figure 18: Post-layout simulation results for current mode (T2)

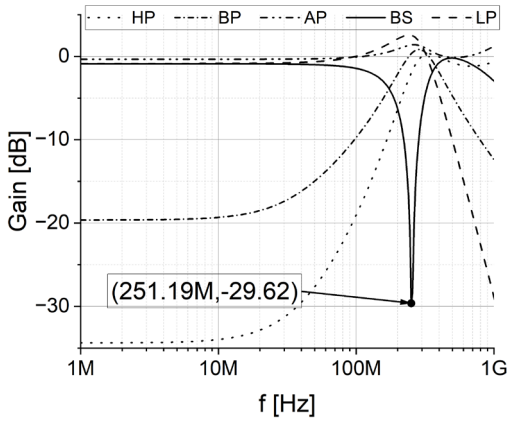

Figure 19: Post-layout simulation results for transconductance mode (T2)

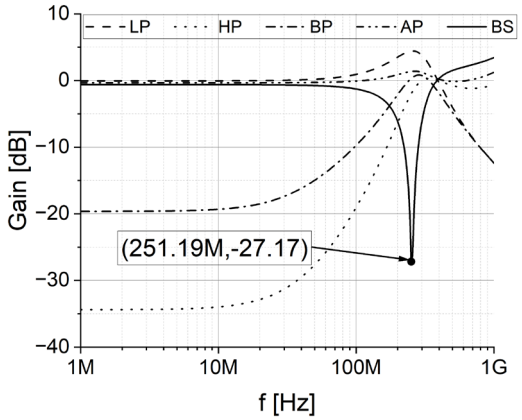

Figure 20: Post-layout simulation results for transresistance mode (T2)

(voltage, current, transresistance, and transconductance). It can be noted that the center (cutoff) frequency of all filter characteristics is approximately 251 MHz. Moreover, no significant attenuation is observed in the passband, and the attenuation in the stopband is acceptable.

To fully verify the filter sensitivity, additional analyses including process variations in MOSFET, bias resistor, and capacitor parameters have been simulated. Furthermore, the dependence of the filter key parameters (e.g. the center frequency and the attenuation at the center frequency) on voltage and temperature variations has been tested. To save space, the post-layout simulation results of the corner analyses have been presented only for the voltage mode. The nominal center frequency is 251.19 MHz, while the nominal attenuation at the center frequency is -30.63 dB.

Figure 21 illustrates the influence of the process variations of the MOSFET parameters. The minimum center frequency is 229.09 MHz in the SS corner, while the maximum center frequency reaches 269.15 MHz in the FF corner. The influence of the process variations of the resistor in biasing circuit is shown in Fig 22. The minimum center frequency is 234.42 MHz in the maximal corner, while the maximum center frequency reaches 281.84 MHz in the minimal corner. Figure 23 displays the process variations of the capacitor parameters. The minimum center frequency is 234.42 MHz in the maximal corner, while the maximum center frequency reaches 275.42 MHz in the minimal corner.

The influence of the voltage is simulated with a ±10% variation around the nominal voltage supply value, as shown in Fig. 24. The center frequency ranges from a minimum of 234.42 MHz to a maximum of 275.42 MHz. Figure 25 presents the filter characteristics under different temperature from -40° to 125°. The center fre-

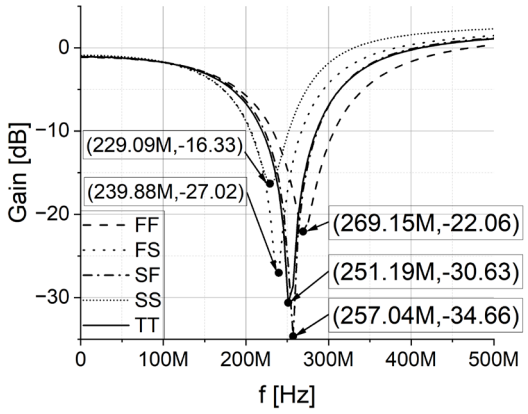

Figure 21: Post-layout simulation results for process variations of the MOSFET transistors (T2)

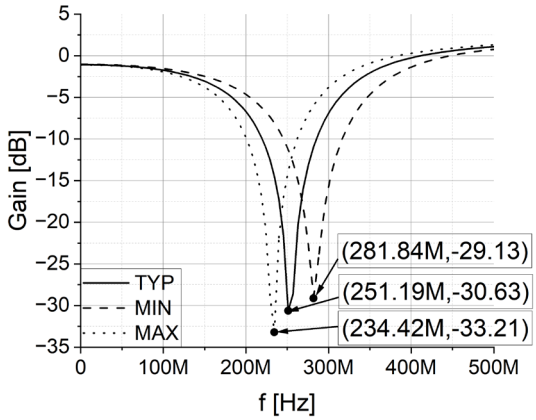

Figure 22: Post-layout simulation results for process variations of the resistor in the biasing circuit (T2)

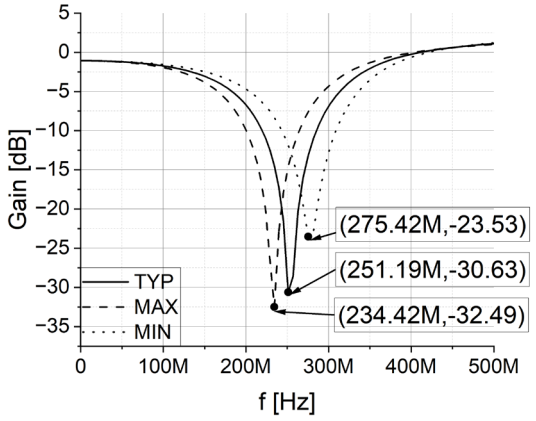

Figure 23: Post-layout simulation results for process variations of the capacitor in biasing circuit (T2)

quency ranges from a minimum of 204.17 MHz to a maximum of 269.15 MHz. In the worst case, when the temperature is 125°, the change in center frequency is less than 19%. As can be observed, the proposed filter is not highly sensitive to different corners.

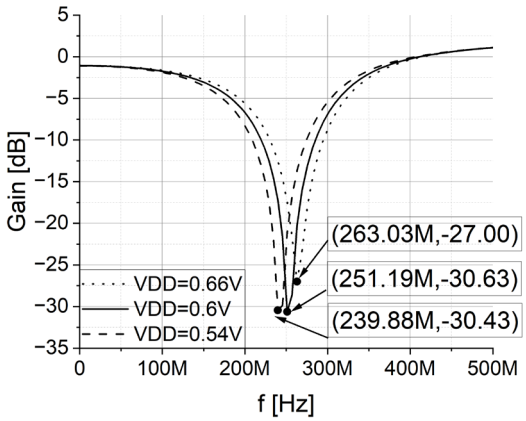

Figure 24: Post-layout simulation results for voltage variations (T2)

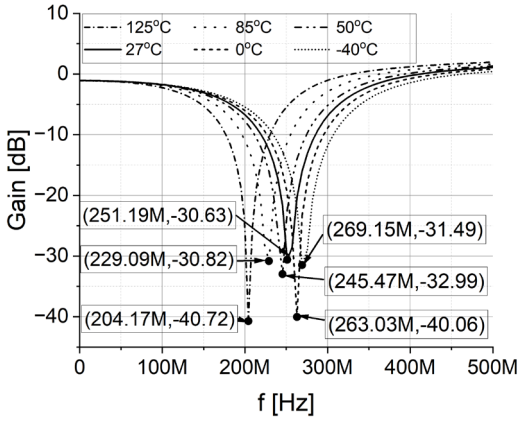

Figure 25: Post-layout simulation results for temperature variations (T2)

A summary of all corner analysis results for all filter operating modes is presented in Table 3. The performance (e.g. the center frequency (f_0 [MHz]) and the attenuation at the center frequency) are provided for the band-stop filter transfer function. Parameters α_N [dB], α_{TK} [dB], α_C [dB], and α_{TR} [dB] represent the attenuations at the center frequency in the voltage, transconductance, current, and transresistance mode, respectively. It can be observed that there are no significant changes in results across PVT variations.

Table 4 presents a comparison of the simulation results obtained in this paper and the reference research presented in [11]. As previously discussed, the filter topology proposed in [11] uses an inverting amplifier at the output (Fig. 1) to decrease the number of transistors and save die area. This study proposes the improved filter topology with the differential amplifier at the output (Figs. 5 and 6) to reduce the impact of process and voltage variations in transconductance and current operating modes (proved by the obtained simulation results). Moreover, this paper operates at a significantly higher frequency but with higher power consumption.

Table 3: Corner analysis results

Process variations of MOSFET					
	TT	SS	FS	SF	FF
f_0	251.2	229.1	239.9	257.0	269.0
α_N	-30.6	-16.3	-27.0	-51.8	-22.1
α_{TK}	29.6	-15.5	-26.3	-34.1	-22.5
α_C	-26.9	-14.8	-17.1	-38.5	-28.7
α_{TR}	-27.2	-14.8	-17.1	-38.5	-28.7
Temperature variations [oC]					
	125	85	50	27	0	-40
f_0	204	229	245	251	263	269
α_N	-41	-31	-33	-30.6	-40	-31
α_{TK}	-38	-30	-32	-30	-40	-31
α_C	-21	-24	-26	-26.9	-35	-35
α_{TR}	-21	-24	-26	-27.2	-35	-35
Process variations of resistor			
	MIN	TYP	MAX
f_0	281.8	251.2	234.4
α_N	-29.2	-30.6	-30.8
α_{TK}	-28.2	-29.6	-33.8
α_C	-26.0	-26.9	-28.3
α_{TR}	-25.7	-27.2	-28.1
Process variations of capacitor			
	MIN	TYP	MAX
f_0	275.4	251.2	223.9
α_N	-23.5	-30.6	-32.6
α_{TK}	-22.9	-29.6	-33.0
α_C	-20.5	-26.9	-36.5
α_{TR}	-20.8	-27.2	-37.0
Voltage variations [mV]			
	540	600	660
f_0	239.9	251.2	263.0
α_N	-30.4	-30.6	-27.0
α_{TK}	-30.0	-29.6	-26.2
α_C	-31.8	-26.9	-26.6
α_{TR}	-31.2	-27.2	-26.3

Table 4: Comparison of the filter performance

Characteristics	[11]	This work
Technology	0.18 µm	0.13 µm
Power supply	±0.5 V	±0.6 V
Power consumption	35 µW	5.4 mW
Center frequency	2.5 MHz	251 MHz
Number of OTAs	3	4
Number of inverters	1	0
Number of transistors	34	37

4 Conclusion

This paper proposes a new MISO mixed-mode universal OTA-C filter. The filter consists of four OTAs and two capacitors. A simple differential amplifier with unity feedback is used as the final OTA stage to convert the voltage signal to a current signal at the filter output. This approach achieves better stability of the OTA characteristics compared to a simple inverter amplifier, resulting in significantly lower filter sensitivity to PVT variations. The filter is designed using the UMC 130 nm MM/RF CMOS process. Post-layout simulations performed using Cadence Design Systems software with the Spectre simulator confirmed the features of the proposed topology. The results verified the superiority of the proposed filter in terms of sensitivity to PVT variations, particularly in transconductance and current modes, with no variations in attenuation within the passband. Furthermore, the results indicate that this study achieved a significantly higher center (cut-off) frequency for the filter compared to the reference work, albeit at the cost of increased overall circuit power and area consumption.

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6 Conflict of interest

The authors declare that they have no conflict of interest.

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