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Temperature and process compensated RF power detector

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Abstract: This paper describes the design of process and temperature compensated wide band radio frequency power detector in a standard UMC 0.13-µm RF CMOS process. Proposed power detector core consists of two RF NMOS transistors biased for operation in weak inversion and output signal of the power detector core is a linear function of input RF peak voltage and residual temperature dependence. Additional compensation circuit is designed in order to make the output voltage less sensitive on temperature and process variation. Power detector circuit has 20 dB of the dynamic range and is especially suitable for use in transmitter chain applications. The temperature compensation provides typical reduction of 50% in temperature sensitivity of the circuit.

Keywords: RF power detector; temperature compensation; weak inversion; Bessel function; compensation circuit

Temperaturno in procesno kompenziran RF detector moči

Izvleček: Članek opisuje dizajn procesno in temperaturno kompenziranega detektorja moči širokopasovne radio frekvence v standardni UMC 0.13-µm RF CMOS tehnologiji. Jedro detektorja se sestoji iz dveh RF NMOS tranzistorjev za delovanje v slabi inverziji. Izhodni signal detektorja je linearna funkcija vhodne RF napetosti in ostanka temperaturne odvisnosti. Dodatno kompenzacijsko vezje znižuje temperaturno in procesno odvisnost. Dinamično območje detektorja moči je 20 dB in je posebej primeren za uporabo v prenosnih verigah. Temperaturna kompenzacija tipično za 50 % zmanjša vpliv temperature.

Ključne besede: RF detektor moči; temperaturna kompenzacija; šibka inverzija; Besselova funkcija; kompenzacijsko vezje

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1 Introduction

Power detectors are widely used in wireless communication systems, in receiver and transmitter chain. Optimal gain setting of the receiver chain is highly dependent on the power level of the input signal. In order to meet optimum gain, power level of the input signal should be measured in real time and appropriate gain adjustment of the receiver chain should be performed. Characteristic for this application is that it requires the dynamic range of power detector circuit exceeding 50 dB or more.

In many applications transmitter should be capable to operate with variable peak level of the output power. In order to obtain accurate power gain control, power detector should be employed in the control feedback loop [1]. Power detectors are also used for: power amplifier emergency shutdown in case of high VSWR [2], predistortion linearization of power amplifier using envelope-feedback [3], or as a part of system for envelope elimination and restoration power amplifier [4].

Power detectors for transmitter applications have relaxed dynamic range requirements compared to those employed in receiver, but other factors may be of importance. Self-heating of the power amplifier affects the performance of power detectors by changing their accuracy [5]. In order to have temperature independent behavior, power amplifier and power detector are usually designed together due to the large mutual influence [5]. Another constraint for power detectors is requirement for low power consumption in order to keep high level efficiency of the overall system.

There are few groups of the power detectors – mixer based [6], Schottky diode [7] and monolithic low power

RF peak detector [8]. First two topologies are not quite suitable for CMOS RF IC implementation regarding: unavailability in standard CMOS RF process, bandwidth limitation, large chip size, high power consumption, etc.

Monolithic low power RF peak detector is most suitable for RF IC implementation due to its advantages of simplicity, wide bandwidth, low power and small chip area [8]. However, it has temperature and process dependence and wideband precision power detectors are mostly implemented in expensive bipolar technology [8].

In this paper, monolithic, low power, process and temperature independent RF peak detector has been developed. It uses NMOS transistors biased in weak inversion in order to get the exponential transistor behavior. Additional circuit for temperature and process compensation has been proposed. The new detector uses inexpensive RF CMOS technology and provides temperature and process independent power detection without post-fabrication trimming.

The paper structure is as following: the design of the power detector core circuit is presented in Chapter 2. Topology and design of the new temperature compensation circuit is presented in Chapter 3. Obtained simulation results and post processing with possible applications are presented in Chapter 4 and 5, respectively. Finally, conclusion is introduced in Chapter 6.

2 Proposed RF power detector

The core of the RF power detector is shown in Figure 1.

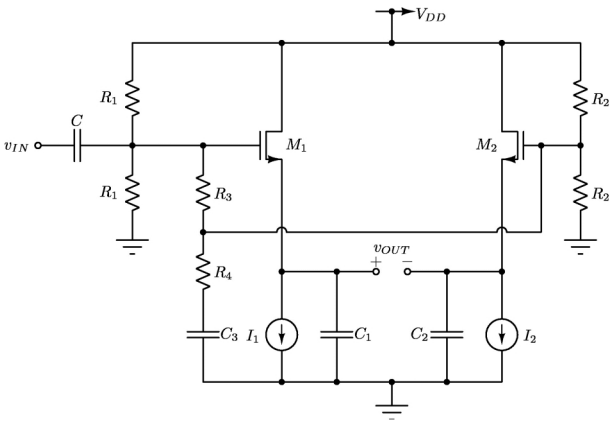

Figure 1: RF power detector core schematics

In order to obtain exponential behavior, transistors M_1 and M_2 are biased for operation in weak inversion. Transistors have the same channel width, number of fingers, length and their bias currents are equal $I_1=I_2=I_{DC}$. Corresponding resistors and capacitors are matched, namely, $R_1=R_2$, $R_3=R_4$, $C_1=C_2$. In this case, the AC signal magnitude at gate M_1 is two times greater than at the M_2 gate.

With given assumptions, instantaneous and average drain currents of transistor M_1 are:

$$i_{D1} = I_S e^{\frac{V_{gs1}-V_t}{nV_t}} = I_S e^{\frac{V_Q-V_T}{nV_t}} e^{-\frac{V_{OUT}^+}{nV_t}} e^{\frac{V_m\cos(\omega_0 t)}{nV_t}}, \quad (1)$$

$$\overline{i_{D1}} = I_1 = I_{DC} = I_S e^{\frac{V_Q-V_T}{nV_t}} e^{-\frac{V_{OUT}^+}{nV_t}} \frac{1}{T}\int_0^T e^{\frac{V_m}{nV_t}\cos(\omega_0 t)}\,dt = I_S e^{\frac{V_Q-V_T}{nV_t}} e^{-\frac{V_{OUT}^+}{nV_t}} I_0\left(\frac{V_m}{nV_t}\right). \quad (2)$$

Average drain current of transistor M_2 is:

$$\overline{i_{D2}} = I_2 = I_{DC} = I_S e^{\frac{V_Q-V_T}{nV_t}} e^{-\frac{V_{OUT}^-}{nV_t}} I_0\left(\frac{V_m}{2nV_t}\right). \quad (3)$$

Where:

V_m - peak amplitude of AC input signal
V_Q - gate DC voltage$I_0(x)$ - modified Bessel function of order zero
n - technology dependant sub-threshold slope parameter

From (2) and (3) it can be seen that average drain current is increased by a factor $I_0(V_m / V_t)$ when RF signal is present. Since the modified Bessel function of order zero is monotonically increasing, the average drain current monotonically increases with RF signal amplitude.

However, the average (DC) current of transistors M_1 and M_2 is constant, and set by current sources I_1 and I_2. Therefore, the average gate-source voltage V_{gs} must decreases for (2) and (3) to hold. This change in average V_{gs} due to input RF signal amplitude is the basis of power detector operation.

For large values of x, $I_0(x)$ has an asymptotic approximation:

$$I_0(x) \approx \frac{e^x}{\sqrt{2\pi x}}. \quad (4)$$

Using equations (2) and (3), the output voltage can be written as:

$$V_{OUT} = V_{OUT}^+ - V_{OUT}^-, \quad (5)$$

$$V_{OUT} = nV_t \ln\left(\frac{I_0\left(\frac{V_m}{nV_t}\right)}{I_0\left(\frac{V_m}{2nV_t}\right)}\right). \quad (6)$$

If we apply approximation (4) on the equation (6), we can get:

$$V_{OUT,PD} = \frac{V_m}{2} - \frac{nV_t}{2}\ln(2). \quad (7)$$

Where:

$$V_t = \frac{kT}{q}. \quad (8)$$

From equation (7), it can be recognized that the average output voltage consists of two factors. First term is proportional to the peak value of the input signal, and the second term is proportional to the temperature. Temperature-dependent term can be cancelled by including an additional circuit in the design, which produces the output voltage proportional solely to the temperature. Temperature dependence of the signal described in equation (7) may be minimized to a large extent by subtracting the power detector voltage from compensation circuit output. Design of temperature compensation circuit is presented in the following section.

3 Compensation circuit

Figure 2 presents topology of the compensation circuit that is used for compensation of the temperature dependent part in equation (7). Like in the core of the RF power detector, transistors M_A and M_B are operating in weak inversion. Transistor M_A has the same dimensions and the same biasing conditions as transistors M_1 and M_2 in the power detector core. The width of the transistor M_B is two times greater than the width of M_1 and they have same value of bias currents. Transistors M_C, M_D and M_E operate as current mirrors and should be perfectly matched. In order to keep same drain voltages in current mirrors, transistor M_F has been employed and it has to be matched with M_A. Additionally, the bias resistors should also be matched, $R_A = R_B = R_E$. The output current I_D of the circuit in the Figure 2 is given by the equation (9).

$$I_D = \frac{V_{GS1} - V_{GS2}}{R_3}. \quad (9)$$

Since transistors M_A and M_B are operating in the weak inversion, the output current is given with:

$$I_D = \frac{V_{GS1} - V_{GS2}}{R_3} = \frac{nV_t \ln\left(\frac{I_D}{I_{S1}}\right) - nV_t \ln\left(\frac{I_D}{I_{S2}}\right)}{R_3}, \quad (10)$$

$$I_D = \frac{nV_t \ln\left(\frac{I_{S2}}{I_{S1}}\right)}{R_3} = \frac{nV_t \ln(2)}{R_3}, \quad (11)$$

resistor value R_C should be set in a way that currents I_D and I_{DC} from detector circuit core shown in Figure 1 are equal. Furthermore, compensation circuit could be used as a current source for the power detector core.

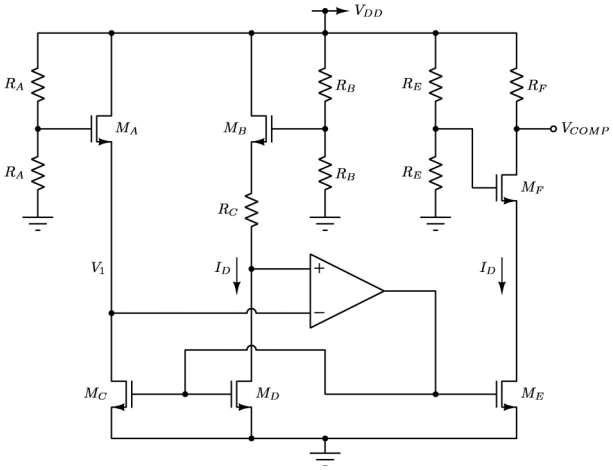

Figure 2: Compensation circuit

Output voltage of the circuit in Figure 2 is given with the following equation:

$$V_{COMP} = V_{DD} - \frac{nV_t R_F \ln(2)}{R_E}. \quad (12)$$

In order to get temperature independent signal, signals at the outputs of the power detector core and calibration circuit (given with equations (7) and (12)) should be subtracted, given the value for the compensated output voltage of the power detector circuit.

$$V_{OUT} - V_{COMP} = V_{DD} - \frac{V_m}{2} + nV_t \ln(2)\left(\frac{1}{2} - \frac{R_F}{R_E}\right). \quad (13)$$

If the value of the resistor R_F is two times smaller than value of R_B, we can get:

$$V_{OUT} - V_{COMP} = V_{DD} - \frac{V_m}{2}. \quad (14)$$

From last equation it can be recognized that the output voltage is temperature and process independent.

4 Simulation results

Based on the previous discussion power detector core and compensation circuit are designed in standard UMC 130nm CMOS RF technology. Parameters of all components are shown in Table 1.

Table 1: Parameters of the components

Components	Parameter	Value
M1, M2, MA, MF	W/L [µm/µm]	2*(5/0.34)
MB	W/L [µm/µm]	4*(5/0.34)
MC, MD, ME	W/L [µm/µm]	4*(4/2.5)
RC	Resistance [Ω]	3922
RF	Resistance [Ω]	1961
RA, RB, RE, R1, R2	Resistance [Ω]	60000
R3, R4	Resistance [Ω]	25
C, C1, C2, C3	Capacitance [pF]	10
I1, I2	Current [µA]	10

Layout of complete chip is presented in Figure 3.

Figure 4 presents voltage sensitivity $\partial V_{OUT}/\partial V_m$ of the output signal performed at frequency of 5GHz. The dynamic range of the input signal amplitude can be estimated from this figure. Lower limit is determined by modified Bessel function approximation given in the equation (4). Namely, this approximation is valid for input AC amplitude greater than 0.2 V. Upper limit presents the highest peak level of the voltage input signal for which all transistors are in saturation. This voltage is determined to be 2 V, giving the operation range of the power detector of approximately 20 dB.

It can be concluded that power detector works with high amplitude level of the input signal, what is desirable for RF transmitters.

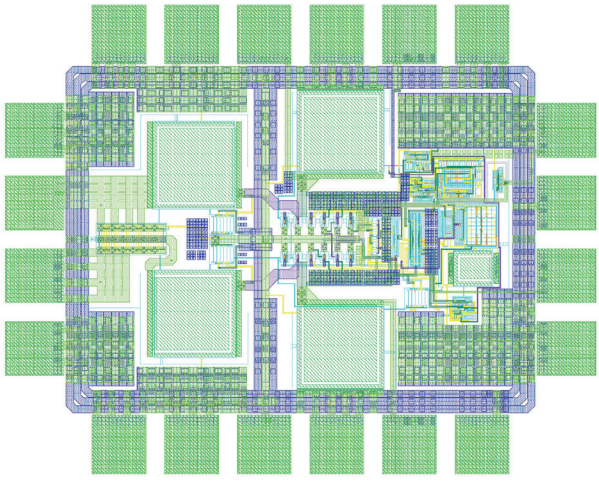

Figure 3: Power detector with calibration circuit

The power detector is simulated with and without the compensation circuit, in order to demonstrate the improvement. Simulations were performed for AC signal magnitude of 1 V and frequency of 5 GHz. Improvement is reached in industrial temperature range of -40 ^{0}C to 100 ^{0}C. Maximum temperature coefficient $(\partial V_{OUT}/\partial T)_{MAX}$ is decreased about two times using this technique.

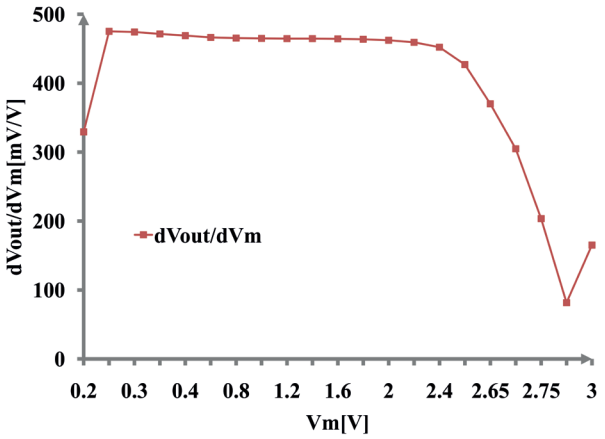

Figure 4: Voltage coefficient of the signal at the output of the power detector

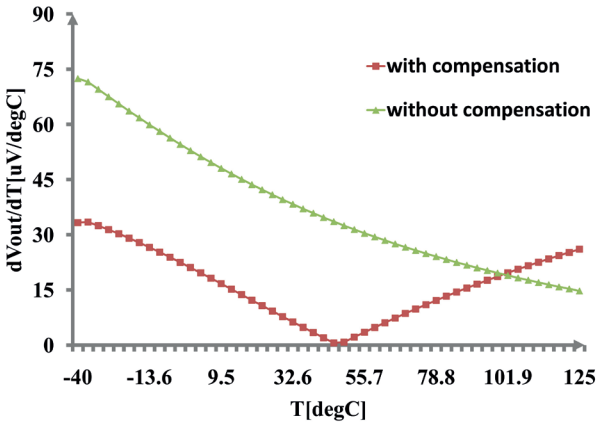

Figure 5: Compensated (red) and non-compensated (green) temperature coefficient of the output signal

5 Post processing and applications

Post processing can be done in analog or digital domain. Each of these options will be discussed in the details including advantages and drawbacks as well as possible applications.

5.1 Analog post processing

Straightforward way to combine the power detector core with the compensation circuit is to use instrumentation amplifiers to perform subtracting and amplifying.

The most important parameter for the amplifiers would be input offset in order to keep high level of accuracy. Clear advantage is simple design and ability to detect input amplitude independently of process or temperature variation. Main disadvantage is small dynamic range 20dB. Although, there are some applications

where this might be enough as; amplifier linearization techniques [9] including polar loop system [10] and amplitude envelope feedback system [10].

5.2 Digital post processing

Dynamic range might be increased using digital post processing. Power detector output voltage (6) and compensation circuit output voltage (12) could be sampled and post processed in digital domain. Parameter nV_t might be extracted from (12) and be used in (6) for extraction of the amplitude V_m. Dynamic range is extended since there is no need for the asymptotic Bessel function approximation (4). Drawback would be complex design. This technique could be used for broad range of applications where temperature and process independent amplitude detection is needed.

6 Conclusion

Today, inexpensive scaling CMOS technology allows large level of integration and operation of the circuits at high frequencies. Its main disadvantage is limitation of the process control, which leads to large variation of component parameters. Wide temperature operation range limits the accuracy of power detector due to temperature-dependent terms in output voltage. In some particular cases, this limitation can be solved by using such circuit topologies which performance depends only of well controlled component matching. This paper presented design of such power detector including compensation circuit.

Using the proposed and described circuit topology, significantly lower temperature dependence of the power detector circuit has been achieved. Namely, maximum temperature coefficient is decreased about two times for input signal level between 0.2 V and 2 V. Power detector temperature dependency is minimized to the extent that it can be neglected in many industrial applications, enabling its widespread use in further designs. For applications which require higher dynamic range, digital post processing could be applied.

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