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Real Time Implementation of PI and PID Controlled Cascaded H-Bridge Eleven Level Inverter using SPWM

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Abstract: Multilevel inverters are nowadays widely used in high-power and high-voltage applications. A multilevel inverter synthesizes a large number of levels to get the desired output voltage levels and they have lot of merits such as improved output waveform, smaller passive filter size, lower Electro Magnetic Interference and reduced harmonics. However, multilevel inverters also have some disadvantages such as increased number of components, voltage-balancing problem and higher switching losses. This paper presents a PI and PID Controlled Cascaded H-bridge eleven level inverter based sinusoidal pulse width modulation control technique suitable for improved power quality applications. The main objective of reducing the THD of output of the chosen eleven level cascaded inverter under set point tracking as well as steady-state with fast transient response are proposed from control point of view. Simulation results have been discussed that the cascaded H-bridge eleven level inverter performs perfectly in connection with PI or PID. A comparative analysis of these two different controllers is revealed. Harmonic spectrum and output voltage and current waveforms have been obtained to validate the role of controllers. Experimental results are presented to confirm the simulation results.

Keywords: Multilevel inverter; Cascaded H-Bridge multilevel inverter; Total Harmonic Distortion; Sinusoidal pulse width modulation; PI Controller; PID Controller

Implementacija PI in PID kaskadnega H-mostičnega enajstopenjskega inverterja v realnem času z uporabo SPWM

Izvleček: Večstopenjski inverterji so danes široko uporabljeni v močnostnih in visoko napetostnih izdelkih. Za doseganje visokih napetosti združujejo veliko število napetostnih izhodov. Odlikujejo jih številne lastnosti, kot so izboljšan izhodni signal, manjši pasivni filter, nizka elektromagnetna interferenca in zmanjšanje harmonikov. Imajo pa tudi slabosti, kot so: veliko število elementov, uravnavanje napetosti in višje preklopne izgube. Članek predstavlja PI in PID krmiljen kaskadni H mostič enajstopenjskega inverterja na osnovi sinusne pasovno širinske modulacije. S stališča kontrolne so predstavljeni glavni vidiki znižanja THD izhoda pri sledenju točk, kakor tudi v stacionarnem stanju. Prikazana je primerjalna analiza dveh inverterjev, rezultati po so potrjeni tudi eksperimentalno.

Ključne besede: večstopenjski inverter; kaskadni H mostič; harmonsko popačenje; sinusna pulzni-širinska modulacija; PI kontroler; PID kontroler

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1 Introduction

Numerous industrial applications require electrical power in large quantities and of high quality and the demands are fast growing in recent years [1]. For various industrial drives applications, power-electronic inverters are becoming more popular [2]. A multilevel inverter is a power electronic device having several levels of dc voltages as inputs and produces a desired output voltage. Recently, multilevel power conversion technology has been developing very fast in the area of power electronics with good potential for future developments. As a result, the medium to high voltage range is the most attractive application of this technology [3]. A multilevel inverter not only enables the use of renewable energy sources, but also achieves high power ratings. A multilevel inverter system can be easily interfaced to renew-

able energy sources such as photovoltaic, wind, and fuel cells for high power applications.

The advantages of multilevel inverters is their smaller stepped output voltage, which results in lower switching losses, lower harmonic components, better electromagnetic compatibility, high voltage capability and high power quality [4]. For both low switching frequency and high switching frequency PWM, multilevel inverters are available with configurations. It must be noted that high switching frequency PWM means lower efficiency and higher switching loss and low switching frequency PWM means higher efficiency and lower switching loss [5].

The patent result search shown that multilevel inverter circuits have been around for more than 25 years. Today, in medium voltage levels with high-power applications, multilevel inverters are widely used [6]. The main field applications are in laminators, pumps, conveyors, compressors, fans, blowers, and mills. Later, there are several topologies have been developed for multilevel converters [7]. There are three different topologies proposed for multilevel inverters are as follows cascaded multi cell with separate dc sources, diode clamped (neutral-clamped) and capacitor-clamped (flying capacitors). These topologies have a different mechanism for providing the voltage level. The series H-bridge was the first topology introduced and more configurations have been developed for this topology [7]. Since this topology consists of series power conversion cells, the power and voltage levels may be scaled easily. The Series H-bridge topology was followed by the diode-clamped converter that utilized a bank of series capacitors [8]. After few years, flying capacitor topology followed diode-clamped topology. This topology uses floating capacitors to clamp the voltage levels, instead of series connected capacitors [9]. H-bridge inverters do not require either flying capacitor or clamping diode inverters because they have isolation transformers to isolate the voltage source.

Moreover, more than enough modulation techniques and control models have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others [10], [11]. In this paper, in order to generate the switching signals of the power converter a special sinusoidal pulse-width modulation (SPWM) technique was implemented. Some requirements must be satisfied when shoot through states are generated, for instance, shoot-through states have to be uniformly distributed during the whole output voltage period with constant width and the average output voltage should remain unaffected. These features result in several merits, such as low ripple input current, low value of the passive elements, reduction in output voltage THD, and gaining of the desired boost factor[12].In addition, many multilevel converter focused on applications such as industrial medium-voltage motor drives [13], utility interface for renewable energy systems [14], flexible AC transmission system (FACTS) and traction drive systems [15], [16]. To improve the power quality in the distribution network , Shunt Active Power Filters using PI, PID and Fuzzy Logic Controller (FLC) for power line conditioners (PLC) have been proposed [17]. In order to maintain the output load voltage at the desired value to supply the power for a variety of loads with a minimum THD , a deadbeat-based proportional-integral (PI) controller using a battery cell as the primary energy source for a stand-alone single-phase voltage source inverter has been proposed [18].

In paper [19], in order to eliminate the Total Harmonic Distortion (THD) and improve the power factor, DSTATCOM drawn from a Non-Linear Diode Rectifier Load has been proposed. In this paper [20] , a nine stepped multilevel power inverter has been designed, which chooses a multi-PWM optimized using genetic algorithms (GA), and minimizing Total Harmonic Distortion (THD) of the first 50 harmonics to about 0% has been presented. In addition,[21] a 43-level asymmetric uniform step cascaded multilevel inverter (CMLI) has been introduced which consists of four H-bridges per phase, with different dc sources of values E, 2E, 7E and 11E and a mixed integer linear programming (MILP) optimization model was employed to determine the switching angles of the CMLI power switches which can minimize the values of any undesired harmonics.

A typical single-phase nine-level inverter chooses full-bridge configuration by using suitable sinusoidal modulation technique as the power circuits. The output voltage has nine levels: zero, positive (+Vdc,+2Vdc,+3Vdc,+4Vdc), and negative(–Vdc,-2Vdc,-3Vdc,-4Vdc) supply dc voltage (assuming that Vdc is the supply voltage). By using the carrier frequency and switching functions, the harmonic components of the output voltage are determined. Therefore, their reduction of harmonics is just restricted to a certain degree.

To overcome this drawback, this paper presents an eleven-level inverter whose output voltage can be obtained in eleven levels. The harmonic content can be reduced, as the number of output levels increases. THD reduction [22] can be considered from three different views namely: by considering new switching strategies, by designing alternative circuit topological structures and by proposing suitable control techniques. The third view, i.e. proposition of suitable control technique is an alternate solution for THD reduction is

discussed in this paper. In view of the inherent merits, Cascaded H-bridge inverter and SPWM control strategy are used in this work. This H-bridge inverter topology uses five reference signals to generate PWM signals for the switches.

In this paper, the performance of both PI and PID controllers are compared and analyzed to minimize total harmonic distortion in cascaded H-bridge eleven level inverter. Results confirm the effectiveness of the proposed controller. The experimental results are presented to confirm the simulation results and thus the proposed idea.

This paper has been arranged as follows. After the introduction in section 1, Section 2 gives an outline of cascaded h-bridge multilevel inverter topology. Then, the Cascaded H-bridge eleven level inverter with PI and PID controllers are explained in Section 3. The two sections 4 and 5 show the simulation and experimental results that validate the proper operation of the inverter. Conclusion and final remarks are made in Section 6.

2 Cascaded H-bridge eleven level Inverter topology

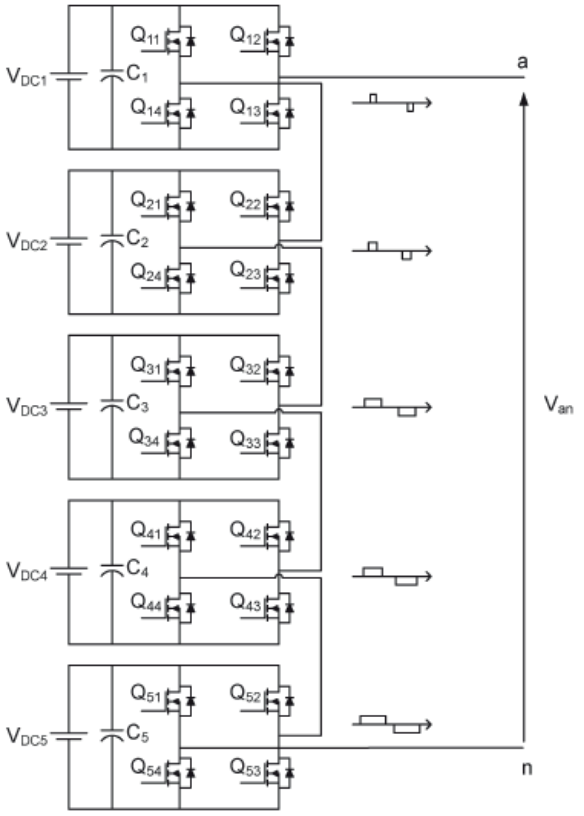

Figure 1: Schematic of a single-phase cascaded h-bridge eleven level inverter

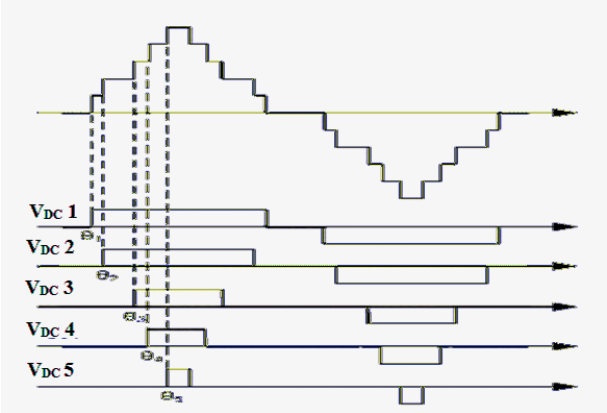

Figure 2: Output voltage waveform of a single-phase cascaded eleven level inverter

Fig. 1 and 2 show the Schematic diagram and Output voltage waveform of a single-phase cascaded h-bridge eleven level inverter. A single-phase 11-level inverter is formed by connecting five identical inverter modules in series. All five identical inverter modules having the same magnitude are fed by DC voltage sources. During the positive half cycle, the power electronic switches (Q11, Q13) are in the on-state, and the power electronic switches (Q12, Q14) are in the off-state. Likewise, during the negative half cycle the power electronic switches (Q11, Q13) are in the off-state, and the power electronic switches (Q12, Q14) are in the on-state and vice versa. The output voltage of the inverter has eleven voltage levels from -5 Vdc. to +5 Vdc. Each of the different full-bridge inverter ac output levels are connected in series such that the total voltage waveform is the sum of the inverter outputs.

The number of phase output voltage levels m in a cascaded h-bridge inverter is given by

$$m = 2n+1 \quad (1)$$

where n is the number of separate dc sources.

Each H-bridge unit produces a quasi-square waveform by phase-shifting the switching timings of its positive and negative phase legs.

3 Cascaded Multilevel Inverter(MLI) with PI and PID Controllers

A PI controller is built for MLI to examine the system behavior, The Cascaded H-Bridge Multilevel inverter with PI controller is shown in Fig. 3. The gate signals are generated using SPWM strategy. The isolated dc power sources are connected to the Cascaded H-bridge in-

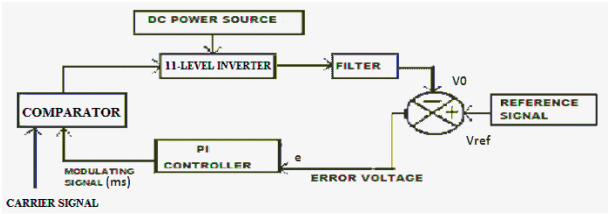

Figure 3: Cascaded MLI with PI Controller

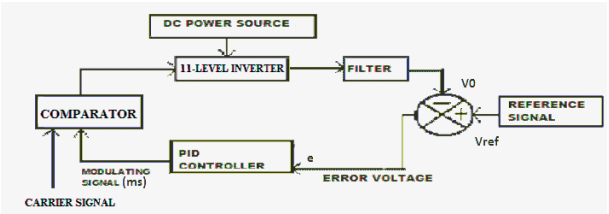

Figure 4: Cascaded MLI with PID Controller

verter. The eleven level output of the cascaded inverter is given to the load through LC filter to obtain sinusoidal output (Vo) and is compared with the reference voltage (Vref) to produce the error signal (e). The input to the PI controller is e. The output of the PI controller i.e the modulating signal (ms) is compared with carrier signal which is used to generate the gating pulses. Thus to get the required sinusoidal output voltage a voltage feedback loop is established. Hence, when the distortion in the output is more, the load is non linear. Using Ziegler – Nichols tuning technique PI controller settings Kp and Ki are designed in this work and the designed values of Kp and Ki are 0.1 and 0.01 respectively.

The Cascaded H-bridge Multilevel inverter with PID controller is shown in Fig. 4.The PID-controller is a linear combination of the P, I and D contributions carried out on the error. Sinusoidal pulse width modulation strategy generated the gate signals. The five isolated dc power sources are connected to the Cascaded H-bridge eleven level inverter. The output of the cascaded h-bridge eleven level inverter is given to the load through LC filter to obtain sinusoidal output (Vo) and is compared with the reference voltage (Vref) to produce the error signal (e). The input of the PID controller is error e. The output of the PID controller is multiplied with the unit reference signal to provide the required modulating signal (ms) and is used to produce the gating pulses in association with a carrier. Using Ziegler – Nichols tuning technique , PID controller settings Kp, Ki and Kd are designed in this work. The designed values of Kp, Ki and Kd are 0.1,0.01 and 0.001 respectively. The

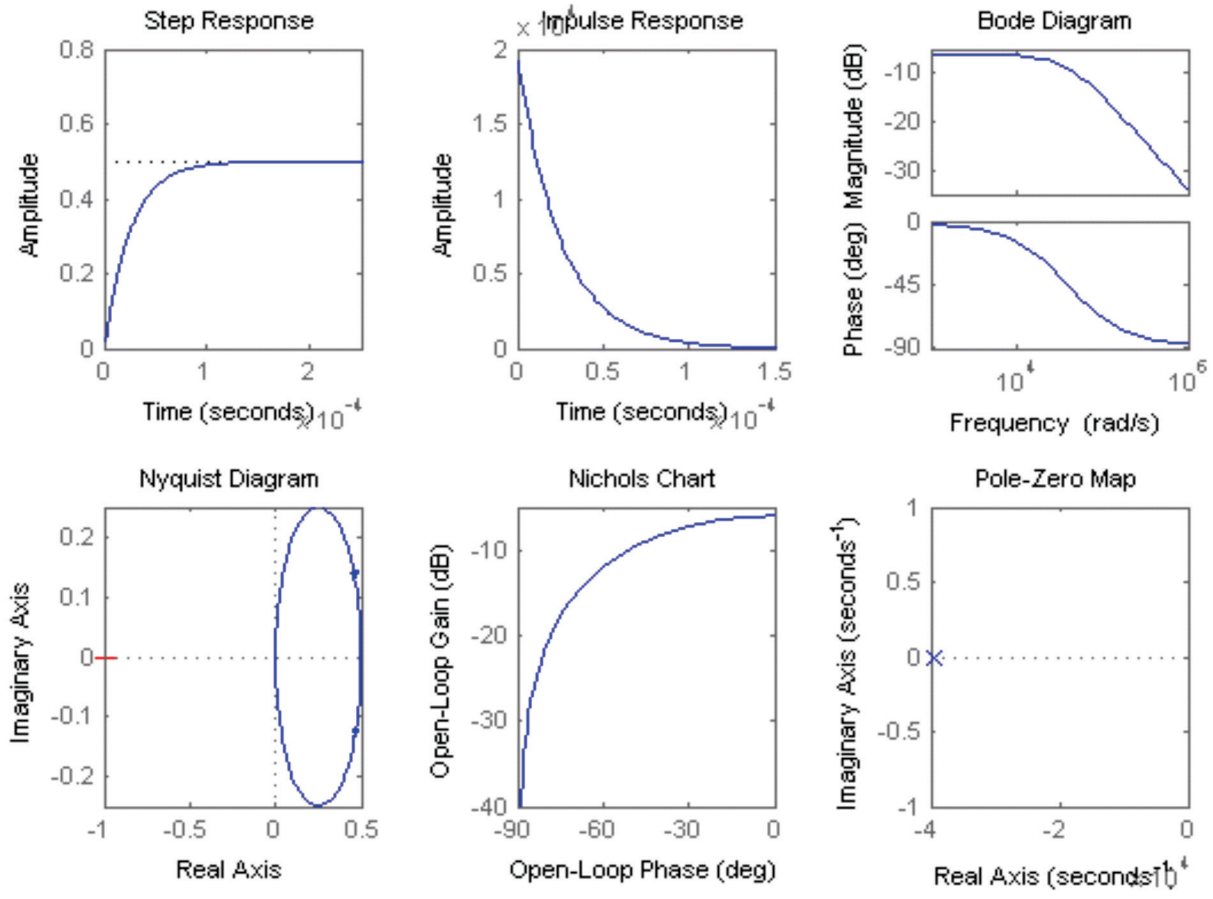

Figure 5: PID stability plots

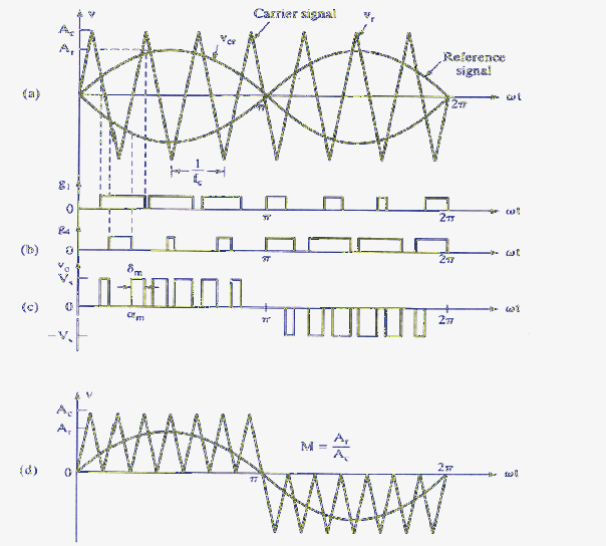

Figure 6: Sinusoidal Pulse width modulation a) Carrier and reference for bipolar modulation; b) pulses for bipolar modulation c) pulses for unipolar modulation d) carrier and reference for unipolar modulation

step response, bode plot, Nichols chart, nyquist, impulse response and pole-zero mapping are presented by carrying out the corresponding stability analysis shown in figure 5.

There are several switching control strategies have been proposed for Cascaded H-Bridge (CHB) inverters. High switching frequency PWM technique is widely used for eliminating harmful lower order harmonics in inverters. Several times the inverter switches are turned ON and OFF during every half cycle and by varying the pulse width output voltage is controlled in PWM control. This paper chooses the sinusoidal PWM control strategy because instead of maintaining the width of all pulses the same as in the case of multiple PWM, each pulse width is varied in proportion to the sine wave amplitude determined at the same pulse. The distortion is reduced importantly compared to multiple PWM. The gating pulses are shown in figure 6.

4 Simulation results

The performance of the proposed PI and PID controllers based cascaded H-bridge eleven level inverter with isolated dc sources is determined through MATLAB/ SIMULINK software. The elements and the parameters considered for simulation are presented in Table 1.

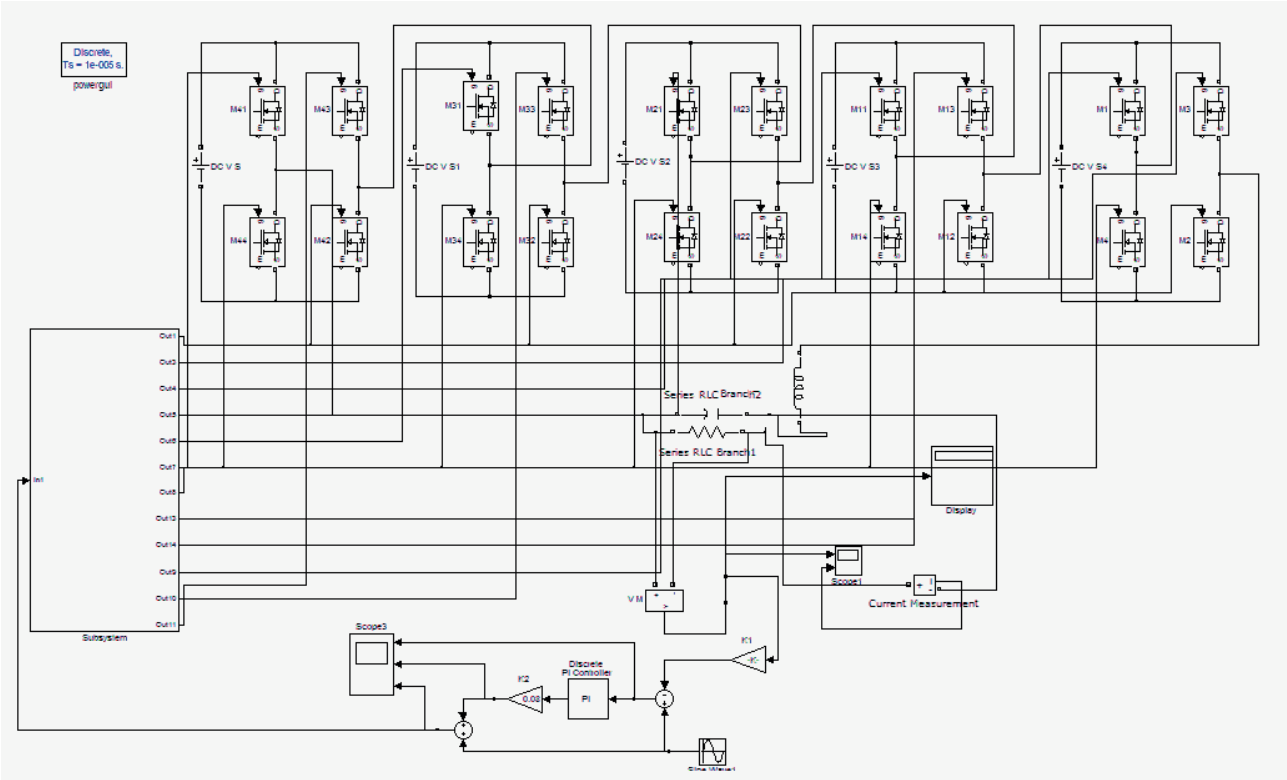

Figure 7: Simulink model of the Cascaded MLI with PI Controller

Table 1: Parameters of the Cascaded H-Bridge Inverter

Parameters	Values
No. of H-Bridge levels	5
No. of Switches	20
DC source voltage for individual H- bridge	34.8V
Fundamental frequency	50Hz
Load resistor	100 Ohm
Load Inductor	40mH

Case 1 : PI controller

The simulation model of cascaded h-bridge eleven level inverter topology using PI controller is shown in

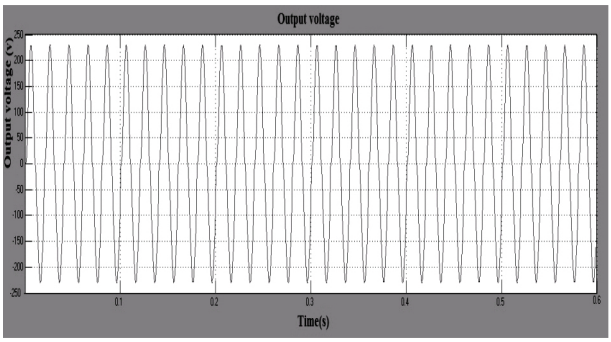

Figure 8: Load voltage waveform(PI Controller)

fig.7. The main power circuit consists of five H-bridges whose dc voltage is considered to be 34.8 V and the eleven level stepped output voltages are obtained and the harmonics are reduced. It also consists of PWM

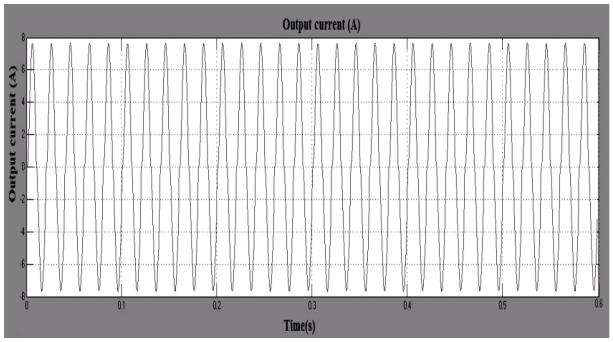

Figure9: Load current waveform(PI Controller)

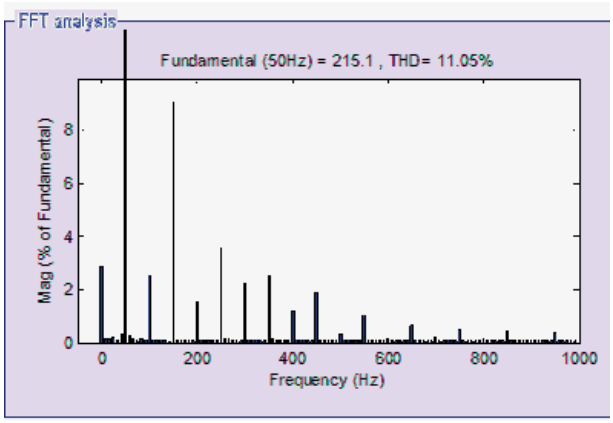

Figure10: Voltage THD

block and has parameters as amplitude, pulse width period and phase delay which is used to determine the shape of the output .Therefore the inverter efficiency is increased. The inverter must perform reliably and

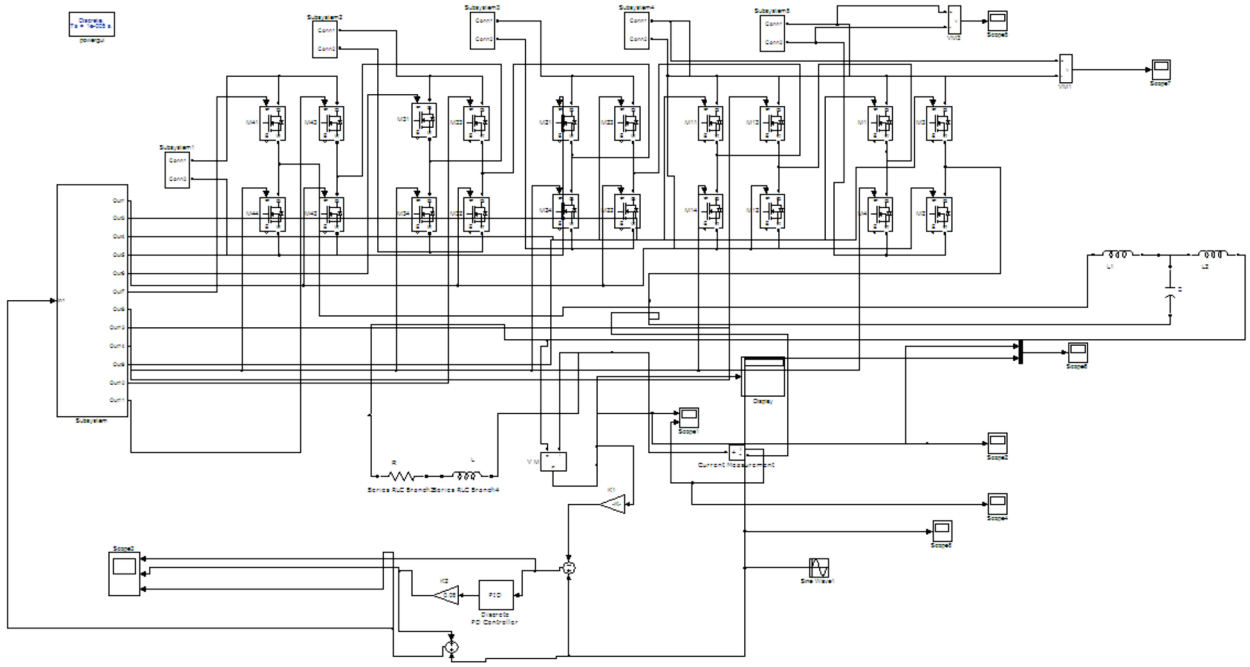

Figure 11: Simulink model of the Cascaded MLI with PID Controller

efficiently to supply a wide range of ac loads with the voltage and required power quality necessary for reliable and efficient load and system performance. The advantages of the proposed topology are high power high voltage handling capability, lower harmonics and lower switching loss. The output voltage and output current of cascaded h-bridge eleven level inverter has eleven levels. The inverter fundamental frequency is 50 Hz. The loads are connected across the cascaded H-bridge eleven level inverter.

The response of the MLI with PI controller is satisfactory and the load voltage and load current is shown in figure 8 and 9. The Total Harmonic Distortion waveform is shown in figure 10. It is observed from the results that the peak overshoot in the output voltage is 5.4 % and the total harmonic distortion is 11.05 %.

Case 2 : PID controller

The Simulink model of the Cascaded MLI with PID Controller is shown in figure 11. The response of the MLI with PID controller is also satisfactory and the load voltage and load current is shown in figure 12 and 13. The Total Harmonic Distortion waveform is shown in figure 14.

It is observed from the results that the peak overshoot in the output voltage is 4.4 % and the total harmonic distortion is 9.70 %. The performance of the controllers is tabulated in Table 2. Hence it is observed from the simulation results that the peak overshoot, settling time , THD are reduced in the output voltage and higher fundamental rms voltage using PID controller.

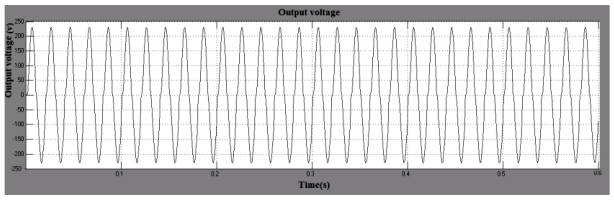

Figure 12: Load voltage waveform(PID Controller)

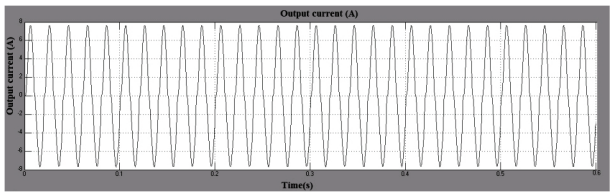

Figure 13: Load current waveform(PID Controller)

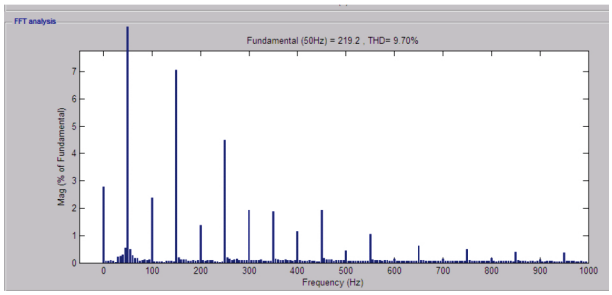

Figure 14: Voltage THD

Table 2: Comparison of Controller Performance

Controllers	Peak Overshoot	Settling Time	RMS fundamental voltage	THD%
PI	5.4	0.04	215.1	11.05
PID	4.4	0.01	219.2	9.70

5 Experimental results

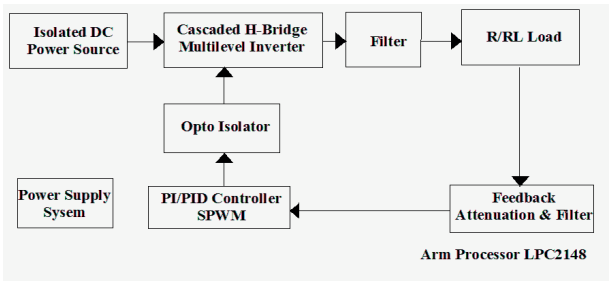

Figure 15: Experimental block diagram

The experimental block diagram of proposed Cascaded H-bridge inverter topology is shown in Fig. 15. This proposed block diagram consists of a multilevel DC/AC power inverter, Optocoupler, Arm processor, filter and a load. The isolated dc power sources are connected to the Cascaded H-bridge inverter. The output of the eleven level inverter is ac voltage which is connected to the load through filter and the load is considered as resistive and an inductive. PI and PID controllers are employed to minimize total harmonic distortion in cascaded H-bridge eleven level inverter.

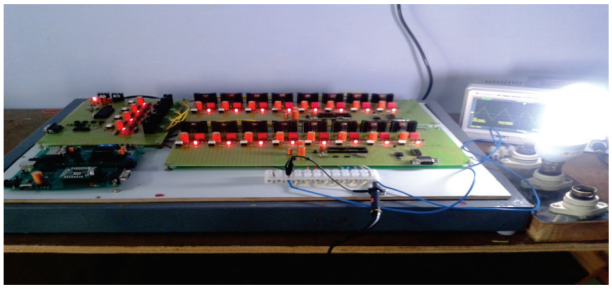

Figure 16: Structure of the experimental prototype

A single phase 0.3kW hardware prototype 11-level inverter as shown in Fig. 16 is developed. It consists of five full-bridge inverters and are connected in a series manner. The inverter uses 8-A, 500-V MOSFETs as the switching devices and the DC source voltage of each H-bridge inverter is selected to be 34.8V and is constant . The output frequency is assumed to be 50 Hz. Five transformers (0-24V, 2A) are used to power up the individual H- bridge inverters. Three transformers (6V-0-6V, 500mA) are used to power up the opto couplers.

The real time implementation of PI and PID controllers for eleven level inverter using LPC2148 Arm Processor is carried out in this work. Sinusoidal PWM strategy for the eleven level inverter is developed using MATLAB software. The PI and PID controllers generate the compensating signal to provide the required modulating signal for regulating the output voltage of this inverter.

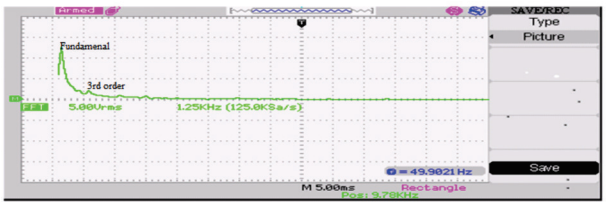

Figure 17: Harmonic spectrum of the inverter output voltage

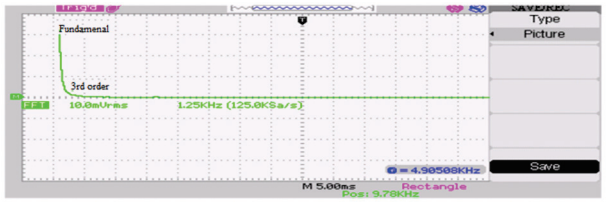

Figure 18: Harmonic spectrum of the inverter output current

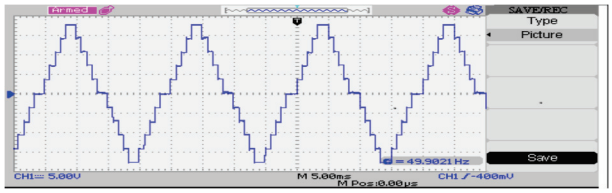

Figure 19: Output voltage waveform

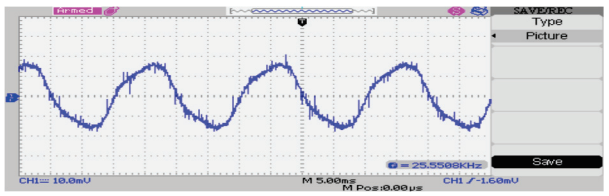

Figure 20: Output current waveform

Fig. 17 and 18 shows the harmonic spectrum of the inverter output voltage and output current . Fig. 19 shows the output voltage waveform. Fig. 20 shows the output current waveform. The elements and the parameters considered for implementation are presented in Table 3 for the cascaded h-bridge eleven level inverter topology.

Table 3: Experimental Parameters of the Cascaded H-Bridge Inverter

Parameters	Values
No. of H-Bridge levels	5
No. of Switches MOSFET IRF840 – 20Nos.	500V,8A
DC source voltage for individual H- bridge	34.8V/2A
Fundamental frequency	50Hz
R Load	47 Ohm
RL Load	47 Ohm,10mH
Opto Couplers MCT2E (20 Nos.)	30V,3A
Filter Capacitor	1000µF
Transformers(5 Nos.)	0-24V,2A
Transformers (3 Nos. for individual H- bridge)	6V-0-6V,500mA

With reference to table 4 a comparison of THD of the output voltage have been done. It is clearly shown that the results of simulation are closer to the experimental values.

Table 4: Comparison of THD of the output voltage

THD (%)		
Controllers	Experimental	Simulation
PI	11.01	11.05
PID	9.2	9.70

6 Conclusion

The real time implementation of PI and PID control strategies for single phase cascaded h-bridge eleven level inverter have been carried out and the results are compared and analyzed. From the obtained simulation results, it is found that PID performs better than PI controller since it provides output with relatively low harmonic distortion and higher fundamental rms output voltage. The PID controller yields a smaller overshoot in the output voltage, quick settling time, good dynamic response and lower total harmonic distortion than the PI controller for power quality applications. The measured value of total harmonic distortion of the inverter output voltage satisfies the IEEE-519 constraints.

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