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Low-Voltage Highly Linear Floating Gate MOSFET Based Source Degenerated OTA and its Applications

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Abstract: The paper proposes a novel low-voltage highly linear floating gate MOSFET based source degenerated OTA. The low voltage operation of the proposed OTA is achieved by using floating gate MOSFETs as input transistors and the linearity is increased by using source degeneration linearization technique. The proposed OTA has low power supply requirement of ±0.6V, rail-to-rail input differential voltage range and wide bandwidth of 1.472 GHz. The applications of the proposed OTA such as active inductor, tunable resistors and filters are also proposed. Finally, the simulation results of the proposed circuits using typical parameters of UMC 0.18 µm CMOS technology are depicted to confirm the theoretical analysis.

Keywords: Active inductor; filters; floating gate MOSFET; OTA; resistors

Nizkonapetostni linearen vhodno izrojen OTA na osnovi MOSFETa s plavajočimi vrati in njegova uporaba

Izvleček: Članek predlaga nov nizkonapetostni linearen vhodno izrojen OTA na osnovi MOSFETa s plavajočimi vrati. Nizko napetostno delovanje je zagotovljeno z uporabo vhodnih MOSFET-ov s plavajočimi vrati, linearnost pa je povečana za uporabo tehnike izroditve vira. Predlagan OTA zahteva napajanje ±0.6V, polni diferencialen napetostni obseg in široko pasovno širino 1.472 GHz. Predlagana je uporaba OTA kot dušilka, nastavljiv upor in filter. Simulacijski rezultati v UMC 0.18µm CMOS tehnologiji potrjujejo teoretične analize.

Ključne besede: aktivna dušilka; filter; MOSFETR s plavajočimi vrati; OTA; upor

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1 Introduction

In recent years, with miniaturization of technology, the demand of low voltage power supply has become essential. For designing of analog circuits, it has become the major factor that they operate with low supply voltage and power as their digital counterparts. Analog designers face many difficulties and challenges due to the limited voltage headroom, because the threshold voltage and drain-to-source saturation voltage of CMOS technologies do not scale down at the same rate as the supply voltage or do not scale at all with low supply voltage. The power supply requirement of analog circuits can be reduced by two techniques known as technology modification and transistor implementation [1]. Using technology modification technique, the device technology dependent threshold voltage can be reduced. But, higher threshold voltage gives better noise immunity and the lower threshold voltage reduces the noise margin to result in poor signal to noise ratio (SNR). Hence, for present day CMOS technology, reduction in threshold voltage is limited to the noise floor level, below which further reduction will introduce an amount of noise sufficient to result in very complex circuits.

Some of the transistor implementation techniques available in literature are level shifters, self-cascode MOSFETs, sub-threshold MOSFETs, bulk-driven MOS-

FETs, floating gate MOSFETs [2-3], etc. Out of these floating gate MOSFETs present a unique advantage of programmability of threshold voltage, which can be lowered from its conventional value, thus makes it suitable for low voltage applications [4-5]. FGMOS is also compatible with standard double-poly CMOS process technology and has been used to develop digital-to-analog (D/A) converters [6], voltage controlled resistors [7]-[8], neural networks [9], operational transconductance amplifiers [5], dividers [8, 10], etc. Motivated by the unique characteristics of the floating gate MOSFETs, a highly linear OTA is proposed. The OTA is a versatile building block employed as the active cell in many analog integrated circuits such as continuous-time filters [11-14], variable gain amplifiers [15], etc.

The paper is organized as follows. The operation of floating gate MOSFET is discussed in Section 2. Section 3 proposes floating gate MOSFET based source degenerated OTA. The applications of proposed OTA such as active inductor, tunable resistors and filters are proposed in Section 4. In Section 5, simulation results are given to demonstrate the effectiveness of the proposed circuits. The paper is concluded in Section 6.

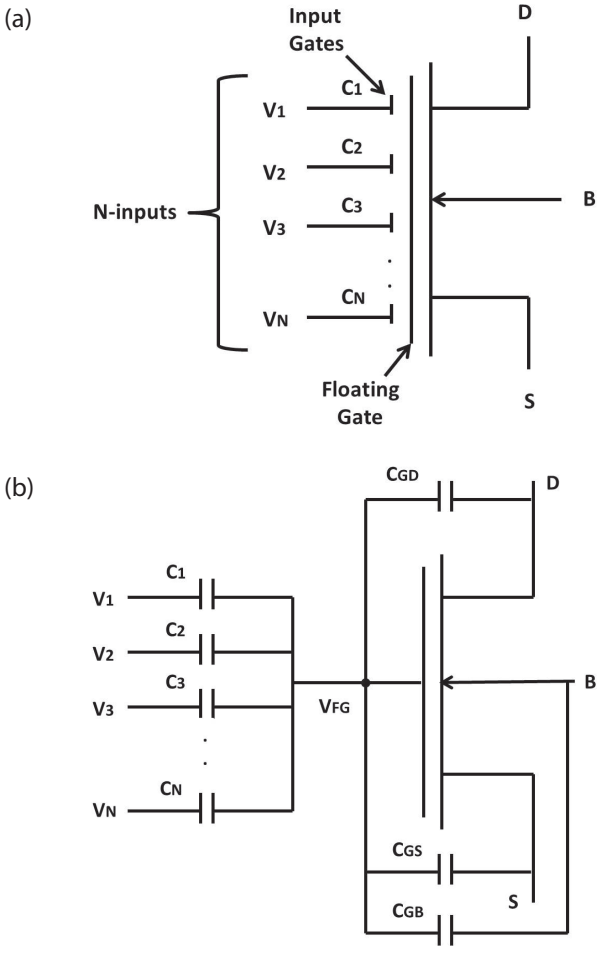

Figure 1: Floating gate MOSFET (a) Symbol and (b) equivalent circuit model

2 Operation of floating gate MOSFET

The structure of floating gate MOSFET is similar to a conventional MOSFET. The difference between these two is the gate, which is electronically isolated, creating a floating node in DC, and a number of secondary gates electrically isolated from the floating gate, above which they are deposited. There exist only capacitive connection between inputs and floating gate [16]. The floating gate which is completely surrounded by highly resistive material serves as charge storage device. Therefore, the first application of the floating gate MOSFET was to store the digital information for very long period in structures such as EPROMs, EEPROMs and Flash memories [17]. Along with this, floating gate MOSFET devices show easy addition and compression of voltage signals, as well as allow a reduction of the effective threshold voltage. The threshold voltage of a floating gate MOSFET can be controlled by the amount of the static charge stored in the floating gate. This property has prompted their use in low voltage low power analog circuits [18]. The symbol and equivalent circuit model of N-input floating gate MOSFET are shown in Figures 1 (a) and (b) respectively. In both the figures, V_i (for i=1, 2,…, N) are the control input voltages and D, S and B are the drain, source and substrate, respectively.

The drain current I_D of n-type N-input floating gate MOSFET in saturation region is given as [19, 20]:

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(W/L\right)\left(\frac{\sum_{i=1}^{N} C_i V_{iS}}{C_T} + \frac{C_{GD}}{C_T}V_{DS} + \frac{C_{GB}}{C_T}V_{BS} - V_T\right)^2 \quad (1)$$

Where μ_n is the electron mobility, C_{ox} is the gate-oxide capacitance per unit area, (W/L) is the aspect ratio, $\sum_{i=1}^{N} C_i$ is the sum of the N-input capacitances, V_{iS} is the applied input voltage at the i^{th} input gate with respect to source, V_{DS} is the drain-to-source voltage, V_{BS} is the substrate-to-source voltage, V_T is the threshold voltage, C_T $(= \sum_{i=1}^{N} C_i + C_{GD} + C_{GS} + C_{GB})$ is the total capacitance seen by the floating-gate, C_{GD} is the parasitic capacitance between floating-gate and drain, C_{GS} is the parasitic capacitance between floating-gate and source, and C_{GB} is the capacitance between floating-gate and substrate. Equation (1) can also be written as:

$$I_D = K_n\left(V_{FGS} - V_T\right)^2 \quad (2)$$

Where $K_n\left(=\frac{1}{2}\mu_n C_{ox}\left(W/L\right)\right)$ is the transconductance parameter and $V_{FGS}=\left(\frac{\sum_{i=1}^{N}C_i V_{iS}}{C_T}+\frac{C_{GD}}{C_T}V_{DS}+\frac{C_{GB}}{C_T}V_{BS}\right)$ is the voltage between floating gate and source of the floating gate MOSFET.

3 Proposed floating gate MOSFET based source degenerated OTA

The proposed floating gate MOSFET based source degenerated OTA is shown in Figure 2. The two differential pairs formed using two-input floating gate MOSFETs M_1, M_3 and M_2, M_4 are connected in series to reduce the distortion [21]. The transistors M_1-M_4 are biased in the saturation region. The differential pairs are also source degenerated by resistors R_1 and R_2. Two input voltages V_1 and V_2 are applied at one of the gate terminals of transistors M_1 and M_2, respectively. The proposed circuit is properly biased with current sources of same values connected to the source terminals of transistors M_1, M_2, M_3 and M_4.

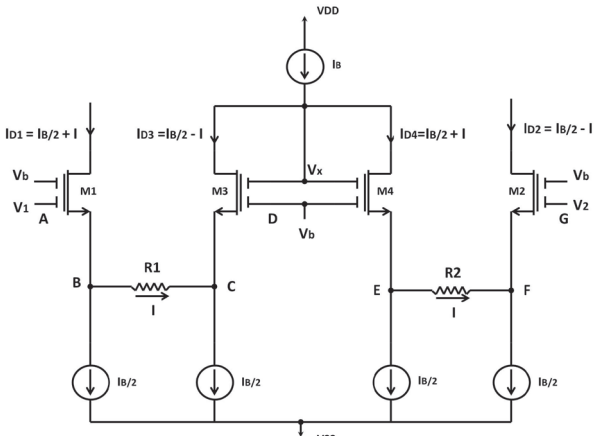

Figure 2: Proposed floating gate MOSFET based source degenerated OTA

Using (2), the drain currents I_{D1}, I_{D2}, I_{D3} and I_{D4} of transistors M_1, M_2, M_3 and M_4, respectively are given as

$$I_{D1}=\frac{I_B}{2}+I=K_n\left(V_{FGS1}-V_T\right)^2 \quad (3)$$

$$I_{D2}=\frac{I_B}{2}-I=K_n\left(V_{FGS2}-V_T\right)^2 \quad (4)$$

$$I_{D3}=\frac{I_B}{2}-I=K_n\left(V_{FGS3}-V_T\right)^2 \quad (5)$$

$$I_{D4}=\frac{I_B}{2}+I=K_n\left(V_{FGS4}-V_T\right)^2 \quad (6)$$

where I_B is the bias current, I is the current flowing through the resistors R_1 and R_2, K_n is the transconductance parameter, V_T is the threshold voltage, V_{FGS1} is the voltage between floating-gate and source of transistor M_1, V_{FGS2} is the voltage between floating-gate and source of transistor M_2, V_{FGS3} is the voltage between floating-gate and source of transistor M_3 and V_{FGS4} is the voltage between floating-gate and source of transistor M_4.

The voltages V_{FGS1}, V_{FGS2}, V_{FGS3}, and V_{FGS4} are given as

$$V_{FGS1}=\frac{C_1}{C_T}V_{1S}+\frac{C_2}{C_T}V_{bS}+\frac{C_{GD}}{C_T}V_{DS1}+\frac{C_{GB}}{C_T}V_{BS1} \quad (7)$$

$$V_{FGS2}=\frac{C_1}{C_T}V_{2S}+\frac{C_2}{C_T}V_{bS}+\frac{C_{GD}}{C_T}V_{DS2}+\frac{C_{GB}}{C_T}V_{BS2} \quad (8)$$

$$V_{FGS3}=\frac{C_1}{C_T}V_{xS}+\frac{C_2}{C_T}V_{bS}+\frac{C_{GD}}{C_T}V_{DS3}+\frac{C_{GB}}{C_T}V_{BS3} \quad (9)$$

$$V_{FGS4}=\frac{C_1}{C_T}V_{xS}+\frac{C_2}{C_T}V_{bS}+\frac{C_{GD}}{C_T}V_{DS4}+\frac{C_{GB}}{C_T}V_{BS4} \quad (10)$$

where C_1 & C_2 are input capacitances, V_{1S} & V_{2S} are the applied input voltages with respect to source at one of the gate terminals of transistors M_1 & M_2 respectively, V_X is the applied voltage with respect to source at one of the gate terminals of transistors M_3 & M_4, V_{bs} is DC bias voltage with respect to source, V_{DS1}, V_{DS2}, V_{DS3} & V_{DS4} are drain-to-source voltages of transistors M_1, M_2, M_3 & M_4 respectively, V_{BS1}, V_{BS2}, V_{BS3} &V_{BS4} are substrate-to-source voltages of transistors M_1, M_2, M_3 & M_4 respectively, and $C_T\left(=\sum_{i=1}^{N}C_i+C_{GD}+C_{GS}+C_{GB}\right)$ is the total capacitance seen by the floating-gate. Applying KVL in the loop ABCDEFG of Figure 2, the loop equation can be written as

$$V_1-V_{FGS1}-IR_1+V_{FGS3}-V_{FGS4}-IR_2+V_{FGS2}-V_2=0 \quad (11)$$

Substituting V_1-V_2= V_{in} (differential input voltage) and R_1=R_2=R, (11) is modified as

$$V_{in}-2IR=V_{FGS1}-V_{FGS3}+V_{FGS4}-V_{FGS2} \quad (12)$$

Using (7), (8), (9), and (10) in (12), the current (I) flowing through resisters R_1 and R_2 is given as

$$I = \frac{K_n\left(V_{in} - 2IR\right)}{2}\sqrt{\frac{I_B}{2K} - \frac{\left(V_{in} - 2IR\right)^2}{16}} \quad (13)$$

From Figure 2, the output current (I_{out}) of proposed OTA can be observed as

$$I_{out} = I_{D1} - I_{D2} = 2I \quad (14)$$

Using

(13) and (14), the output current (I_{out}) is given as

$$I_{out} = K_n\left(V_{in} - I_{out}R\right)\sqrt{\frac{I_B}{2K} - \frac{\left(V_{in} - I_{out}R\right)^2}{16}} \quad (15)$$

Equation (15) shows the relationship between output current (I_{out}) and differential input voltage (V_{in}) of proposed OTA. The transconductance of the proposed OTA can be calculated as

$$G_m = \frac{g_m}{1 + g_m R} \quad (16)$$

where $g_m = \sqrt{\frac{K_n I_B}{2}}$ is the transconductance of the transistors M_1-M_4. The nonlinear term in (15) depends on $V_{in} - I_{out}R$ rather than V_{in}. When $R >> 1/g_m$, the nonlinear term becomes zero and thereby high linearity can be achieved. The complete circuit of proposed OTA is shown in Figure 3, in which resistors R1 and R2 are replaced with the help of transistors M_{R1}-M_{R2} and M_{R3}-M_{R4}, respectively. These transistors (M_{R1}-M_{R4}) are operating in the ohmic region. The differential inputs V_1 and V_2 are applied at one of the input gates of floating-gate transistors M_1 and M_2 respectively and the output currents I_{out1} and I_{out2} are also taken out differentially, which allows the proposed OTA to be categorized as fully differential OTA. The fully differential structure of the OTA helps for better linearity as the even harmonics are cancelled out and only odd harmonics are left to contribute in total harmonic distortion. The common-mode voltage variations at the output nodes due to the fully differential structure can be stabilized by Common-Mode Feedback (CMFB) circuits. But the inclusion of CMFB circuits may results in stability issues as well as increases the complexity and power consumption. A current source formed by PMOS transistor M_5 is used for biasing purpose. Three current mirrors are formed using NMOS transistors M_6–M_{10}, M_{17}–M_{18}, M_{19}–M_{20} and two current mirrors are formed using PMOS transistors M_{11} – M_{13}, M_{14} – M_{16}. These current mirrors are used to copy the currents at the appropriate nodes of the circuit. The remaining transistors are used to transfer the currents at the appropriate nodes.

4 Applications of proposed OTA

The proposed OTA is used to develop some of the important analog building blocks such as active inductor, tunable resistors and filters.

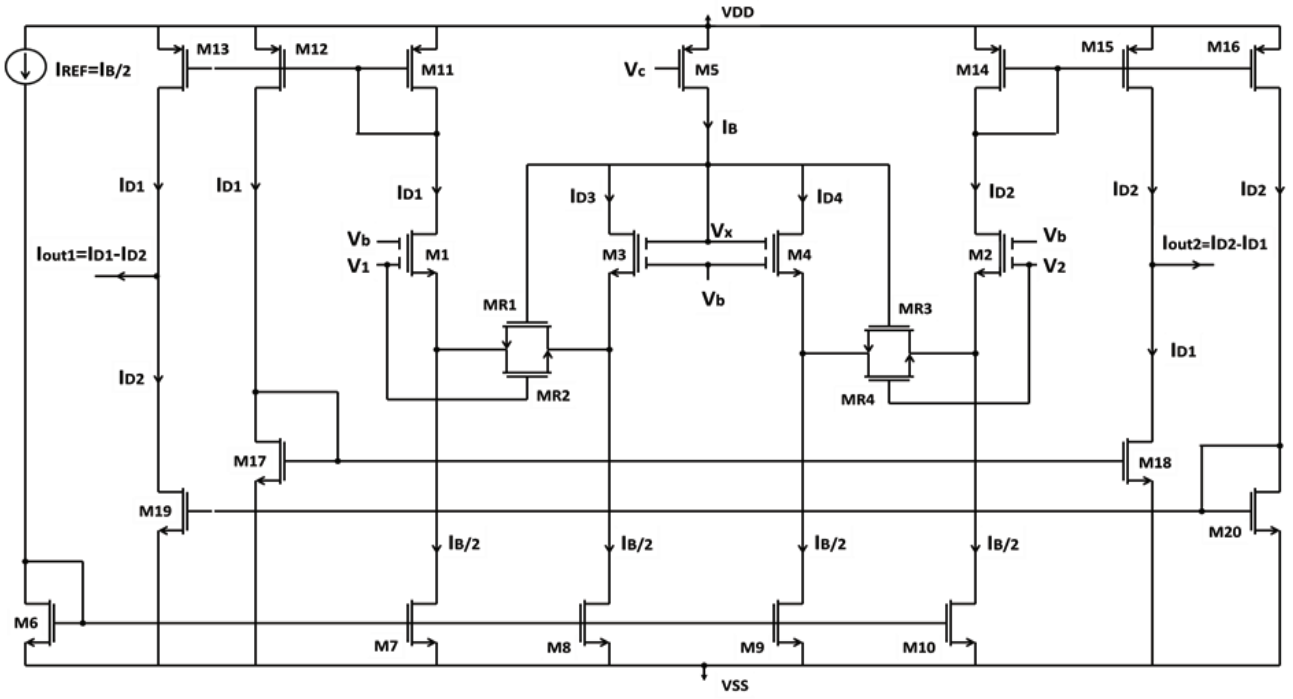

Figure 3: Complete circuit diagram of proposed OTA

4.1 Active inductor

The proposed active inductor is shown in Figure 4. The inductor has been developed using a capacitor C and two proposed OTA.

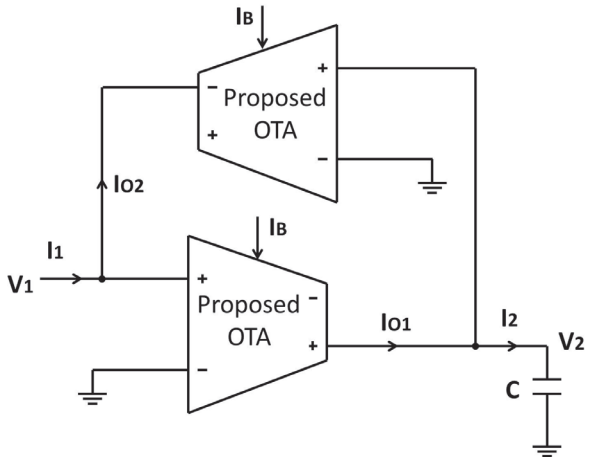

Figure 4: Proposed active inductor

In Figure 4, the current (I_2) flowing through capacitor C is given as

$$I_2 = I_{O1} = G_m V_1 \tag{17}$$

where G_m is the transconductance of the proposed OTA and V_1 is the input voltage.

The input current (I_1) can be written as

$$I_1 = I_{O2} = G_m V_2 = G_m \frac{I_2}{sC}; \tag{18}$$

where V_2 is the voltage across capacitor C.

Using (17) and (18), the current (I_1) is modified as

$$I_1 = \frac{V_1}{s\left(C/G_m^2\right)} = \frac{V_1}{sL_{eq}} \text{ ; where } L_{eq} = C/G_m^2 . \tag{19}$$

From (19), it can be seen that the value of equivalent inductance depends on the transconductance G_m of the proposed OTA.

4.2 Tunable resistors

Tunable resistors have a significant role in the analog circuit design because they can be employed as tuning elements in various analog circuit applications. The tunable floating and grounded resistors based on proposed OTA are shown in Figures 5 (a) and (b), respectively.

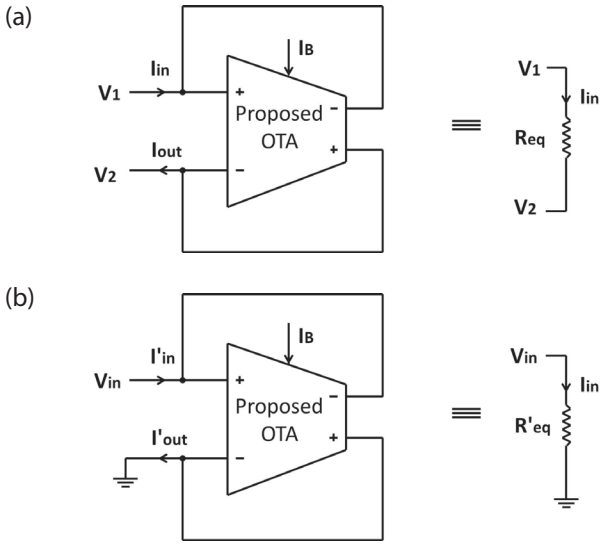

Figure 5: Proposed tunable resistors (a) floating resistor and (b) grounded resistor

In Figure 5 (a), the input current (I_{in}) is given as

$$I_{in} = I_{out} = G_m \left(V_1 - V_2\right) \tag{20}$$

where V_1 and V_2 are the input voltages and G_m is the transconductance of proposed OTA.

From (20), the equivalent resistance (R_{Feq}) is given as

$$R_{Feq} = \frac{\left(V_1 - V_2\right)}{I_{in}} = \frac{1}{G_m} ; \tag{21}$$

where

$$G_m = \frac{I_{in}}{\left(V_1 - V_2\right)}$$

The grounded resistor shown in Fig 5(b), it is observed that $V_2 = 0$, and $V_1 = V_{in}$. Substituting the values of V_1 and V_2 in (21), the equivalent resistance (R_{eq}) is given as

$$R_{eq} = \frac{V_{in}}{I_{in}} = \frac{1}{G_m^{'}} ; \text{ where } G_m^{'} = \frac{I_{in}}{V_{in}} \tag{22}$$

From (21) and (22), it can be seen that the equivalent resistances R_{Feq} and R_{eq} of floating and grounded resistors, respectively are varied with the transconductance.

4.3 Tunable filters

The tunable low-pass, high-pass and band-pass filters based on proposed OTA are presented.

4.3.1 Low-pass filters

The low-pass filters based on proposed OTA is shown in Figure 6.

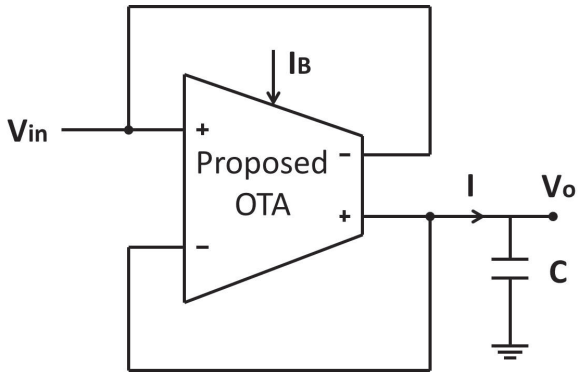

Figure 6: Proposed low-pass filter

In the figure, the current (I) flowing through capacitor C and the output voltage (V_0) are given as

$$I = G_m\left(V_{in} - V_0\right) \tag{23}$$

$$V_0 = I/sC \tag{24}$$

where G_m is the transconductance of proposed OTA. Using (23) and (24), the transfer function of first order low-pass filter can be written as

$$\frac{V_o}{V_{in}} = \frac{G_m}{G_m + sC} \tag{25}$$

4.3.2 High-pass filters

The high-pass filter based on proposed OTA is shown in Figure 7.

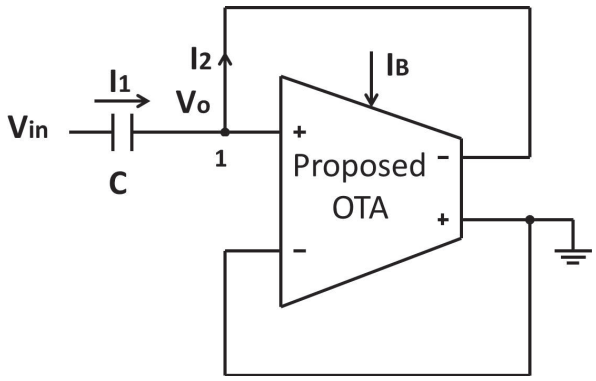

Figure 7: Proposed high-pass filter

In the figure, applying KCL at node 1, we get

$$\left(V_{in} - V_0\right)sC - G_m V_0 = 0 \tag{26}$$

where G_m is the transconductance of proposed OTA. From (26), the transfer function of first order high-pass filter can be written as

$$\frac{V_o}{V_{in}} = \frac{sC}{G_m + sC} \tag{27}$$

4.3.3 Proposed band-pass filters

The band-pass filter based on proposed OTA is shown in Figure 8. In the figure, applying KCL at nodes 1 and 2, we get

$$\left(V_{in} - V_1\right)sC_1 = G_m V_1 + \left(V_1 - V_0\right)G_m \tag{28}$$

$$sC_2 V_0 = G_m\left(V_1 - V_0\right) \tag{29}$$

Using (28) and (29), the transfer function of first order band-pass filter can be written as

$$\frac{V_o}{V_{in}} = \frac{sC_1 G_m}{s^2 C_1 C_2 + sG_m\left(C_1 + 2C_2\right) + G_m^2} \tag{30}$$

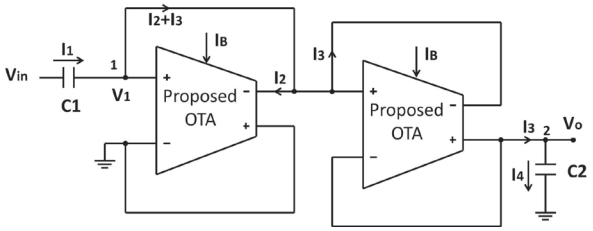

Figure 8: Proposed band-pass filter

5 Simulation results

In this Section, the simulation results of proposed OTA and its applications such as inductor, tunable resistors and filters are presented. The workability of all of the proposed circuits have been verified by Cadence EDA tool using typical parameters of UMC 0.18µm CMOS technology.

5.1 Simulation results of floating-gate MOSFET based source degenerated OTA

The DC transfer characteristic of the proposed OTA (Figure 3) is shown in Figure 9. From the plot, it can be seen that the output current of the OTA varies linearly with respect to the input differential voltage (V_{in}) and the range of the input differential voltage for linear operation is -0.6V to +0.6V.

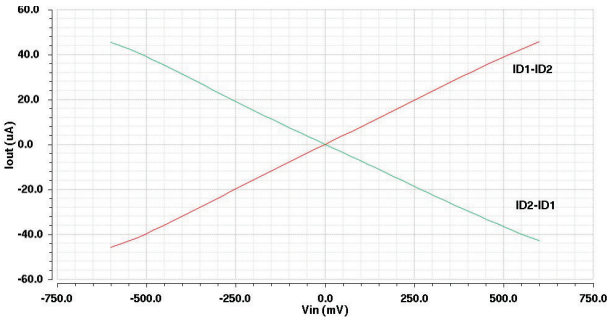

Figure 9: DC transfer characteristic of proposed OTA

The frequency response of the proposed OTA is shown in Figure 10. From figure, the transconductance is observed as -82.41dB (75.5µA/V) and the bandwidth is 1.47GHz for capacitive load of 1pF. Also, it is evident that the proposed OTA is stable as the gain is negative in decibels (dB) when phase angle is -180^0. The bandwidth gradually decreases for the larger values of capacitive loads.

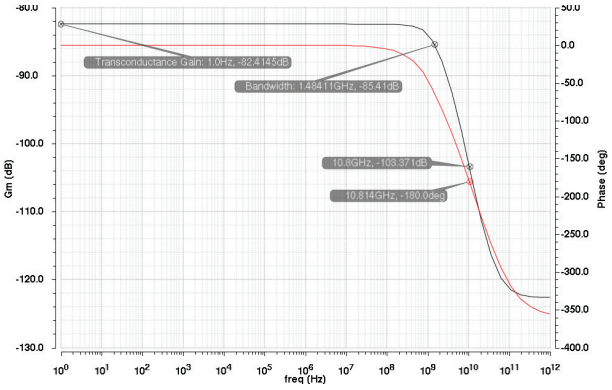

Figure 10: Frequency response of proposed OTA

The variation of the transconductance with respect to bias current (I_B), ranging from 120µA to 200µA with the increment of 20µA is plotted in Figure 11 and the corresponding values of transconductance are obtained as 70.08 µA/V, 72.78 µA/V, 75.54 µA/V, 80.18 µA/V and 87.85 µA/V, respectively.

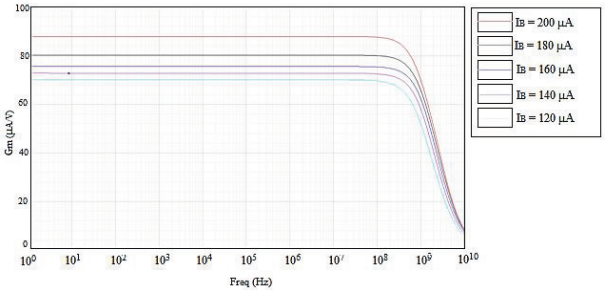

Figure 11: Variation of transconductance with respect to bias current (I_B)

For the distortion analysis of the proposed OTA, the sinusoidal differential input voltage of 5MHz with peak-to-peak amplitude ranging from 0.1V to 1.2V is employed.

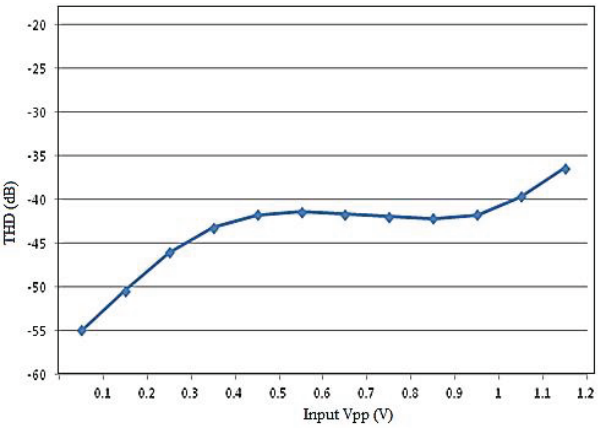

Figure 12: Total Harmonic Distortion plot of proposed OTA

Table 1. Comparison of proposed OTA with other OTAs available in literature

References	Power Supply (V)	Gm (µA/V)	Bandwidth (MHz)	Input Range (Vpp)	Power Consumption (mW)	THD (db) @Frequency (MHz) @Input (Vpp)
[22]	±0.9	22	-	1	0.057	-
[23]	1.5	40	65	0.95	0.126	-110@0.001@0.35
[24]	0.8	28.4	-	0.8	0.0312	-40@1@0.8
[25]	1.5	155	40	0.6	0.042	-55@5@0.1
[26]	2	266	175	0.6	0.160	-48@0.001@0.4
[27]	±1.5	850	780	0.4	20	-
[28]	±1.5	46	-	3	2.6	-60@0.1@3
[29]	0.5	245	10	0.5	0.11	-45@5@0.4
[30]	0.7	-	-	1.4	0.010	-35@5@0.4
Proposed work	±0.6	75.5	1472	1.2	0.56	-42@5@1

Figure 12 shows the total harmonic distortion (THD) obtained in the output waveform as a function of the peak-to-peak input voltage and it is observed that for differential input voltage (V_{in}) ranging from 0.1V to 1V, distortion is still low (≤ -42dB). The comparison between the performance parameters of proposed highly linear floating gate MOSFET based source degenerated OTA with the existing OTAs available in literature is listed in Table 1. From the table it is observed that the proposed circuit has rail-to-rail input voltage range with low power supply and high bandwidth.

5.3 Simulation results of active inductor

For the simulated inductances the value of the capacitance (C) is chosen as 1pF. The values of equivalent inductance (L_{eq}) are obtained as 0.129 mH, 0.155mH, 0.175 mH, 0.188 mH and 0.203 mH for different values of transconductance (Gm) as 87.85 µA/V, 80.18 µA/V, 75.54 µA/V, 72.78 µA/V and 70.08 µA/V, respectively.

5.4 Simulation results of proposed tunable resistors

Figure 13 shows the I-V characteristics of the floating resistor (Figure 5(a)) operating at supply voltages of ±0.6V. The current I_{in} is plotted for various values of V_2 ranging from -0.3V to 0.3V with the increment of 0.15V, while V_1 is varied from -0.3V to 0.3V. From the plot, it can be seen that the proposed circuit behaves as linear floating resistor over the differential input voltage range from -0.3V to 0.3V. The values of the equivalent resistance (R_{Feq}) are obtained as 9.21 KΩ, 8.84 KΩ, 8.69 KΩ, 8.43 KΩ and 8.21 KΩ for V_2 equals to -0.30V, -0.15V, 0V, 0.15V and 0.30V, respectively. Also, the grounded resistor is realized by connecting the second input voltage source (V_2) to the ground. The values of the equivalent grounded resistor (R_{eq}) for different values of applied bias current (I_B) as 120 µA , 140 µA, 160 µA , 180 µA and 200 µA are obtained as 10.82 KΩ , 9.5 KΩ, 8.69 KΩ, 7.75 KΩ and 7.19 KΩ, respectively.

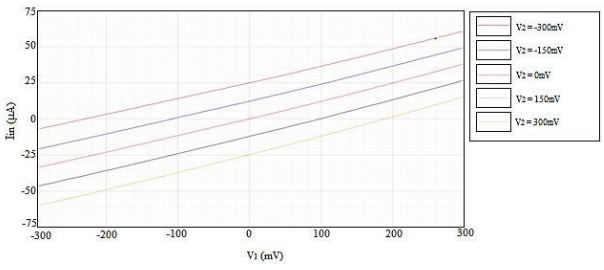

Figure 13: DC characteristic of proposed floating resistor

5.5 Simulation results of proposed filters

The proposed OTA is used to develop first order low pass, high pass and band pass filters. The frequency response of first order low pass, high pass and band pass filters for various values of bias current ranging from 120µA to 200µA with the increment of 20µA are shown in Figures 14 (a), (b) and (c), respectively.

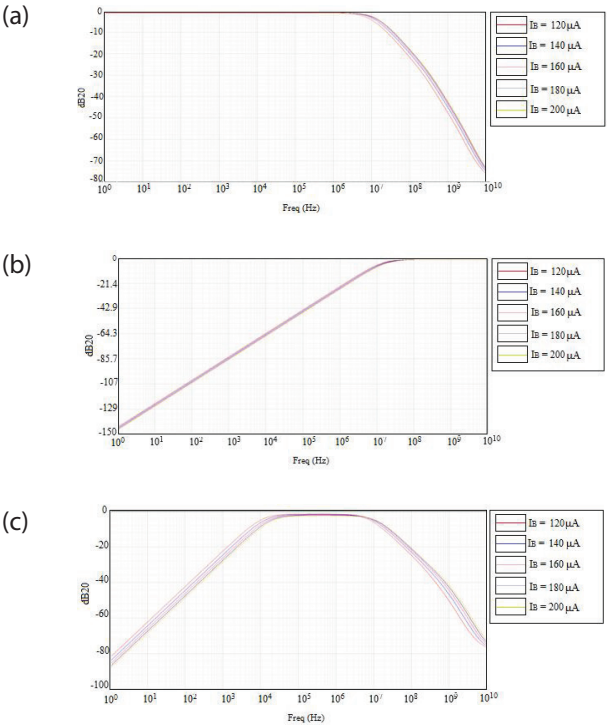

Figure 14: Frequency response of proposed first order: (a) low pass, (b) high pass and (c) band pass filters

6 Conclusions

A highly linear floating gate MOSFET based source degenerated OTA is developed. The proposed OTA utilizes floating gate MOSFETs to reduce the power supply requirement of the circuit and source degeneration technique is used to increase the linearity of the designed OTA. The proposed OTA operates at ±0.6V power supply. The circuit has rail-to-rail input voltage range with transconductance gain of 75.5µA/V. The 3db bandwidth of the designed OTA is 1.47GHz. The proposed OTA has wide input voltage differential range, low power supply requirement and high bandwidth.

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