Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials Vol. 48, No. 2(2018), 115 – 120

# The Design of Broadband LNA with Active Biasing based on Negative Technique

Gang Wang, Jiarui Liu, Shiyi Xu, Jiongjiong Mo, Zhiyu Wang, and Faxin Yu

School of Aeronautics and Astronautics, Zhejiang University, Hangzhou, China

**Abstract:** In this paper, we present a broadband LNA based on an improved negative feedback design. With the adjustment of the negative feedback inside the chip, the LNA achieves a planarized gain and an optimized operating bandwidth from 0.2 GHz to 4 GHz. To guarantee the good performance stability under severe environments, an active biasing is used inside the chip. As a result, effective compensations for the fluctuation of the supply voltage and the temperature variation are achieved. The LNA chip uses GaAs pHEMT at 0.25-µm technology node and SIP package technique. This broadband LNA shows good performances, including gain of about 15 dB, gain flatness of less than 1dB, and noise figure of less than 1.5 dB. The packaged size of this broadband LNA is 3 mmX3 mmX1 mm.

Keywords: feedback network; broadband LNA; active biasing; SIP package

# Načrtovanje širokopasovnega LNA z aktivnim napajanjem na osnovi negativne tehnike

**Izvleček:** Članek predstavlja širokopasovni LNA na osnovi izboljšane negativne povratne zanke. Nastavljiva negativna zanka v čipu omogoča LNA doseganje ojačenja in optimalne pasovne širine med 0.2 in 4 GHz. Za doseganje dobrih lastnosti v neugodnem okolju je uporabljeno aktivno napajanje v čipu. Doseženo je efektivna kompenzacija fluktuacij napajalne napetosti in temperature. LNA čip uporablja GaAs pHEMT v 0.25 µm tehnologiji in SIP ohišje. LNA izkazuje dobre lastnosti vključno z ojačenjem 15 dB, stabilnostjo ojačenja pod 1 dB in šumom pod 1.5 dB. Velikost ohišja je 3 mmX3 mmX1 mm.

Ključne besede: povratno omrežje; širokopasovni LNA; aktivno napajanje; SIP ohišje

\* Corresponding Author's e-mail: jrliu@zju.edu.cn

# 1 Introduction

With the rapid evolution of wide-bandwidth technology, more attentions are drawn by the design of wideband receivers which are able to cover a wide range of frequency standards [1].

The main difficulty in designing a wideband LNA is to achieve high gain, low noise figure and excellent linearity simultaneously. There were various architectures reported in the literature to achieve wideband LNAs, including distributed LNAs, balanced LNAs, common gate LNAs and feedback LNAs. The first three share features of small input and output reflection coefficient while they have disadvantages such as low gain and high power dissipation [2, 3]. The feedback is featured for tradeoff among several performance specifications, which is popular in wideband LNA designs. There are many researches which have designed wideband LNAs utilizing feedback technology. However, only LNA die is considered in their works, and no parasitics of bonding wire and package are taken into account. Biasing circuit also has influence on the performance of LNA. The current mirror with temperature compensation is the most popular biasing, but it does not take the fluctuation of power supply into consideration [4].

In this paper, we report a broadband LNA with an active biasing based on an improved negative feedback. In order to extend the bandwidth, a feedback unit is used between the drain and gate, and a RC cell is added at the source. The influence of external parasitics is introduced by applying equivalent circuit elements of bonding wire and ESD circuits. The stable performances under different severe conditions are achieved via an active biasing inside LNA die, which can compensate the fluctuation of environmental temperature and the supply voltage variation.

The LNA described in this paper exhibits a broad bandwidth of more than 20 octaves, from 0.2 GHz to 4 GHz, covering several communication standards like GSM, GPS, TD-SCDMA, WCDMA, and Bluetooth.

## 2 Design principle and approach

As the circuit diagram showed in Fig. 1(a), the wideband LNA in this paper is composed of Cascode amplifier, feedback circuit, active biasing circuit, ESD circuit, source degeneration inductance, input and output matching networks. We choose the Cascode topology for priority to eliminate miller effect and to increase reverse isolation [5]. A load capacitor Cg is added at the gate of M2 to improve power gain. And a resistor Rg is added in series in order to minimize the deterioration of stability due to the introduction of Cg. The equivalent element of bonding wires (b1, b2, b3), pads(p1, p2, p3) and the ESD circuits are also considered in our simulation.



**Figure 1:** (a) The electric circuit diagram of LNA Amplifier (b) A novel active biasing circuit

The active biasing circuit of the presented LNA is shown in Fig. 1(b). Q2 and Q5 work as switching transistor. When VEN is set at low voltage, the switching transistor is in off-mode, and only an infinitesimal current exists in biasing circuit. While in on-mode when VEN is set at high voltage, DC bias is supplied for the operation of LNA. Q6 works as diode for voltage stabilization.

E-mode transistor Q1 and Q3, resistor R1, R2 and R3 form the temperature compensation circuit. When the ambient temperature decreases, the drain current of Q1 increases. As a result, the potential at point A decreases. Thereby, the gate-to-source voltage and the source current of Q3 decrease. And the voltages on R3 which is also the gate-to-source voltage of Q1 would decrease. This results in the restriction of the drain current growth of Q1, which benefits the performance stability of the LNA. Similar temperature compensation phenomenon can be achieved when ambient temperature increases.

The temperature compensation circuit also works as a supply voltage regulation circuit. When Vbb decreases, potential would decrease at point A and B. Therefore the gate-to-source voltage of Q3 would decrease, which as we mentioned above, results in a decreasing of gate-to-source voltage of Q1.Then the drain current of Q1 would increase, which restricts the decrease of potentials at point A and B.

In conclusion, the active biasing circuit can compensate the temperature and voltage fluctuations effectively. Therefore, a stable output voltage can be achieved and stable performance at different severe conditions is guaranteed.

According to the feedback circuit of LNA, traditional negative feedback circuit is composed of a single resistor between drain and gate, which couples part of signal from output to input, and enhances the bandwidth along with the sacrifice of gain [6, 7].

In our design, we exhibit an improved negative feedback to further extend the bandwidth and improve the high-frequency performance of the LNA. As shown in Fig. 2(a), a capacitor Cf is introduced for the isolation of DC signal. And an inductor Ld is added at drain for the compensation of the capacitive portion of output impedance at high frequency, which extends the operating frequency range.

For simplification, we analyze the contribution of Zd and Zp, respectively. The simplified equivalent circuits are shown in Fig. 2(b) and 2(c).







**Figure 2:** (a) Improved negative feedback amplifier (b) The equivalent circuit of LNA with  $L_d$  (c) The equivalent circuit of LNA with  $L_d$  and *RC* cell

From Fig. 2(b), we know

$$V_{in} = V_{out} \frac{Z_f}{Z_{gs} / / Z_s + Z_f}$$
(1)

$$V_{out} = (I_{out} - i_{ds})[Z_s // Z_{gs} + Z_f]$$
<sup>(2)</sup>

$$R_{out} = \frac{V_{out}}{I_{out}} = \frac{(Z_{ds} + Z_d)(Z_{gs} / / Z_s + Z_f)}{g_m Z_f Z_{ds} + Z_{ds} + Z_d}$$
(3)

Where

(a)

$$Z_{ds} = \frac{1}{sC_{ds}} / R_{ds} \tag{4}$$

The inductor Ld (Zd in equation (3)) is introduced to effectively eliminate the capacitive parts of load resistance, and as a result to achieve a broad bandwidth, as shown in curve B in Fig. 3.

As shown in Fig. 2(c), Zp at source consists of an inductor Lp and a RC parallel cell. The degeneration inductor Lp is introduced to reduce the difference between optimum impedances of NFmin and Gainmax, and to improve the LNA performance on NF and Gain simultaneously. As for the RC cell, the capacitor Cp behaves as open at low frequency and gain attenuation exists due to the resistor Rp. While at high frequency, the impedance of Cp is close to short and no signal flows through Rp. Therefore the gain flatness of LNA is improved.

The EM simulation of the presented LNA with novel negative feedback circuit is carried out using ADS. The gain performance comparison with traditional negative-feedback LNA as a function of frequency is shown in Fig. 3. Compared with curve A, operating from 0.2 GHz to 2.1 GHz, the bandwidth of curve B is extended pronouncedly, covering 0.2 GHz to 3.6 GHz, due to the introduction of Ld. From the comparison between curve B and C, the latter attains more ideal gain flatness covering 0.2 GHz to 4 GHz due to the gain attenuation at low frequency by the introduction of paralleled RC cell at source.



**Figure 3:** The Gain characteristic of LNA with various feedbacks, in which A: traditional feedback, B: feedback with additional  $L_{d}$ , C: presented novel feedback

#### 3 Implementation and measurements

The proposed LNA is constructed by an LNA die and several lumped elements including the output impedance matching inductor and capacitor, a decoupling capacitor and a DC blocking capacitor. SIP technique is used for integration. Based on the tradeoff between gain and output power linearity, we use a pair of 16  $\times$  40  $\mu m$  GaAs pHEMT with Cascode configuration on the LNA die.

The broadband LNA die is fabricated by 0.25- $\mu m$  GaAs pHEMT process with the size of 0.8 mm  $\times$  0.75 mm, including all RF and DC pads, as shown in Fig. 4(a). In the design of LNA layout, ESD circuits are introduced at each DC supply pads for electrostatic protection.

The substrate of the SIP package consists of 4 metal layers. On the bottom metal layer there locates the LGA (Land Grid Array) pads, which have smaller parasites compared to traditional pins [8]. The second and third metal layers are patterned for biasing DC signal. The top layer is for RF signal. The total size of substrate is 3 mm  $\times$  3 mm.



Figure 4: (a) Layout of LNA die (b) Packaged LNA

In order to minimize the size of the LNA chip, we use an inductor as the input matching element on the LNA die and put the input block capacitance, the output matching network which consists of a low-pass LC cell, an inductor Lo, and a capacitor Co on the package substrate.

When packaging is finished, we measure the LNA in detail under the bias condition Vdd=3.3 V and Vbb=3.3 V at room temperature. Fig. 5(a) shows the measured S-parameters. From 0.2 GHz to 4 GHz, LNA shows no-

less-than 15 dB small signal gain, and less than -10 dB reflection loss at both input and output. The gain flatness within operating frequency band is about 1.2 dB. Fig. 5(b) shows the measured NF, P-1dB and IIP3. The NF of the LNA is less than 1.6 dB, while P-1dB is 17 dBm. The OIP3 is 19 dBm, from which we deduct the gain with 15 dB, therefore the IIP3 is 4 dBm.





**Figure 5:** (a) The S-parameter of LNA. (b) The NF,  $P_{-1dB}$  and OIP3 of LNA.

To explore the advantages of the biasing circuit inside the LNA die, we measure the S-parameters and the NF at different temperature conditions (-40°C, 25°C, 85°C), as shown in Fig. 6(a) and 6(b). With the variation of temperature from -40°C to 85°C, the fluctuation of gain and NF are both within ±0.4 dB, which validates the temperature compensation of the active bias.

The comparison of published measurement results of wideband LNAs and this work is shown in Table 1. The bandwidth of this work is up to 20 octaves while maintaining a superior gain flatness, a low NF and a good linearity.

## 4 Conclusion

This paper presents a broadband LNA based on the improved negative feedback design. GaAs pHEMT at 0.25-

Ref	Device Tech	Freq (GHz)	G (dB)	NF(dB)	ΔG (dB)	VDC (V)	P-1dB (dBm)	IIP3 (dBm)	Pdiss (mW)
[9]	0.5 μm GaAs pHEMT	2.5~5	17	2.4~3	1.6	1.5	-2	2.3	33
[10]	0.18 μm CMOS	0.9~1.1	10.7	1.3	None	2.5	18.4	3	50
[11]	0.18 μm CMOS	2.5~6.8	11.5	4.2	4	1.8	None	None	8.1
This Work	0.25 μm GaAs pHEMT	0.2~4	15	1.6	1.2	3.3	17	4	33

Table 1: Performance comparison of wideband LNA



**Figure 6:** (a) The S-parameter of LNA. (b) The NF,  $P_{-1dB}$  and OIP3 of LNA.

μm technology node and SIP package technique are applied. The LNA consists of a pair of 16 × 40 μm GaAs pHEMTs with Cascode configuration and a novel negative feedback circuit between drain and gate which remarkably extends the operation bandwidth. An active biasing technique is applied to effectively compensate the fluctuation of the supply voltage and the temperature variation. The designed LNA has achieved a broad bandwidth of up to 20 octaves from 0.2 GHz to 4 GHz while maintaining a gain flatness of less than 1.2 dB. A low NF of less than 1.6 dB and a good linearity are also obtained. The presented LNA can be applied in severe conditions to cover several communication standards like GSM, GPS, TD-SCDMA, WCDMA, and Bluetooth.

# 5 Acknowledgment

This work was supported by the National Natural Science Foundation of China under Grant 61604128.

## 6 References

- 1. 2. Cho, Kang Fu, and S. Wang, "A 0.4~5.3GHz wideband LNA using resistive feedback topology," *IEEE Mtt-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization* (2016) 1.
- P. Bousseaud, M. A. Khan and R. Negra, "Inductorless wideband LNA with improved input Matching using feedforward technique," 2016 46th European Microwave Conference (EUMC), pp. 1027-1030, 2016.
- 4. Wang, Minghua, et al. "A power reduction technique for wideband common gate low noise amplifers." *IEEE, International Midwest Symposium on Circuits and Systems IEEE*, pp. 969-972, 2014.
- 5. Weinberg, Elena K., and M. R. Stan. "SymmTop: A Symmetric Circuit Topology for Ultra Low Power Wide Temperature-Range Applications." VIsi IEEE:585-590, 2015.
- 6. S. N. I. S. Zulkepli and T. Z. A. Zulkifli, "Asymmetric T-coil, resistive feedback cascode low noise amplifier for ultra wideband receiver," 2015 IEEE International Circuit and Symposium (ICSyS), PP. 11-16, 2015.
- 7. A. P. Kulkarni and S. Ananthakrishnan, "1 to 3 GHz Wideband Low Noise Amplifier design," *Computers and Devices for Communication (CODEC), 2012 5th International Conference*, pp. 1-4, 2012.

- 8. Z. Zhang, A. Dinh and L. Chen, "A 2 GHz bandwidth LNA using resistive feedback with added inductor," *2012 IEEE International Conference on Ultra-Wideband*, pp. 375-378, 2012.
- 9. J. Y. Jeon, S. G. Kim, Y. S. Eo and S. H. Jung, "A Transformer feedback wideband CMOS LNA for UWB application," *2015 Asia-Pacific Microwave conference (APMC)*, pp. 1-3, 2015.
- 10. Y. Peng, K. Lu, W. Sui, et al, "A low power 2.5-5GHz low-noise amplifier using 0.5μm GaAs pHEMT technology," *Journal of Semiconductors*, 33(10): vol. 33, no. 10, 2012.
- 11. B.-K. Kim, D. Im, J. Choi , and K. Lee, "A 1 GHz 1.3 dB NF + 13 dBm output P1dB SOI CMOS low noise amplifier for SAW-less receiver ,"*in Proc. IEEE Ra-dio Freq. Integr. Circuit Symp. Dig. Montral, QC*, pp. 9-12, Jun.2012.

Arrived: 24. 02. 2018 Accepted: 22. 05. 2018