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Nano CMOS Charge Pump for Readerless RFID PLL

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Abstract: Readerless RFID has become more significant for reliable wireless communication. The Phase Locked Loop (PLL) is among the most crucial functional block in the Readerless RFID where the PLL performance greatly depends on the Charge Pump (CP). Conventional CP circuits suffer from current mismatching characteristics which generate phase offset and spurs in the PLL output signals. To overcome these problems, the CP current mismatch has to be minimized. An enhanced CP circuit with zero current mismatch is presented in this article adopting an ideal current mirror technique and an additional inverter to provide a rail-to-rail voltage. The post-layout simulation shows that the proposed CP maintains the steady current over a wide range of output voltage from 0.1-1.8 V consuming the substantially lower power of 0.178 µW. The CP circuit is designed in 130 nm CMOS process that operates at 1.8 V, and the core occupies 17 x 59.5 µm2. The proposed CP will be a good solution for low voltage, high-frequency PLL structure which suffers from poor performance.

Keywords: Charge pump; CMOS; Current mismatch; PLL; RFID

Nano CMOS črpalka energije za RFID PLL brez čitalca

Izvleček: RFID brez čitalca so postali pomembni za zanesljivo brezžično komunikacijo. Eden izmed kritičnih funkcijskih blokov RFID brez čitalca je, od črpalke energije (CP) odvisna, fazno sklenjena zanka (PLL). Konvencionalni CP trpijo z neuravnoteženo tokovno karakteristiko, ki vpliva na izhodni signal PLL. V izogib tem problemom je potrebno minimizirati CP. Članek opisuje izboljšan CP z ničelno tokovno neuravnoteženostjo z uporabo tehnike idealnega zrcaljenja toka in dodatnega inverterja za zagotavljanje napajanja. Simulacije nakazujejo da CP vzdržuje konstantni tok čez široko območje napajalne napetosti od 0.1-1.8 V in porabijo izredno malo moč 0.178 µW. Vezje je zasnovano v 130 nm CMOS tehnologiji pri napajalni napetosti 1.8 V. Velikost jedra je 17.0 x 59.5 µm2. Predlagana rešitev je dobra za uporabo v nizkonapetostnihvisokofrekvenčnih PLL strukturah z nizkim učinkom.

Ključne besede: črpaka energije; CMOS; tokovno neujemanje; PLL; RFID

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1 Introduction

At present, Readerless RFID systems are experiencing rapid growth because of the advancement of the wireless communication system. RFID is an identification system, where data is transferred/received via radio frequency among antenna, reader, and transponder. In an RFID system, electronic product code which is also known as the identification code is attached to

an object for tracking. A frequency synthesizer (FS) is a feedback system that produces one or more frequencies from a single or several frequency sources. Charge pump based PLL (CPPLL) is broadly used in a wireless communication systems for frequency synthesis; especially in radio, telecommunications and other electronic applications due to its simple feedback system [1, 2]. CPPLL is preferred because of low bias current [3, 4], low static phase offset [5-7] and large system gain [8, 9]. Furthermore, it performs the key role to ensure the stability of frequency synthesis [10, 11]. The PLL is generally composed of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO) and a frequency divider as depicted in Figure 1. Among all the functional blocks, CP is the most crucial block which significantly contributes to boosting the PLL's overall performance and stability. It changes the digital signal originating from PFD into an analog signal which in turn controls the VCO frequency [12]. The output voltage of the charge pump must be fixed when the PLL goes into a locked state at a specific frequency. Any change of that voltage results in frequency offset. [5, 13, 14]. In this regard, it is imperative to design a charge pump circuit that can generate a steady output current and can produce a superbly matched current with zero error in CPPLL.

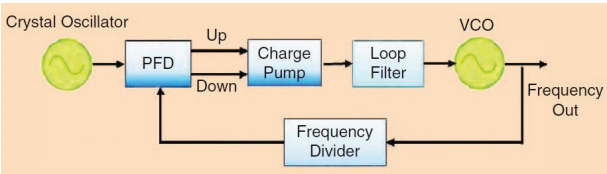

Figure 1: A Basic Block Diagram of CPPLL [4]

Charge pump (CP) is the subsequent stage to the PFD, i.e., the output (UP and DWN) signals of the PFD are fed to the CP circuit. The key principle of a charge pump is to translate the logic states of the PFD into suitable analog signals to control the voltage-controlled oscillator (VCO) through a loop filter. Fundamentally, the charge pump is made up of current sources and switches as shown in Figure 2. The output currents from the CP is usually filtered by a low pass filter (LPF) that converts the charge pump current to an equivalent control voltage for the VCO.

The conventional CP circuit consists of a charge and a discharge digital output current source, ICH and IDIS respectively described in Figure 2. A couple of transistor-based switches control both ICH and IDIS of the PFD. The two switches drive the loop filters and convert the output signals of the PFD to an analog voltage signal, Vcntrl, to tune the frequency of the VCO. The basic CP circuit suffers from many disadvantages, and as a consequence, several charge pump architectures have

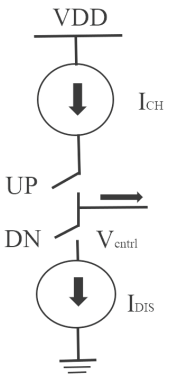

Figure 2: The basic concept of a charge pump circuit.

been reported with their pros and cons in the literature [14].

The imperfection of a CP can be estimated by the current mismatch, timing mismatch, power consumption, and charge sharing. But the current mismatch is the most vital parameter which leads the PLL performance. The current mismatch implies the magnitude dissimilarity between charging and discharging current which is a crucial concern for the CP design [8, 15]. Figure 3 represents the charging and discharging time diagram of a charge pump circuit.

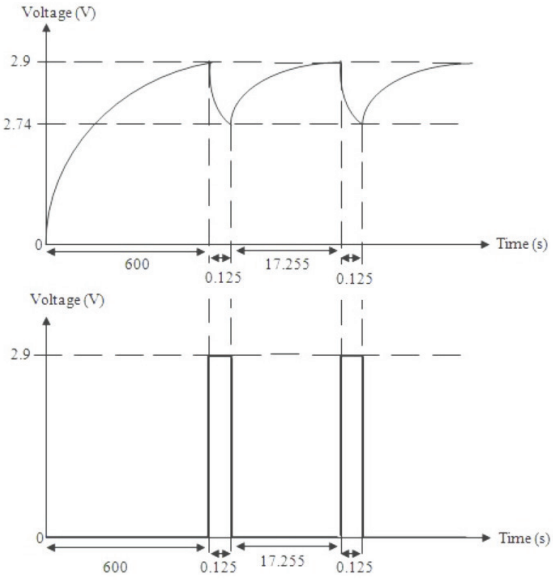

Figure 3: Charging and discharging time diagram of a charge pump circuit

The issues of current mismatch and leakage current introduce the phase error problem and produce PLL's reference spur [16, 17]. The current mismatch and leakage can be characterized as:

$$\Delta\emptyset = 2\pi \left(\Delta\emptyset_{timing} + \Delta\emptyset_{mismatch} + \Delta\emptyset_{leakage}\right) \quad (1)$$

Where, ΔØ, ΔØtiming, ΔØmismatch, and ΔØleakage, are the phase error, timing mismatch, current mismatch and leakage current of the CP circuit, respectively. Equation 1 shows that the current mismatch is directly associated with phase error and PLL's reference spur which is otherwise called dynamic jitter [7]. The measure of the reference spurs Pr can be defined by [18]

$$Pr = 20\log\left(\frac{\Delta Øf_{\mathrm{BW}}}{\sqrt{2f_{REF}}}\right) - 20\log\left(\frac{f_{REF}}{f_{PL}}\right)[dBc] \qquad (2)$$

and the loop bandwidth, f_{BW} is given by

$$f_{BW} = I_{CP}K_{VCO}R/(2\pi N) \qquad (3)$$

Where, Pr is the PLL reference spur, f_{REF} refer the reference frequency of the phase frequency detector (PFD), f_{BW} stands for the loop bandwidth, ΔØ is the phase error, and f_{PL} is the Loop filter's pole frequency. I_{CP} stands for the CP current flow, K_{VCO} refers to the VCO gain, R is the loop filter's resistor value where N is the divider value. Equation (2) describes that Pr is proportional to the loop bandwidth (f_{BW}) and phase error (ΔØ). Which means, the reference spurs can be reduced by increasing the reference frequency (f_{REF}) and minimizing the phase error (ΔØ) and loop bandwidth (f_{BW}). Therefore, a CP design is required, which can reduce the current mismatch and maintain the constant current over a wide range of output voltage. By decreasing the current variation and mismatch, the performance of CP can be significantly improved. This reduces the PLL's spurs and static phase offset. Therefore, a CP that can reduce the current mismatch and maintains the currents constant across a wide range of output voltage is the key block for creating an optimum CPPLL system.

Based on the literature review the current mismatch issue in CP design can be overcome in many ways [20-23]. Low-voltage cascade topology [19, 20] is a conventional approach for minimizing the current mismatch at the cost of high output resistance. With this conventional approach, the current mismatching features in these CPs [19, 20] are scaled down to 2%. Besides, current mismatching is reduced to <1% in [6, 8] by integrating operational amplifiers (Op-amp) technique. This method integrates a negative feedback amplifier along with op-amp where Op-amp controls the voltage node maintaining high amplifier gain and provides the advantage of the large input voltage of charge and discharge currents [21]. The current mismatch in [7] is reduced by executing a differential CP with an active loop filter (LF) and common-mode feedback scheme. This scheme integrated an op-amp, an analog adder, and a reference voltage circuit. Huh et al [22] proposed a replica CP where the current mismatch is compensated down to 1% by utilizing a bias generator. But, it requires a complicated circuit and creates a longer locking time. An unexpected current mismatch occurs in this architecture because of the fabrication mismatch between two CPs.

The variables that are responsible for current mismatch are current sharing, charge injection and clock feed. Controlling the switching circuit by the transistor causes charge injection. Charge injection arises when the transistor is utilized to govern the switching circuit and produce limited capacitance to the current sources [20, 23]. Keeping in mind the end goal to diminish current mismatch and current variation, the power consumption and the output voltage dynamic range must also be considered. Besides, the approach with double stage op-amps in three rail-to-rail amplifiers is competent and established for reducing the current mismatch. It adjusts the current mirror gate bias that results in matching the output of the switch current with the drain current. Thus, it reduces the static phase offset significantly and minimizes the current mismatch. This article proposes an improved CP design in 130 nm CMOS process based on the current mirror method employing an inverter at the gates of transistors for providing a rail-to-rail voltage swing to accomplish adequate current matching.

2 Proposed Charge Pump Circuit

A modified CP is designed based on current mirror technique integrating an inverter at the gates of the transistor to provide a rail-to-rail voltage swing that reduces the current mismatch and the voltage mismatch problem. The recommended CP circuit with current mirrors technique is presented in figure 4. The two current sources I1 and I2 are implemented as current mirrors. I1 and Up utilize PMOS transistors while I2 and Down use NMOS transistors. To increase the output resistance, the lengths of all transistors have been set to twice the minimal size at 700 nm [8]. To decrease the required amount of VGS the transistors with large widths were chosen so that the circuit could perform near the rail. An inverter is added at the PMOS transistor because its input must be inverted. Two inverters were set at the Dn gate to match the capacitances at the gates. Transistors M5 and M9 are connected to the node "aout" through the mirror transistors M6 and M8. This helps to decrease the impact of charge sharing. Moreover, the current mirror approach ensures that the charge and discharge currents retain a precise value for large voltage and guarantee that the Up and the Dn inputs are matched well. To assure both currents are equivalent, the current mirror is utilized for replicating current Up and current Dn from a single current source.

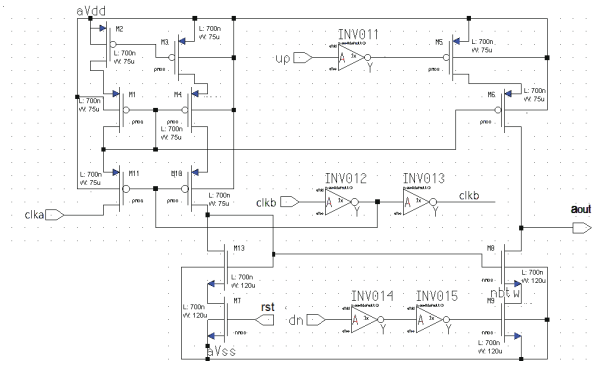

Figure 4: The proposed CP circuit based on current mirrors technique with inverters

3 Results and Discussions

The post-layout results of the designed CP circuit are depicted in figure 5-9. From the post-layout simulation, it is shown that the proposed CP can reach maximum output voltage of 1.8 V. Generally, schematic simulation is viewed as an ideal case, while the post-layout simulation is considered the actual case, which incorporates reverse charge sharing or body impact and parasitic capacitance. The post-layout simulation output voltage result is identical in comparison with the schematic simulation. The output results of the designed CP are verified using ELDONET simulators in TSMC 130 nm CMOS process. Usually, the voltage amplitudes of "clka" and "clkb" are equal to the power supply (VDD). The simulation parameters are used at 10 MHz pumping clock frequency along with 0.1 pF pumping capacitor and the input voltage connected to a 1.8V power supply. It is found that the designed CP circuit is successfully pumped up and down for the output voltage range from 0.1V to 1.8V. Figure 5 shows that when the reset transistor is disconnected, "clkb" is set to be delayed by 1.5 ns. As a result, the output waveform is observed to be charged up to Vdd, and the Up signal is wider than the Dn signal.

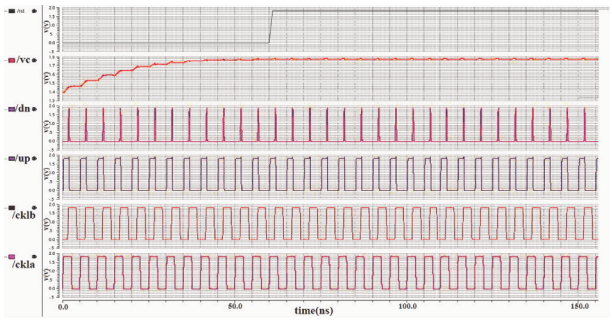

Figure 5: Post layout Result of Proposed CP Circuit: Pumping-Up @ (Vdd = 1.8 V, f = 10MHz)

Figure 6 clearly shows the voltage trend at the Vc node moving down, and the Dn pulse is wider than the Up pulse. When the reset transistor is connected, and "clka" signal is delayed by 1.5 ns. Figure 7 is the zoomed plot of the simulation where the Dn and Up signals are perfectly in phase with the pulse widths being 224.6 ps (Dn) and 222.8ps (Up). The voltage of pumping-up and pumping down for the modified CP is in the range between 0.1 V and 1.8V.

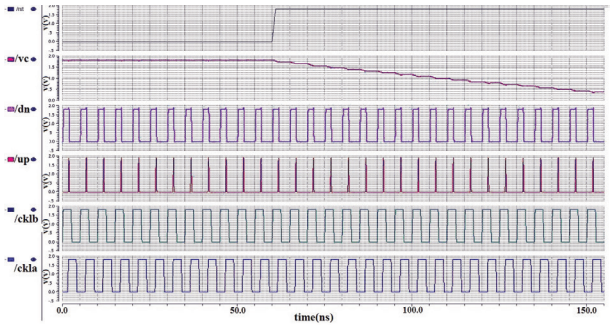

Figure 6: Post layout of the proposed CP Circuit: Pumping-down@ (Vdd = 1.8 V, f = 10MHz).

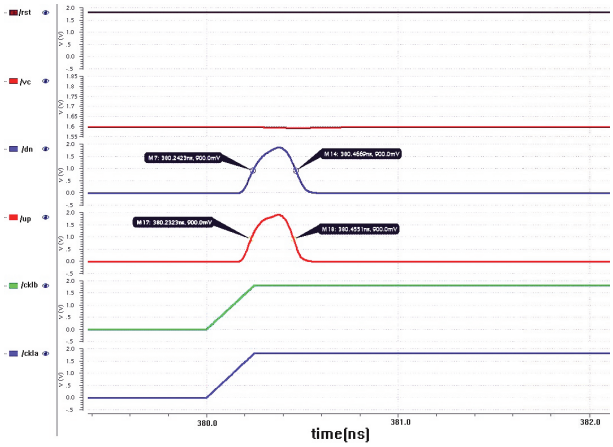

Figure 7: Simulation result of proposed CP Circuit (When both clock sources set are perfectly in-phase)

Figure 8 describes the current matching of the designed charge pump circuit, and it is observed that the maximum value for the current mismatch is zero. The curve (Figure 8 results) is taken from the Mentor Graphics EZwave analysis window. In EZwave window, the current mismatch is shown in the form of the graph instead of a percentage. The cyan and Blue, both graphs represent the current (Y-axis) graph with respect to time(X-axis). It can be seen in the figure that, the changes in the current of both graphs with respect to time (X-axis) is almost the same. There is no difference in current fluctuation which represent the Zero current mismatch. The zero current mismatches are achieved because of the low voltage NMOS cascade mirror technique and the addition of the M5 and M9 which are connected to the node "aout" through the mirror

transistors M6 and M8. For the PMOS switched mirror, the low-voltage cascade current mirror is connected to Gnd and for the NMOS switched mirror VDD is chosen as these are the values of Up and Dn signals at the lock which results in higher matching. Figure 8 proves that this modified scheme manages to decrease the effects of charge sharing and the current mismatch as well.

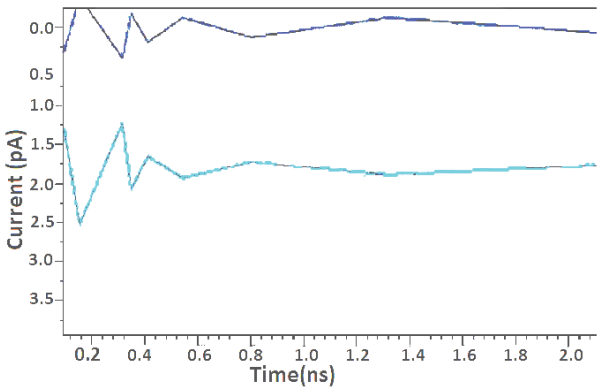

Figure 8: Current Up and Dn Plots (current matching)

Statistical analysis is very important in the absence of measured results. The Monte Carlo analysis of the proposed CP is presented in Figure 9 as a histogram representation. For 50 runs, the actual current mismatch of the proposed CP is zero. But randomly it shows the current mismatch varies from -2 to 2.5% which is very negligible. Besides, according to the netlist analysis of Monte Carlo simulation, the results showed that the current mismatch performance of the CP was stable around zero percentage. The Monte Carlo analysis was performed in the Mentor graphics environment.

The performance comparison among proposed CMOS charge pump circuit and recently reported other CMOS CP designs based on different input and output parameters are given in table 1.

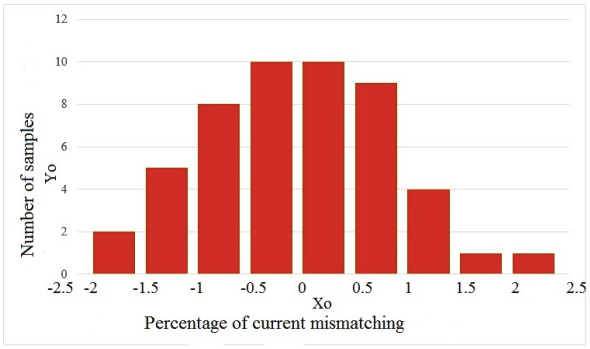

Figure 9: Monte Carlo simulation of current mismatch of the proposed CP

From table 1, it can be noted that the performance of the charge pump can be assessed by the current mismatch and power dissipation. For easy integration on a compact die, the designer tends to choose a simple circuit architecture for the charge pump. It can be observed from table 1 that the proposed CP circuit exhibits a many-fold reduction in both current mismatch and power dissipation compared to others designs. The major advancements have been achieved in the current mismatch of the proposed CP. The maximum current mismatch (<7%) occurs in [6] in table 1. The channel length modulation effect, the mismatch between PMOS and NMOS transistors and CMOS process variations cause this high current mismatch. Park et al.

Table 1: Comparison of proposed CMOS CP performance with other CMOS CP architectures.

Publication year and Ref.	CMOS CP scheme	CMOS process (µm)	Supply voltage (V)	Output voltage (V)	Current mismatch	Power consumed
[23] [2011]	Rail-to-rail op-amp	0.18	1.8	0.4-1.7	0.4%	0.9 mW
[24] [2013]	Basic CP-PLL	0.18	1.8	0.7-1.3	5%	1.6 mW
[8] [2013]	Digital calibration technique	0.18	1.8	-	1%	6.2 mW
[11] [2014]	Dickson CP with CTS's	0.18	1.8	1.8-4.2	-	1.2 mW
[25] [2015]	Feedback Op-amp	0.18	1.8	0.25- 1.	<5%	13 mW
[26] [2016]	Wide-swing current mirror	0.18	1.8	0.3- 1.5	0.32%	0.38 mW
[6] [2017]	Feedback loop	0.18	1.8	0.3-1.4	<7%	740 µW
Proposed CMOS CP	**Current mirror and chain inverter**	**0.13**	**1.8**	**0.1-1.8**	**0%**	**0.178 µW**

[25] suggested architecture also suffers from a high current mismatch of <5% because of the finite output impedance of the current source and highest power consumption of 13 mW. A high power consumption and current mismatch are achieved at the same time by Zhiqun et al. [6] Implementing a rail-to-rail operational amplifier. The recently reported CP proposed by Lozada et al. [8] managed to achieve a good current mismatch of 0.32% and less power consumption compared to [6, 11]. Therefore, compared to results mentioned in table 1, it can be concluded that the proposed charge pump circuit has the lowest power consumption of 0.178 mW and provides the lowest (zero) current mismatch by using the current mirror and chain inverter technique which leads to a high-performance CPPLL. Moreover, in the case of output voltage, it is clear that the output voltage of the proposed CP is significantly higher than those of all previously designed [24-26] charge pumps. This signifies the notable enhancement in output over those achieved in previous researches.

Figure 10 presents the complete layout of the proposed CP using TSMC 130 nm CMOS process. The dimension of the designed CP layout is 17 x 59.5 μm. Since the CP circuit covers only a small area, it reduces the cost as well. In this design, the triple-well isolated MOSFET structure has been used. Multi-finger structure has also been implemented for transistors with large aspect ratios to keep the conductivity within acceptable limits. The layout is designed for the convenience of cascading an extra pumping stage to the output voltage for additional improvement. Fabrication in CMOS technology makes it a good candidate for integration with other CMOS-based devices or modules in telecommunications and other electronic applications.

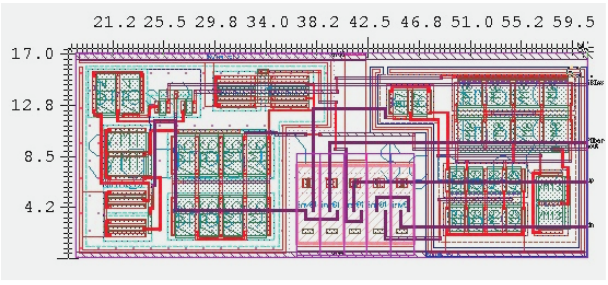

Figure 10: Layout diagram of proposed CMOS CP using TSMC 130 nm CMOS technology

4 Conclusions

The CP output parameters have a large impact on PLL performance. To meet the current demand of low power consumption, zero current mismatch and zero net charges, an enhanced charge pump circuit implementing the current mirror technique along with an inverter is presented in this research. The low voltage NMOS cascade mirror technique and additional transistors that are connected to the output node through the mirror transistors manage to achieve the lowest current mismatch. The post-layout result shows that the proposed charge pump circuit provides zero current mismatch at 1.8 V supply voltage with a pumping capacitor of 0.1 pF and consumes only 0.178 μW. The charge pump circuit is suitable for Readerless RFID applications and can be widely used in various low power wireless electronic devices such as a transceiver; disk read/write channels for high-speed data transmission, clock synthesis, synchronization, jitter reduction, etc.

5 Conflicts of Interest

"The authors declare no conflict of interest."

6 Acknowledgment

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