

Digitally Adjustable Differential Gain Stage

Miha Gradišek, Drago Strle

Laboratory for Microelectronic, University of Ljubljana, Faculty of Electrical Engineering, Ljubljana, Slovenia

Abstract: Most ASIC's demand signal conditioning sub-circuits to modify various signal parameters; one of the important parameter is the gain. The presented configuration is based on the conventional R-2R structure which mainly suffers from the mismatch imperfections. The study shows possible approach to improve mismatch characteristic or enables us to take the advantage to increase bit resolution without mismatch deteriorations. The approach could be used to even further improve accuracy of the numerous previously described approaches [1], [2] which already eliminate high resolution mismatch imperfections. Paper presents the implementation of the gain stage with digital gain adjustment, in the range from 0.9 to 1.1 in 128 equidistant monotonous steps, nevertheless the approach could be implemented even for higher resolution stages. For robust design in terms of the fabrication process and harsh environment operation, a fully differential amplifier was designed in standard 0.18 μ m CMOS technology. Designed amplifier in combination with resistive network is presented together with simulation results including the parasitic capacitances.

Keywords: digitally adjustable gain; resolution improvement; R-2R stage; differentially balanced structure

Digitalno nastavljiva diferencialna ojačevalna stopnja

Izveček: Večina namenskih integriranih vezij potrebuje podslope vezij, ki skrbijo za obdelavo signalov in njihovih parametrov; pomemben parameter je ojačenje. Predstavljena konfiguracija bazira na konvencionalni R-2R strukturi, ki je znana po neznamenljivem vplivu neidealnosti ujemanja elementov vezja. Študija predstavlja možen pristop za izboljšavo teh karakteristik oziroma nam omogoča povečanje ločljivosti ne da bi se pri tem poslabšale karakteristike ujemanja. Pristop se lahko uporabi na že znanih rešitvah za odpravo neidealnosti [1], [2] in tako še dodatno izboljša ločljivost. Delo predstavlja implementacijo ojačevalne stopnje z digitalno nastavljivim ojačenjem od 0.9 do 1.1 v 128 ekvidistančnih monotoni korakih, vendar bi se lahko podoben pristop uporabil tudi za stopnje z večjo ločljivostjo. Robustno delovanje glede na proces izdelave in obratovalne pogoje je dosežen z diferencialnim ojačevalnikom dizajniranim v standardni 0.18 μ m CMOS tehnologiji. V članku je predstavljen načrtan ojačevalnik v kombinaciji z uporabnim vezjem skupaj s simulacijskimi rezultati vključujoč parazitne kapacitivnosti.

Ključne besede: digitalno nastavljivo ojačenje; izboljšanje ločljivosti; R-2R stopnja; diferencialno uravnotežena struktura

* Corresponding Author's e-mail: miha.gradisek@fe.uni-lj.si

1 Introduction

Common part of numerous analog ASIC's (Application Specific Integrated Circuits) incorporate circuits for signal conditioning. Modification of signal amplitude through gain adjustment presents one of the most frequently used approach. Several implementations are possible. In analog implementations the gain is changed using some nonlinear element in the feedforward or feedback path; the problem of such implementations is large distortions of the signal. In narrow band systems, this is acceptable, however, in our case, the system is wide band and thus analog nonlinear gain adjustment is not acceptable because we would like to

achieve the distortions in the range of 0.01%. Thus, the only possibility is digital gain adjustment [3]. Each approach has associated advantages and disadvantages shortly described above. The important characteristics of the digital gain adjustment stage are: the resolution of gain steps, the responsivity, the distortions, the bandwidth, the area, and the final product cost.

The paper investigates a possible approach for digital gain adjustment using the similar circuit as known from the R-2R DA converters. The implementation is based on the conventional R-2R ladder structure to adjust the gain through the binary weighted currents. Com-

pared to other structures it has some advantages (for example small area and fast switching) and some disadvantages (for example non-monotonicity) [4], where non-monotonicity is more evident at higher number of bits. The monotonicity performance of a higher resolution stages could be improved by a numerous approaches as a resistor laser trimming procedure, binary LSB and unary MSB algorithmic segmentation [2], ordered element matching [1] and others. Some of them contributes to more complex digital logic with interconnection considerations taking into account wiring placement as a result of on-chip gradients, while some others enlarge inevitable die area as a result of inability of analog component accuracy at shrunk dimensions [2]. Mismatch suppression could be achieved with increased dimensions of the unit resistors as described with the Pelgrom's Law [5]. Nevertheless monotonicity could be improved even without increment of the resistor dimensions at the expense of additional R-2R structure presented in this work. Approach take the advantage of the fully-differential interconnection of both structures which yields higher robustness [6]. A method which maintains monotonicity of the gain stage with higher number of bits in the ASICs with two anti-phase shifted input signals is proposed.

The paper is organized as follows. Section 1 introduces the problem and explains why the R-2R structure is preferable. Section 2 describes the principle of operation, while Section 3 presents simulation results. Section 4 presents the layout and Section 5 concludes the article.

2 Circuit description

2.1 Principle of operation

The principle schematics of a fully differential, digitally adjustable gain stage is shown in the Fig. 1. It consists of a resistive network composed of two R-2R ladder structures and feedback resistors. The adjustable gain stage provides the gain in the range from 0.9 to 1.1. R-2R determined adjustable gain ($Gain = \pm 0.1$) is superpositioned to the constant one ($Gain = 1$) determined by feedback resistors R_{FB1} and R_{FB2} . To take the advantage of the proposed approach of doubling gain range, input signals **inp** and **inn** should be anti-phase shifted as differential structure suppresses in-phase signals. In the case when multiplexer directly translates the portion, determined by the bits, of the signal **inp** to the upper amplifier feedback resistor R_{FB2} , the absolute amplitude of the output signal **outn** is increased and in contrary decreased in a case when the portion of the **inn** is crossed through a multiplexer and tied to the

upper resistor R_{FB2} . In this manner multiplexer with its switches permutates in-between two R-2R ladder structures and thus control whether the gain is increased or decreased. The proposed approach with differentially connected R-2R structures yields higher resolution compared to single-ended structure at the expense of increased die area. The stage has gain resolution equivalent to 7 bits. According to the desired gain, determined by the six bits b_i ($i=0,1,\dots,5$) plus additional one b_6 for multiplexer (sign bit), the portion of the current from the R-2R structure is connected either to the signal ground or to the summing point at the input node of a differential amplifier. Resistor R_{FB2} in combination with differential TIA (trans-impedance amplifier) serves as a current to voltage converter. Two differential output signals are kept around the signal ground with a help of common mode feedback circuit (**CM** block in the Fig. 1). Output common signals are assured by a help of additional amplifier which compares the voltage V_{CM} to the reference voltage (i.e. signal ground) and provides error correction through the feedback biasing signal V_{CMB} (Fig. 2).

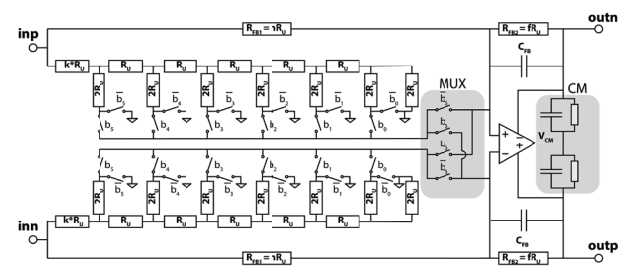


Figure 1: Simplified schematic of a fully differential, balanced, R-2R adjustable gain stage.

2.2 Resistive network

The gain of the stage is composed of two super-positioned contributions. The constant one is determined by the ratio f/n of resistors R_{FB1} and R_{FB2} while the variable one is based on the adjustable R-2R stage determined by binary weighted currents delivered to the virtual ground of the TIA from the R-2R stage. Values of resistors are determined in a way to achieve a desired gain range from 0.9 to 1.1 in 128 equidistant monotonous steps. Desired gain steps can be realized according to (1) by setting unit resistors multiplication factors to $k=153$, $n=16$ and $f=16$ (see (1)).

$$Gain = - \left(\sum_{i=0}^5 \frac{R_U}{(k+1)R_U} \frac{b_i}{2R_U} (-1)^{b_i} + \frac{1}{nR_U} \right) fR_U \quad (1)$$

Unit resistance is selected appropriately to provide on one side sufficient accuracy and bandwidth, and on the other side to maintain low noise and low current con-

sumption. The resistors should exhibit high linearity (low voltage coefficient), small temperature coefficient, acceptable noise, small parasitic capacitance and good matching properties. This is accomplished by appropriate size of the unit resistor and appropriate layout. Considering mentioned parameters, high resistive poly resistor is used [4]. Unit resistance R_U is composed of foundry minimal recommendation of five squares. Used high resistive poly resistor with sheet resistance of approximately $350 \Omega/W$ yields $R_U \cong 1.836 \text{ k}\Omega$.

2.3 Switches

In order to realize high accuracy of gain adjustment, it is essential to properly construct the switches as well. Weighted currents in the R-2R branches call for scaled switches from the one with a minimum conduction resistance for b_5 to the switch with maximum resistance for b_0 , which has 32 times larger resistance compared to the switch b_5 . Nevertheless, maximum resistance of each switch should be much smaller than the unit resistance R_U . To meet the switch conduction requirements, they should be adequately dimensioned. For the same reason, multiplexer switches should be properly designed as well. In general, large switches have relative large parasitic capacitance that affects the speed and stability. However, R-2R switches in the proposed approach do not experience any voltage change as they are tied to the signal ground node. This is convenient in terms of the system bandwidth. R-2R and multiplexer switches are constructed as transmission gates with complementary MOSFETs with different dimensions to maintain approx. linear resistance over different voltages. In addition, dummy MOSFETs are added to the nodes, to reduce the clock feedthrough effect and off channel charge injection during switching and to ensure the same loading of all driving lines, thus to mitigate the gain transition glitches. Remaining imperfections during gain adjustment are empirically determined by simulations and solved with time delayed control lines through buffered inverters.

2.4 Differential trans-impedance amplifier

Fully differential TIA with feedback resistances R_{FB2} and R_{FB1} converts currents out of the resistive R-2R network to two differential output signals. Since closed loop configuration impact overall system bandwidth and stability, the TIA is based on the folded cascode architecture (Fig. 2). Sufficient unity-gain bandwidth is needed to overcome the gain variations at the frequency of the signal. Poorly designed TIA, in terms of bandwidth, can at high frequencies cause large gain variations. TIA is composed of a PMOS differential pair (M3, M4) with tail current of $200\mu\text{A}$, which is distributed between two NMOS transistors (M5, M6). Each of them

drains additional current of $40 \mu\text{A}$ from PMOS load (M7, M8). To clearly present conformation, additional cascode transistors for performance improvement are missing in the simplified schematic. Output stage is based on the common source configuration with Miller compensation.

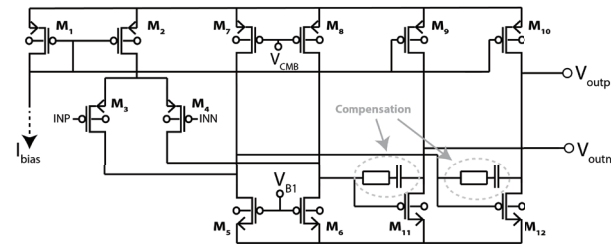


Figure 2: Transimpedance amplifier based on the folded cascode architecture.

TIA must be stable under all conditions, therefore a differential and common mode stability is assured using appropriate frequency compensation circuitry. It should be properly designed using appropriate feedback capacitor C_{FB} (Fig. 1), which implements low pass filtering characteristics. This capacitance compensates influence of the parasitic capacitance of the switches in the R-2R ladder structure.

3 Simulation results

The circuitry is designed in TSMC 180nm CMOS technology and characterized using Cadence Virtuoso environment. Process verification includes all process corners: typical, low-slow, slow-fast, fast-slow, fast-fast and/or statistical variations: MC, MM; complete temperature range from -40°C to 150°C and supply voltage range from 3V - 5V .

Principle of operation of gain adjustment is presented in the Fig. 3. The gain is equal to 1 when the bits b_5 - b_0

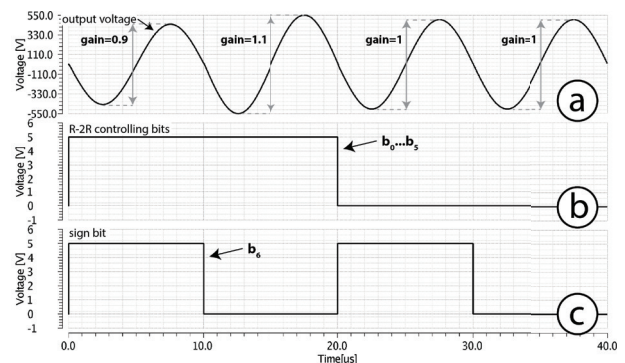


Figure 3: Gain adjustment: (a) signal at the output of the amplifier, (b) status of controlling bits b_0 to b_5 , (c) status of multiplexer bit b_6 .

are set to low independently of the multiplexer bit b_6 . When b_6 is low, enabled b_0 - b_5 bits increase the gain up to 1.1 and when b_6 is high the gain is decreased from 1 down to 0.9 in 127 equidistant steps.

Figure 4 shows transient response to 500 kHz input square signal. The system settles $2\mu\text{s}$ after power-on.

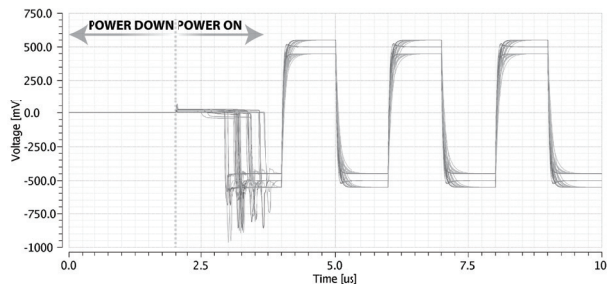


Figure 4: Transient response at gain: 0.9, 1 and 1.1 for 500 kHz square-wave input signal.

Implementation with two 6-bit R-2R ladder structures yields better accuracy as one with single 7-bit R-2R structure. In the Fig. 5, the matching accuracy of two 7-bits R-2R ladder based structures are presented. Fig. 5(b) shows LSB gain variations for proposed approach with two 6-bit R-2R structures and multiplexer which implements the b_6 compared to the previous design [4] with one 7-bit R-2R structure presented in Fig. 5(a). One 6-bit R-2R structure provides adjustable gain range of 0.1 which is doubled over constant gain of 1 with a help of an additional 6-bit R-2R and multiplexer, while 7-bit R-2R have to provide an adjustable gain range of 0.2 above the constant gain of 0.9. Distribution of the LSB gain shows improvement of the standard deviation of the proposed approach compared to the previous one for approximately 40%.

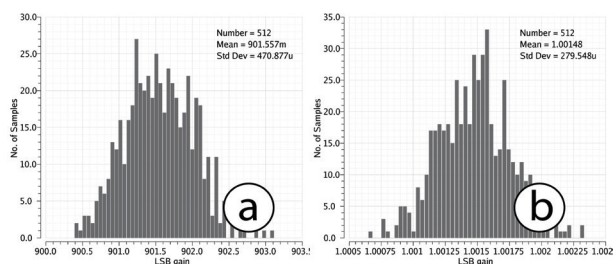


Figure 5: LSB gain variation: (a) mismatch of the previous design and (b) mismatch for proposed approach.

Closed loop AC characteristics of the amplifier with digital gain adjustments are presented in the Fig. 6, for gains set to 0.9, 1 and 1.1. At higher frequencies, the gain characteristics starts to distort as a result of process influence to the gain bandwidth of the TIA. Nevertheless, closed-loop gain characteristics at low frequencies are mainly affected by the mismatch contribution of the R-2R structure [7]. It is evident in the case when

an ideal amplifier is used and R-2R mismatch is the main contributor to the overall gain variations, which are listed in the Table 1.

Table 1: Influence of process and mismatch variations on the LSB gain using real and ideal TIA.

	Real amplifier		Ideal amplifier	
	Std. dev.	Std. dev.	Std. dev.	Std. dev.
	@ 100kHz	@ 500kHz	@ 100kHz	@ 500kHz
Process	8.20E-05	1.83E-03	1.42E-07	3.46E-06
Mismatch	2.90E-04	4.58E-04	2.82E-04	2.82E-04

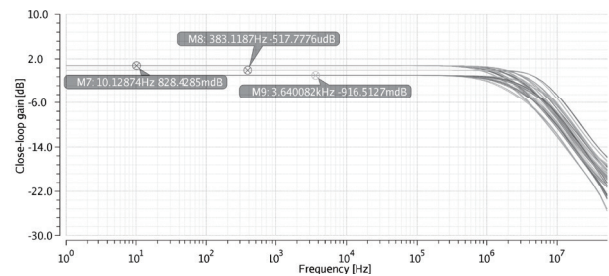


Figure 6: Closed-loop characteristic for the gain stage with gain variations 0.9, 1 and 1.1.

Figure 7 shows open loop differential AC characteristics. Most critical phase margin of 53° is met at 12.7MHz for 3V power supply, fast-fast corner and at temperature of 150°C . Fig. 8 shows AC characteristics for common mode feedback signal (V_{CM}). It shows stable behavior and provides the appropriate output common signal.

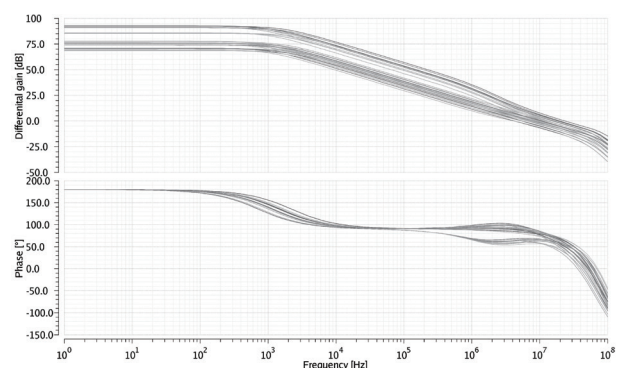


Figure 7: Differential open-loop gain and phase characteristics.

The offset of the complete gain stage is generated inside the TIA, as a result of the mismatch of the MOSFETs in the input differential stage. Offset distribution based on Monte-Carlo simulation is shown in the Fig. 9. The maximum input offset is 3mV and is included in the evaluation of the system performance.

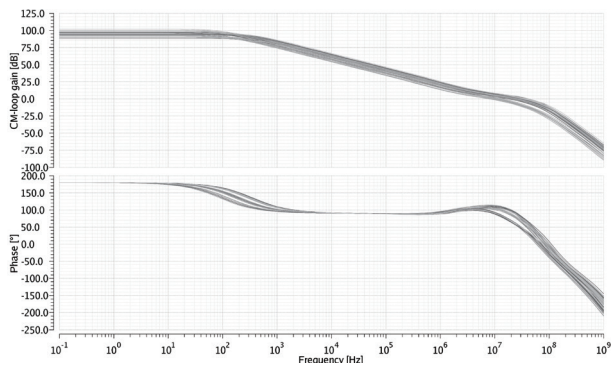


Figure 8: Open-loop gain and phase characteristics of the common mode feedback signal V_{CM} .

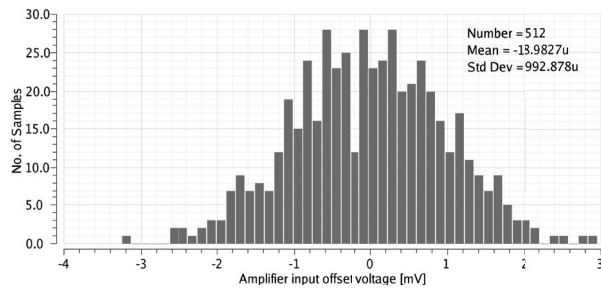


Figure 9: TIA input offset for mismatch variations.

The CMRR behavior of the gain stage with added input offset voltage of 3mV is shown in the Fig. 10. The presented characteristics show that the amplifier input offset deteriorate CMRR performance as it is proportional to the invert value of the offset [8].

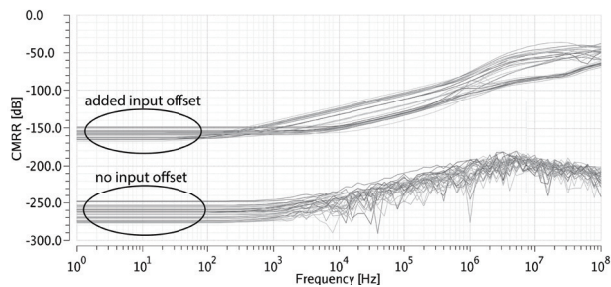


Figure 10: CMRR with and without added offset.

The important parameter is also a phase shift at the highest frequency of 500 kHz. The worst phase shift of 14° happens as expected at the largest gain, for supply voltage of 5.5V, at 150°C and max process variation of the R-2R structure. This deviation could be trimmed in the separate process of the phase shifting. Typical power consumption is 660 μA at 3.3V supply voltage, typical process parameters and 25°C . It is increased to 860 μA at 5.5V supply voltage, fast-fast process parameters corner and at 150°C .

4 Layout

The layout of the stage is presented in the Fig. 11. It is symmetrical. As already mentioned, the R-2R implementations are prone to glitches during gain switching. Appropriate control logic is realized in a way to equalize digital control signals delay. The resistors mismatch is improved by using the optimum width of the resistors (R_U dimensions $4\mu\text{m} \times 20\mu\text{m}$). In addition, the surrounding of all resistors must be the same, which is achieved using appropriate dummy resistors that reduce the edge effects. Analog inputs are shielded from the digital signals. For higher accuracy, sensitive current mirrors and differential stage of the TIA are protected with additional dummy devices. Signal ground tracks are wide enough to minimize voltage drops across the gain stage. Overall silicon area occupies approximately 0.2 mm^2 .

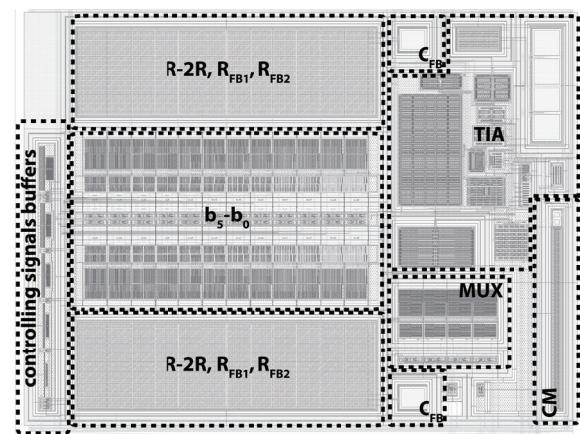


Figure 11: Layout of adjustable gain ratio cell.

5 Conclusions

This paper presents design, optimization and implementation of a digitally adjustable gain stage, based on R-2R structure. Proposed approach yields performance improvements in terms of the accuracy compared to the previous realizations. Designed TIA is implemented in a way to provide sufficient bandwidth of the system together with the parasitic contributions of the resistive network and switches. The characteristics of the amplifier are verified in terms of process and mismatch variations as well as supply voltage and temperature.

6 References

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