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A Compact 3.1–5 GHz RC Feedback Low-Noise Amplifier Employing a Gain Enhancement Technique

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Abstract: A low-noise amplifier (LNA) with main cascode amplifying stage utilizing a current-reuse transconductance-boosting technique is presented in this paper. This topology increases the effective transconductance, g_m, of the input transistor and prevents a large voltage drop across the load resistor, thus reducing power consumption. The feedback topology made of source follower connected in series with a parallel RC network improves input impedance matching at high frequencies, while a gate peaking inductor inside the feedback loop enhances the amplifier bandwidth. The proposed LNA is implemented in UMC 0.18 µm CMOS technology for a lower band of the ultra-wideband spectrum from 3.1 to 5 GHz. Measurements show a power gain (S_{21}) of 9.7±0.45 dB with the 3-dB band from 1.1 to 5.57 GHz. The input return loss (S_{11}) is below −10 dB from 1 to 5 GHz, while the output return loss (S_{22}) is less than −10 dB and the reverse isolation (S_{12}) is better than –25.5 dB across the whole measured bandwidth, 1–7 GHz. The input-referred 1-dB compression point (P_{1dB}) is −10.5 dBm at 3 GHz. The average noise figure (NF) obtained by post-layout simulations is 4.24 dB, with a minimum value of 4.05 dB at 4.92 GHz. By using only one inductor in the proposed design, the total chip area is greatly reduced to 0.913 mm^2. The LNA core area occupies 0.353 mm^2 and consumes 9.97 mW from a 1.8 V supply.

Keywords: CMOS technology, radio frequency integrated circuits (RFIC), ultra-wideband (UWB), low-noise amplifier (LNA), current-reuse technique, resistive-feedback technique

Kompakten 3.1–5 GHz RC povratni nizkošumni ojačevalnik s tehniko povečanja ojačenja

Izvleček: V članku je predstavljen nizkošumni ojačevalnik (LNA) z glavno kaskodno ojačevalno stopnjo s tehniko ponovne uporabe toka in povečanja transkonduktance. Uporabljena topologija povečuje efektivno transkonduktanco g_m vhodnega tranzistorja in preprečuje velike napetostne padce na bremenskem uporu, kar zmanjšuje porabo. Povratna topologija serijsko povezanega sledilnega vira s paralelnim RC omrežjem izboljšuje ujemanje vhodne impedance pri visokih frekvencah, pri čemer gladilna tuljava vrat v povratni zanki povečuje pasovno širino ojačevalnika. Predlagan LNA je izveden v UMC 0.18µm CMOS tehnologiji za spodnji del ultra širokega pasu spektra od 3.1 do 5 GHz. Meritve izkazujejo donos moči (S_{21}) 9.7±0.45 dB s pasovno širino 3-dB med 1.1 in 5.57 GHz. Povratne vhodne izgube (S_{11}) so pod -10 dB med 1 in 5 GHz, izhodne povratne izgube (S_{22}) so pod -10 dB, povratna izolativnost (S_{12}) boljša od -25.5 dB preko celotne pasovne širine 1-7 GHz. Vhodno naslovljena 1 dB točka kompresije (P_{1dB}) je -10.5 dBm pri 3 GHz. Povprečna slika šuma simulacije po postavitivi je 4.24 dB. Pri uporabi le ene tuljave se površina čipa močno zmanjša na 0.913 mm^2. Jedro LNA zaseda 0.353 mm^2 in porabi 9.97 mW pri 1.8 V napajanju.

Ključne besede: CMOS tehnologija, radio frekvenčna integrirana vezja (RFIC), ultra širok pas (UWB), nizkošumni ojačevalnik (LNA), uporovna povratna tehnika

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1 Introduction

In 2002, the Federal Communication Commission (FCC) set up rules and regulations for ultra-wideband (UWB) technology and allocated 7.5 GHz of unlicensed spectrum (from 3.1 to 10.6 GHz) for commercial deployment [1]. An UWB signal is defined as any signal that occupies bandwidth greater than 500 MHz or whose fractional bandwidth exceeds 0.20, where fractional bandwidth is defined as the −10 dB bandwidth occupied by the signal divided by its center frequency.

There are two different UWB approaches: multi-band (MB) UWB technology and impulse radio (IR) UWB. The former uses frequency hopping with orthogonal frequency division multiplexing (OFDM), where the available bandwidth of 7.5 GHz is divided into 528 MHz subbands, while the latter uses a series of short duration impulses, typically on the nanoseconds scale, utilizing a very wide bandwidth in the frequency domain. In MB-OFDM four band groups are defined, such as group A (3.1–4.9 GHz), B (4.9–6 GHz), C (6–8.1 GHz), and D (8.1–10.6 GHz), while the IR-UWB can be subcategorized in Time-Hopping (TH) UWB and Direct-Sequence (DS) UWB. The band of DS-UWB is separated into two parts, low band (3.1–4.9 GHz) and high band (6.2–9.7 GHz) [2].

The applications of UWB technology cover two areas: high data rate transmissions over short distances and low data rate communications with ranging and localization capabilities. The high data rate mode of UWB is related to short range wireless personal area networks (WPANs), while in the low data rate mode, UWB systems allow a new range of applications, including medical, military, vehicular radar, and security systems [3]. Generally, UWB shows a number of advantages compared to conventional narrowband applications, such as good time domain resolution, immunity to multipath propagation and interference, and potentially low complexity and low cost [4].

The FCC did not specify the type of the signal and modulation scheme of the UWB signal, but only the spectrum mask that the signal needs to meet with the emission limit restrictions issued for each specific UWB application. Power levels set for wireless communications are very low, i.e. −41.3 dBm/MHz, which allows coexistence of UWB and other conventional narrowband systems. Due to these strict power emission rules for the transmitter and the additional transmission path losses, the received signal power is typically three orders of magnitude smaller than that of narrowband systems [5]. This makes UWB receiver front-end design very challenging, particularly the design of the UWB low-noise amplifier. Since the overall noise figure of the receiver is mainly determined by the NF and the gain of the LNA, a sufficient gain and a low noise figure within a defined bandwidth is obligatory. In addition, to reduce return losses, adequate input and output matching is needed. All these requirements have to be fulfilled with low power consumption and within a wide bandwidth. Furthermore, for an UWB LNA designed for OFDM systems good power linearity is required to suppress adjacent channel interference. In the UWB impulse radio systems with more complex forms of modulation, e.g. BPSK (Binary Phase Shift Keying), good phase linearity (i.e., small group delay variation) is required instead. The frequency component of the transmitted signal should experience the same delay amount to be recovered properly.

With increasing interest on commercial wideband integrated systems such as radars and wireless UWB and optical receivers, there is a demand for wideband complementary metal-oxide semiconductor (CMOS) amplifiers in the front-end section of such systems, since the CMOS process is more attractive and promising technology for high level of integration and system-on-chip (SOC) applications. CMOS devices offer the advantages of high f_T and f_{max} as well as superior linearity and lower voltage operation, due to lower threshold voltages (CMOS V_T vs. bipolar V_{BE}). Bipolar junction transistors (BJT) offer the advantages of noise performance and an improved transconductance. The 1/f noise due to carrier trapping-detrapping at interface states and thermal noise due to gate and channel resistances are both significantly higher in CMOS than in BJTs. To reduce noise, very large CMOS devices and large operating current are often required. While the ultimate selection is based on system specifications, the noted differences between performance and economics also need to be considered.

Often, the LNA's performance depends on on-chip inductors, which occupy a large area, making these topologies less attractive for low-cost application [6–8]. In this paper, an LNA with one main amplifying stage implemented in low cost UMC 0.18 μm CMOS technology is presented. Since inductors available in the used technology consume very large chip area, it was necessary to decrease their number. Only one peaking inductor inside the feedback loop is used in proposed design for enhancement of the amplifier's bandwidth. Furthermore, to overcome this technology constraint and to meet the requirements for LNA figures of merit (FoMs) some additional design techniques need to be used. To achieve wideband input impedance matching, the feedback network enhanced with a shunt capacitor. High gain in the whole operating band and low power consumption are obtained by merging resistive-feedback and current-reuse transconductance-

boosting technique. Section 2 presents basic UWB LNA topologies, Section 3 gives insight into the feedback technique and Section 4 explains the proposed circuit topology. Section 5 reports the measurement results along with the simulation data. Section 6 contains the conclusions based on the performance of the proposed LNA.

2 UWB LNA design techniques

There are several wideband amplifier architectures that can be used in CMOS technology.

The general block diagram of a distributed amplifier consists of transmission lines (realized using either coplanar waveguides or cascaded LC circuits) and gain stages distributed along them, that determine the overall gain of the amplifier. With this architecture impedance matching over a wide bandwidth can be achieved, but losses in the transmission lines limit the maximum gain. Moreover, it usually employs many spiral inductors that occupy a large chip area and consume considerable amounts of power, which makes them unsuitable for low power and low cost applications [6], [7].

The overall input reactance of the common-source amplifier with inductive source degeneration and extended with a multi section filter structure as input impedance matching circuit, is in resonance over the whole band. With this architecture low power consumption can be achieved, although noise performance will be degraded due to the LC network loss. In addition, a large silicon area is required, occupied by numerous integrated inductors [8].

The common-gate stage provides wideband input impedance matching with less design complexity and small area occupancy, for proper device size selection and bias current of the input transistor. However, the main disadvantage of this amplifier is a high noise figure as its relatively low transconductance value cannot provide low noise and high gain in the whole frequency range. To overcome this issue and discrepancy between input and noise matching, noise cancelling methods need to be used. Also, this type of amplifier is usually combined with an additional amplifying stage, which provides high-frequency gain and enhances the bandwidth [9].

Another area-saving solution is a common-source amplifier with resistive shunt-feedback technique [10]. With this approach wideband input impedance matching and flat gain can be obtained, though it is challenging to achieve very wide bandwidth with low NF. Moreover, due to strong dependence of voltage gain on the amplifying transistor's transconductance a large amount of current is required to achieve high gain. Therefore, to increase the transconductance and to reduce the power consumption a novel LNA circuit design needs to be proposed.

3 Theory of resistive-feedback LNA

The basic feedback topology, where the feedback resistor R_F, is implemented directly between the gate and drain of the input transistor, at low frequencies and under the impedance matched condition, exhibits a voltage gain of:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{R_L - g_{m1}R_L R_F}{R_L + R_F} \approx -\frac{R_F}{Z_{in}} \tag{1}$$

where R_L is the load resistor, g_{m1} is transconductance of the input transistor M_1, and Z_{in} is the input impedance of this circuit given by:

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{R_L + R_F}{1 + g_{m1}R_L} \approx \frac{R_L + R_F}{g_{m1}R_L} = \frac{1}{g_{m1}}\left(1 + \frac{R_F}{R_L}\right) \tag{2}$$

For a common-source (CS) amplifier employing the feedback resistor connected through a source follower, the voltage gain at low frequencies under the impedance matched condition is:

$$A_v = \frac{v_{out}}{v_{in}} = -g_{m1}R_L \approx -\frac{R_F}{Z_{in}} \tag{3}$$

and the input impedance is given by:

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1 + g_{m2}R_F}{g_{m2}\left(1 + g_{m1}R_L\right)} \approx \frac{1}{g_{m1}}\frac{R_F}{R_L} \tag{4}$$

where g_{m2} represents the source follower's transconductance.

By using A_v and Z_{in} approximate equations (1)–(4), for a voltage gain of 10 dB and input impedance matched to 50 Ω, the feedback resistor R_F in both cases is 158 Ω. If g_{m1} = 50 mS, it follows from (2) and (4) that R_L is 105 Ω and 63 Ω, respectively. By inserting a source follower in the feedback, the value of R_L is reduced by 40% compared to the topology without it. The reduction in R_L leads to a wider amplifier bandwidth, since a decrease

in load resistance shifts the main pole, determined by the RC time constant of the CS output node, to higher frequencies. An additional benefit of a smaller load resistor value is the decrease in voltage drop across R_L, which allows proper biasing of the amplifying transistor with high current demands.

4 UWB LNA circuit design

The schematic of the proposed UWB LNA is shown in Fig.1. The input stage consists of an amplifying stage based on a cascode configuration, which is enhanced with resistive feedback connected through a source follower, and current-reuse M_3–M_5 block. The output stage is realized as a simple source follower that provides a broadband output impedance of 50 Ω for measurement purposes.

Input impedance matching is obtained by using a shunt feedback circuit, composed of source follower and R_FC_F parallel network. By using the source follower in the feedback path, the value of resistor R_L is decreased, resulting in a smaller voltage drop across the load resistor and in an enhancement of frequency band. However, to achieve a high gain, the drain current of transistor M_1 should be large, which makes the voltage drop still significant. By adding transistor M_3 these two effects, R_L voltage drop and enhancement of the M_1 transconductance, are less coupled. In this way, the current through cascode transistor M_2 is only part of the current of transistor M_1 and the voltage drop across resistor R_L is reduced, thus improving the voltage headroom. The amount of current through transistor M_3 is controlled by the current mirror, formed by transistors M_4 and M_5. By connecting the gate of M_3 to that of M_1, the total transconductance of the input stage g_m is enhanced and is given as the sum of the transconductances of transistors M_1 (NMOS) and M_3 (PMOS). Consequently, the gain of the LNA increases. Additionally, by inserting the current-reuse stage, current through R_L decreases, thus the value of the resistor R_L could be increased, which leads to higher amplifier gain and reduced noise figure value, but smaller bandwidth.

For the basic feedback topology, the input impedance, given by (4), increases at high frequencies as the amplifier gain, $g_{m1}R_L$, drops due to parasitic capacitances. By adding a capacitor C_F in parallel with feedback resistor R_F, the feedback impedance at high frequencies is reduced, the input impedance remains constant with frequency change and the broadband impedance matching is improved.

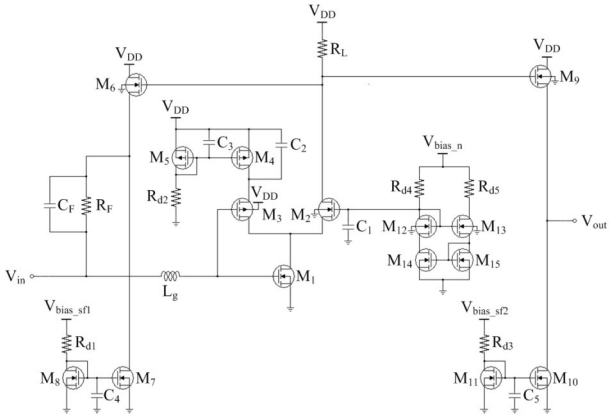


Figure 1: Proposed 3.1–5 GHz CMOS UWB LNA.

The total input node capacitance is approximately the sum of the capacitance C_F and the gate capacitances of transistors M_1 and M_3. Inductor L_g is connected to the gate of M_1 and M_3, as shown in Fig. 1, to resonate with these capacitances. Simulations show, that by increasing the inductance of L_g, gain peaking becomes more significant and the amplifier bandwidth enhances up to some value above which the bandwidth starts to decrease. The voltage signal at the gate of M_1 (M_3), and hence the transconductance, increases approaching the resonant frequency causing gain peaking. Additional increase in the gain value is obtained by adding a large value capacitor C_2 at the source of transistor M_3. With increasing frequency, the source impedance seen by transistor M_3 decreases. This results in a larger transconductance g_{m3} value and consequently a higher LNA gain.

Three simple bias circuits composed of resistors R_{dn} (n = 1, 2, 3) and transistors M_n (n = 4, 5, 7, 8, 10, 11) as current mirrors are used. To decrease the overall power consumption (P_D), the width of the bias transistors is a small fraction of that of the corresponding amplifying transistors. A bias circuit using a modified Wilson current mirror sets the bias level for transistor M_2, as shown in Fig. 1. Supply voltages V_{bias_sf1}, V_{bias_sf2}, and V_{bias_n} are driven externally to provide an additional degree of measurement freedom and ability to compensate for process and voltage variations. In a final design these voltages can be set to V_{DD}, which in turn decreases the number of pads and reduces chip area.

In further analysis, influences of cascode stage and output buffer stage are omitted for simplicity.

4.1 Bandwidth enhancement with inductor L_g

For the LNA employing the RC feedback network connected through a source follower, without inductor L_g at the gate of the input transistor M_1, the voltage gain of the amplifying stage is derived as:

$$A_{v1} \approx -\frac{(g_{m1}+g_{m3})R_L\left(1+j\omega\frac{C_{gs6}}{g_{m6}}\right)}{1+j\omega\frac{C_{gs6}}{g_{m6}}\left(1+\frac{R_L}{Z_F}\right)}\cdot\frac{1}{1+j\omega(C_{gs1}+C_{gs3})R_g} \tag{5}$$

where R_g is the gate resistance, and Z_F is the impedance determined by the capacitor C_F in parallel with the feedback resistor R_F, given by:

$$Z_F = \frac{R_F}{1+j\omega C_F R_F} \tag{6}$$

If the value of resistor R_F is of the same order as the value of resistor R_L, A_{v1} can be simplified as:

$$A_{v1} \approx -\frac{(g_{m1}+g_{m3})R_L}{1+j\omega(C_{gs1}+C_{gs3})R_g} = -(g_{m1}+g_{m3})R_L \tag{7}$$

After inductor L_g is placed inside the feedback loop, the first amplifying stage voltage gain can be approximated as:

$$A_{v1} \approx -\frac{(g_{m1}+g_{m3})R_L\left(1+j\omega\frac{C_{gs6}}{g_{m6}}\right)}{1+j\omega\frac{C_{gs6}}{g_{m6}}\left(1+\frac{R_L}{Z_F}\right)}\cdot$$

$$\cdot\frac{1}{1+j\omega(C_{gs1}+C_{gs3})R_g-\omega^2(C_{gs1}+C_{gs3})L_g} \tag{8}$$

and after simplifying:

$$A_{v1} \approx -\frac{(g_{m1}+g_{m3})R_L}{(C_{gs1}+C_{gs3})L_g\left[\frac{1}{(C_{gs1}+C_{gs3})L_g}+j\omega\frac{R_g}{L_g}-\omega^2\right]} \tag{9}$$

It can be seen that by inserting inductor L_g at the gate of transistor M_1, the second-order circuit is obtained. From (9) follows that the frequency of the pair of complex-conjugate poles is ω_0: $1/\sqrt{L_g(C_{gs1}+C_{gs3})}$ and the Q-factor of a complex-conjugate pole pair is equal to:

$$Q = \sqrt{\frac{L_g}{R_g{}^2(C_{gs1}+C_{gs3})}} \tag{10}$$

It can be seen that with this inductor L_g addition potential bandwidth enhancement can be achieved. Fig. 2 shows the simulation results of the voltage gain for different values of the gate inductor L_g. For an increasing value of inductor L_g, the bandwidth of the amplifier is improved. However, based on the expression for bandwidth in terms of Q-factor and resonant frequency, $BW=\omega_0/Q$, exceeding a certain value of the inductance, the peaking becomes severe and the bandwidth starts to degrade.

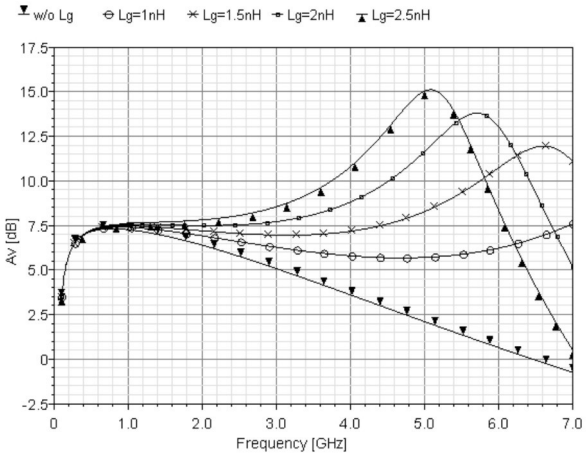


Figure 2: Simulation results of the voltage gain for different L_g values.

For the proposed design the optimum inductance value of L_g is found to be 2.3 nH. With this value the LNA covers the frequency band from 3.1 to 5 GHz with 1.82 dB variation in S_{21} parameter.

4.2 Influence of capacitor C_F on impedance matching

The input impedance of the proposed LNA is given by:

$$Z_{in} = \frac{Z_F+\frac{1+j\omega C_{gs6}R_L}{g_{m6}+j\omega C_{gs6}}}{1+|A_{v1}|} \,||\, \frac{1-\omega^2(C_{gs1}+C_{gs3})L_g}{j\omega(C_{gs1}+C_{gs3})} \tag{11}$$

where C_{gs6} and g_{m6} are the gate-source capacitance and the transconductance of the source-follower transistor M_6, respectively. The real and imaginary parts of the input impedance are examined, as shown in Figs. 3 and 4.

From Figs. 3 and 4 it can be seen that the input impedance is determined by two equivalent subcircuits. At low frequencies the parallel resonant circuit with resonant frequency around 4 GHz shows the dominant effect on overall LNA impedance. Below this frequency the parallel RLC circuit has inductive and beyond it capacitive character, as shown in Fig. 4. From the expression for the output impedance of the source follower, given by

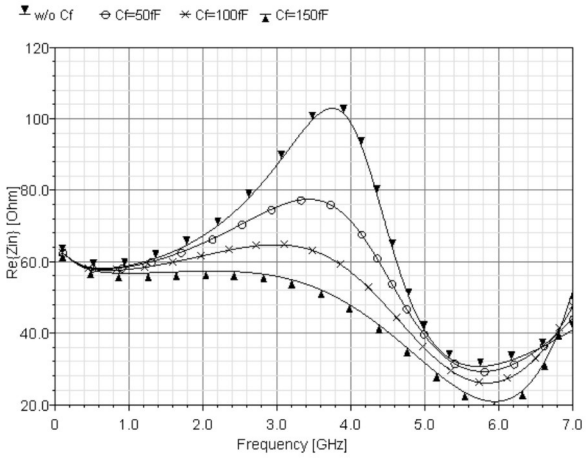


Figure 3: Simulation results of the real part of the input impedance for different C_F values.

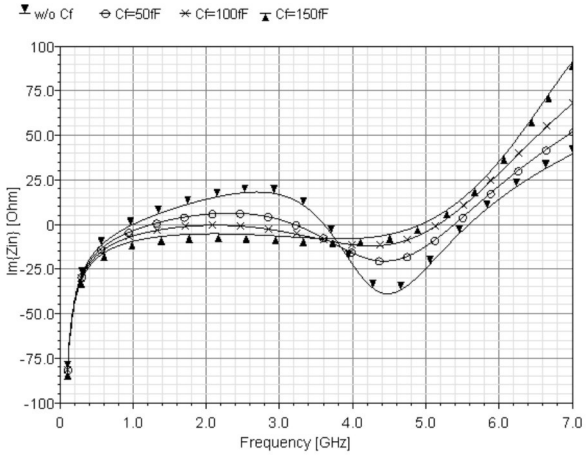


Figure 4: Simulation results of the imaginary part of the input impedance for different C_F values.

$$Z_{out} = \frac{1 + j\omega R_L C_{gs6}}{g_{m6} + j\omega C_{gs6}} \tag{12}$$

it can be observed that by increasing the frequency, for $1/g_{m6} < R_L$, the impedance of the source follower shows inductive behavior. Based on the method presented in [11], this impedance can be represented as a parallel LR_1 circuit connected in series with a resistor R_2. The component values can be obtained as:

$$L = \frac{j\omega C_{gs6}}{g_{m6}}\left(R_L - \frac{1}{g_{m6}}\right) \tag{13}$$

$$R_1 = R_L - \frac{1}{g_{m6}} \tag{14}$$

$$R_2 = \frac{1}{g_{m6}} \tag{15}$$

This inductance forms a parallel resonant circuit together with the input capacitances C_{gs1} and C_{gs3}. By adding capacitor C_F in parallel to feedback resistor R_F, the real component of the feedback impedance is reduced, given by (6), and comes closer to ideal 50 Ω, as shown in Fig. 3. In addition based on (11) the capacitive effect is increased by A_{v1}, which decreases the imaginary part closer to zero and, therefore, improve input impedance matching. Consequently, the parameter S_{11} is improved, as shown in Fig. 5.

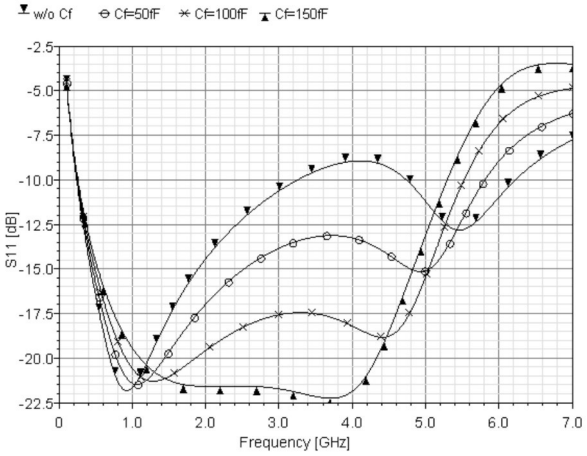


Figure 5: Simulation results of the S_{11} parameter for different C_F values.

At high frequencies the influence of the serial resonant circuit, formed by inductor L_g and input capacitances of transistors M_1 and M_3, can be seen with resonant frequency at 6 GHz given by:

$$\omega_0 = \frac{1}{\sqrt{L_g\left(C_{gs1} + C_{gs3}\right)}} \tag{16}$$

The influence of capacitor C_F can be seen from Figs. 3 and 4, as a reduction of the input impedance real part. As before, capacitor C_F decreases the feedback impedance for increasing frequency. The imaginary part of the input impedance will start to increase with frequency as a result of inductive behaviour.

4.3 Noise analysis

At high frequencies the noise is white, but at low frequencies the power spectral density is inversely proportional to the frequency.

For transistors in the proposed LNA, it was found that the flicker noise (1/f) corner frequency is around 10 MHz, which is in accordance with the data given in Process Design Kit (PDK) for 0.18 µm CMOS technology. From simulation it was found that 1/f noise of the LNA

is mainly contributed by the input amplifying NMOS transistor M_1 (14.55 %), with the W_1 = 105 µm.

The noise factors of the most important thermal noise sources of the LNA, under input impedance matched condition and not considering a gain boosting stage, are derived as:

$$F_{RL} \approx \frac{1}{g_{m1}{}^2 R_L R_S} \tag{17}$$

$$F_{RF} \approx \frac{R_F}{g_{m1}{}^2 R_L{}^2 R_S} \tag{18}$$

$$F_{M1} \approx \frac{1}{g_{m1} R_S} \frac{\gamma_1}{\alpha_1} \tag{19}$$

$$F_{M6} \approx \frac{1}{g_{m6} R_S} \left(\frac{1}{g_{m1} R_L} \right)^2 \frac{\gamma_6}{\alpha_6} \tag{20}$$

where F_{RL}, F_{RF}, F_{M1}, and F_{M6} stand for the noise factors due to thermal noises of the load resistor R_L, the feedback resistor R_F, the amplifying transistor M_1, and the source follower transistor M_8, respectively. R_S is the input source resistance, γ is the MOSFET's thermal noise coefficient, and parameter α describes g_m/g_{d0} ratio, where g_{d0} is the drain-source conductance at zero V_{DS}. The total noise factor of the LNA is given as:

$$F = 1 + F_{RL} + F_{RF} + F_{M1} + F_{M6} \tag{21}$$

In the final LNA design, transistor M_3 is added to enhance transconductance of input transistor M_1, so lower value of noise factor can be achieved, as can be seen from (17)–(20). Consequently, a lower current flows through resistor R_L providing some additional increase of R_L for the same voltage headroom, but a smaller bandwidth. During the design procedure trade-offs among power consumption, BW, input impedance matching and NF are performed.

5 Measurement and simulation results

The proposed LNA circuit was designed and implemented in UMC 0.18 µm twin-well CMOS technology with supply voltage V_{DD} = 1.8 V.

Simulations were obtained by using Cadence Design System with Spectre device models for all components. Post-layout simulations were performed using Assura, Cadence parasitic extractions tool. Transistor models are realized as multi-finger structures with 0.18 µm fixed gate length. The information about transistor widths is presented is Table 1, while values of passive components used in the circuit are given in Table 2. The bulks of all NMOS/PMOS transistors are connected to adequate reference voltages (GND in case of NMOS, and V_{DD} in case of PMOS transistors), as shown in Fig. 1.

Table 1: Transistors widths (W), L = 0.18 µm.

Devices	$M_{1,4,9}$ [µm]	$M_{3,6}$ [µm]	$M_{2,10}$ [µm]	M_{15} [µm]	M_5 [µm]	$M_{7,8,11-14}$ [µm]
Design values	21 × 5	13 × 5	11 × 5	9 × 5	7 × 5	5 × 5

Table 2: Values of passive circuit components.

Devices	R_F [Ω]	R_L,R_{d4} [Ω]	$Rd_{1,3}$ [Ω]	R_{d2} [kΩ]	R_{d5} [Ω]	L_g [nH]	C_1 [pF]	$C_{2,3}$ [pF]	$C_{4,5}$ [pF]	C_F [fF]
Design values	219.8	136.6	719.7	3	317.7	2.3	4.9	4	2	119.9

A die microphotograph of the proposed LNA circuit is shown in Fig. 6. Using only one inductor in the LNA design, the chip area is greatly reduced and measures 1.251×0.729 mm^2. The active area, which excludes the pads, is approximately 0.919×0.384 mm^2.

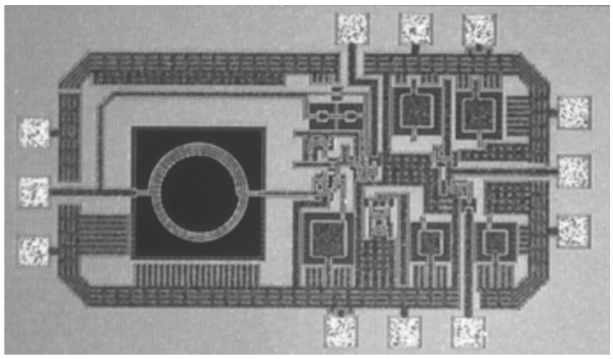
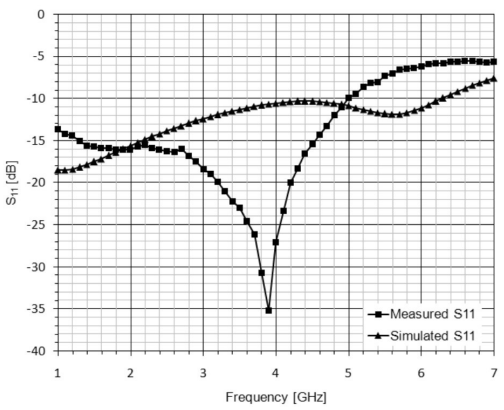


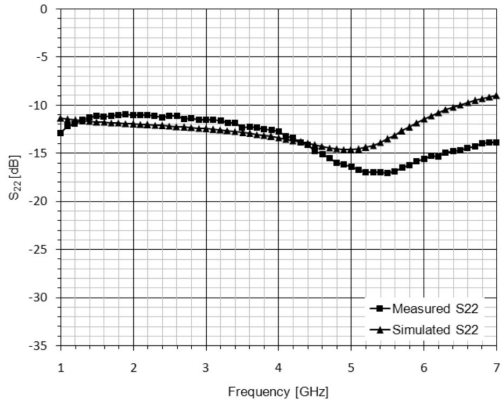
Figure 6: Die microphotograph of the designed LNA.

On-wafer probing under a 1.8 V supply voltage was performed to characterize the circuit performance of the LNA. The S-parameters were measured by using a Rohde & Schwarz ZVM Vector Network Analyzer. Fig. 7 shows the measured S_{11}, S_{22}, S_{21}, and S_{12} parameters along with the simulation results. The measured input return loss (S_{11}) is better than –10 dB for the frequency range from 1 to 5 GHz. The discrepancy between simulation and test results is mainly attributed to the additional parasitic effects. Over the entire frequency band of interest (3.1–5 GHz), the measured output return loss (S_{22}) and the measured isolation (S_{12}) remain below –11.52 dB and –36.07 dB, respectively. Fig. 7(c) shows the measured power gain (S_{21}) versus frequency. The LNA achieves a high S_{21} of 9.7±0.45 dB over the 3.1–5 GHz band, and a 3-dB bandwidth from 1.11 to 5.57 GHz.

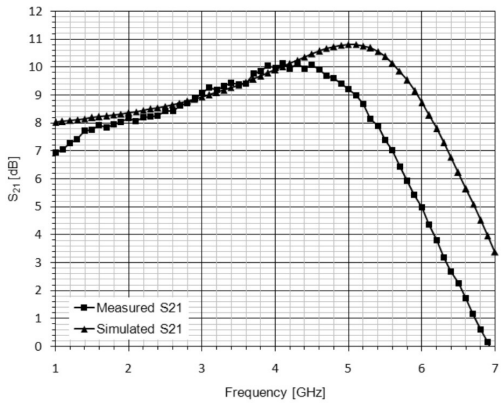
(a)



(b)



(c)



(d)

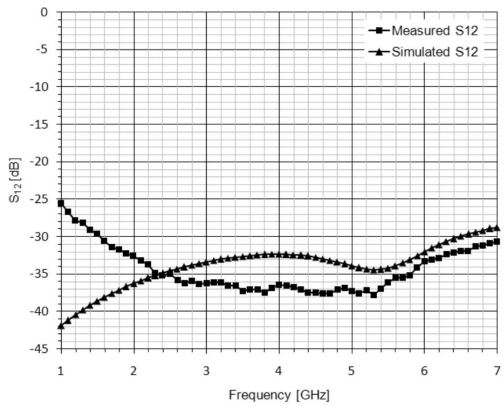


Figure 7: Measurement and simulation results: (a) S_{11} parameter, (b) S_{22} parameter, (c) S_{21} parameter, (d) S_{12} parameter.

The post-layout simulation result for the noise figure (*NF*) is shown in Fig. 8. It can be seen that the parameter value varies from 4.42 dB at 3.1 GHz to 4.06 dB at 5 GHz, with a minimum of 4.05 dB at 4.92 GHz.

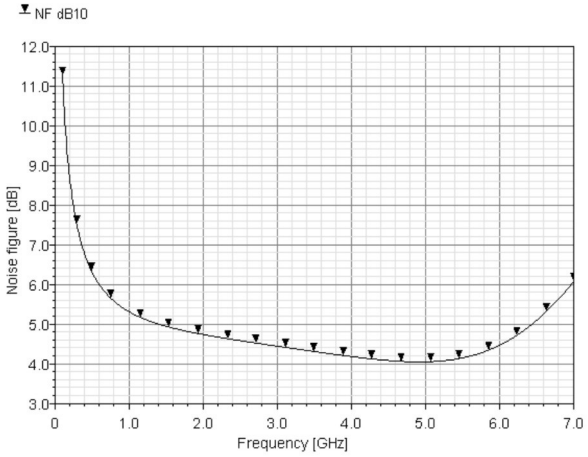


Figure 8: Post-layout simulation results: Noise figure (*NF*).

The linearity of the proposed LNA was characterized measuring the 1-dB compression point using a Rohde& Schwarz Spectrum Analyzer FSP 30. An Hewlett Packard Network Analyzer 8753E, was used as an input source for varying the input power from –35 to 0 dBm. Due to its limitation in the frequency range, the linearity was measured only at 3 GHz. Measurements were performed for five LNA samples, and the results range from –9.5 to –11.5 dBm. Average result is plotted in Fig. 9.

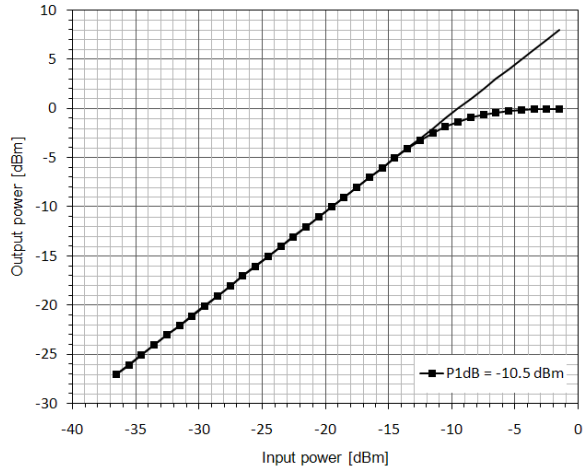


Figure 9: Measured results: 1-dB compression point.

The use of source-follower as LNA output stage leads to amplifier linearity degradation. The additional source follower in the feedback circuit further decreases 1-dB compression point. Despite this, proposed LNA meets the linearity requirements for the UWB amplifier design and shows better linearity performance than other re-

ported amplifiers designed in 0.18 µm technologies, which in addition use more complex circuit designs and increase costs.

A common measure for phase linearity is the group delay, defined as the derivation of the transfer function S_{21} phase. The measured maximum group delay variation of the proposed LNA is ±34.59 ps across the 3.1–5 GHz band. By definition, a group delay variation of less than ±10 % of the bit period over the specified bandwidth is required to limit the generation of data dependent jitter [12]. This corresponds to maximum possible bit period of 345.9 s, i.e. bit rate up to 2.89 Gb/s. Thus, proposed LNA shows good phase linearity.

The stability of the LNA is determined by the Rollett stability factor K and the auxiliary stability factor B_1. Minimum values of K and B_1 are 3.66 and 0.94, respectively, hence unconditional stability requirements, given by $K > 1$ and $B_1 > 0$ [13], are satisfied. In addition, the geometric stability factors of an amplifier are calculated. The µ (Mu) and µ' (Mu-prime) factors are so called load stability factor and source stability factor, respectively. A two port network is unconditionally stable if $\mu > 1$ or $\mu' > 1$ [14], which means that with any load presented to the input or to the output of the device, the circuit will not become unstable. Furthermore, it can be said that larger values of µ and µ' imply greater stability. The stability factors of the proposed UWB LNA are calculated for all frequencies where the device is able to provide a gain larger that unity. The measured results are shown in Fig. 10. It can be noticed, that LNA circuit is stable for all frequencies, up to 10 GHz.

The current consumption of the LNA was measured with a Keithley 2000 Multimeter. The LNA's total core current is 5.54 mA. Taking the currents drawn by the bias circuits and the output buffer into consideration, the LNA dissipates a total of 28.54 mW from a 1.8 V supply.

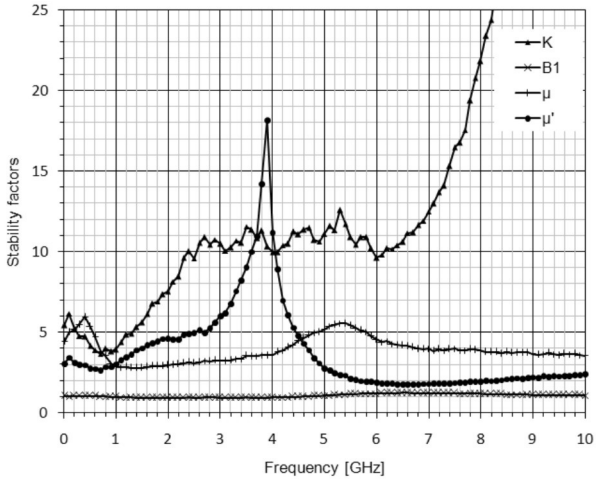


Figure 10: Measured results: Stability factors.

To provide a certain level of controllability, separated pins are added in the design for supply voltages V_{bias_sf1}, V_{bias_sf2}, and V_{bias_n}. By decreasing these voltages (they are nominally set to 1.8 V), S-parameters and noise figure characteristics are affected. Post-layout simulation results are shown in Figs. 11–13.

By changing the voltage V_{bias_sf1} from 1.8 to 1 V, the gate-source voltage of transistor M_7, V_{gs7}, and consequently the gate-source voltage of transistor M_1, V_{gs1}, is increased. A higher V_{gs1} voltage results in a larger transconductance value g_{m1} and leads to S_{21} increase. Additionally, due to higher output resistance the low-frequency gain increases and peaking is less pronounced. According to the (4), input impedance value decreases and diverges from 50 Ω, which leads to a higher parameter S_{11} value. Furthermore, voltage V_{bias_sf1} variations result in minor S_{22} change and slight increase of *NF*. Decrease in voltage V_{bias_n} value influences transistor M_2 biasing point, thus decreasing the overall gain of the amplifier up to 1dB. As a result, input impedance value, given by (11), increases and S_{11} parameter degrades. The voltage V_{bias_sf2} variations affect output impedance matching. For V_{bias_sf2} = 1 V, the output resistances of transistors M_9 and M_{10} increase. As a result, the LNA's output impedance changes, which leads to S_{22}, and consequently, S_{21} decrease.

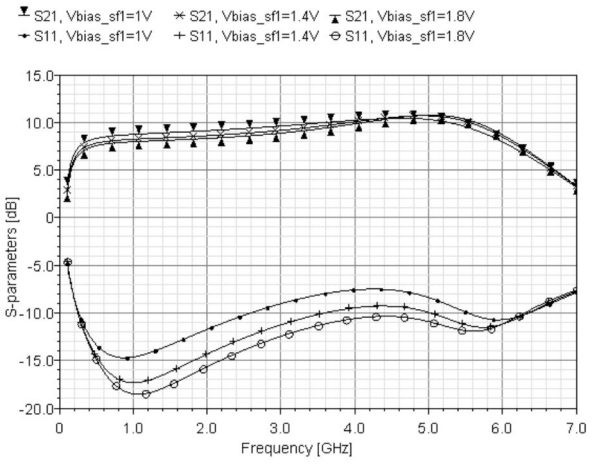


Figure 11: Post-layout simulation results: Simulated S_{11} and S_{21} when varying V_{bias_sf1} in the range from 1 to 1.8 V, with 0.4 V step.

Table 3 summarizes the measurement results of the proposed LNA compared to the FoMs of the recently published works. The design presented in this paper shows low variation of gain and noise in the 3.1–5 GHz band. As the main drawback of selected low cost 0.18 µm technology are inductors, that occupy a large area, by reducing their number to one, the chip area is greatly reduced and comparable to the area occupied by other designs, implemented in different 0.18 µm technolo-

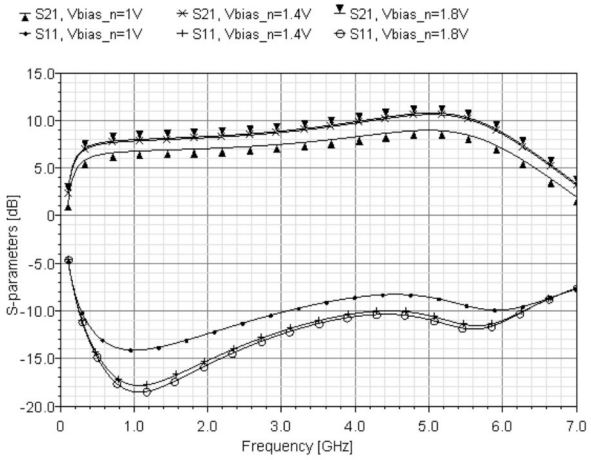


Figure 12: Post-layout simulation results: Simulated S_{11} and S_{21} when varying V_{bias_n} in the range from 1 to 1.8 V, with 0.4 V step.

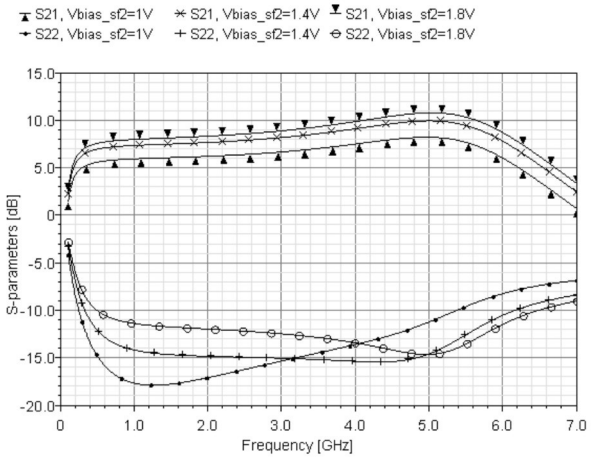


Figure 13: Post-layout simulation results: Simulated S_{22} and S_{21} when varying V_{bias_sf2} in the range from 1 to 1.8 V, with 0.4 V step.

gies. For example, the LNA topologies presented in [15] and [16] use four inductors, in [17] and [18] three, and in [19] five. Consequently, the small number of inductors in LNA design reduces the degrees of freedom, so additional techniques need to be used to meet requirements for all LNA FoMs. From Table 3 follows that parameters achieved in the presented paper are comparable to the results given by other authors, making the proposed architecture suitable for UWB wireless applications.

6 Conclusion

The proposed LNA is designed for lower UWB band from 3.1 to 5 GHz. By utilizing only one inductor placed inside the feedback loop, a compact layout design in low cost UMC 0.18 µm CMOS technology is presented. Therefore, proposed design is comparable with the other reported designs implemented in different technologies. To meet other LNA requirements different techniques are used. The amplifier employs the feedback resistor connected through a source follower, which leads to a wider operating frequency range and improved voltage headroom of the amplifier. In addition, the drain current of the cascode transistor is reduced by adding the PMOS transistor to form a current-reuse topology with the amplifying transistor. Consequently, the effective transconductance is enhanced, leading to high gain values. By adding feedback capacitor in parallel to feedback resistor, the input impedance is kept constant with frequency and wideband input impedance matching is obtained. The simulation and measurement results show low gain and noise variations in the band of interest, from 3.1 to 5 GHz, while satisfying the input and the output matching conditions and the power consumption requirements. Good power and phase linearity performances make the proposed LNA suitable for both OFDM and UWB impulse radio system applications.

Acknowledgments

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Table 3: Performance comparison of LNAs implemented in 0.18 µm technologies.

Ref.	BW [GHz]	S_{21} [dB]	S_{11} [dB]	S_{22} [dB]	NF [dB]	P_{1dB} [dBm]	P_D [mA@V]	Die area [mm^2]
/15/	3–5	12.7±0.4	<–13	<–10	3.2–5.5	–11.7	9.6*@ 1.8	0.7
/16/	3–4.8	13.5±1.5	<–10	/	3.5–6.8	–18	3.7*@ 0.9–1.8	0.76
/17/	3–7	10±1.5	<–11	<–11	3.5–4	/	5 @ 1.8	0.59
/18/	0.6–6.2	10.1±1.5	<–21	<–22	5.3–5.8	–13	5.6 @ 1.5	0.8
/19/	2–6	12.5±0.5	<–10	/	3–3.7	/	8.3 @ 1.8	0.98
This work	3.1–5	9.7±0.4	<–10	<–11	4–4.4**	–9.5	5.5*@ 1.8	0.91

*LNA core **simulated

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