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Sneak path current equivalent circuits and reading margin analysis of complementary resistive switches based 3D stacking crossbar memories

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Abstract: Sneak path currents of resistive memories is an important issue. They increase with increasing memory size and should be minimized for a usable resistive memory. The complementary resistive cells have been suggested as an alternative to one-cell resistive memories to decrease leakage currents. In literature, multilayer resistive memory topologies have also been inspected to minimize leakage currents. Recently, feasibility of 3D resistive RAMs is also inspected. However, to the best of our knowledge, no one has given equivalent leakage circuit models for complementary resistive switches based 3D resistive RAMs yet. In this study, equivalent leakage circuit models for different layers of a 3D resistive RAM with complementary resistive cells have been given and their leakage resistance and reading margins are compared to that of one layer crossbar memory. Some interesting and crucial results are obtained. Alternative complementary resistive switches based 3D resistive RAM topologies with insulating layer(s) for minimized leakage currents are suggested.

Keywords: Complementary Resistive Switches, 3D Multilayer Resistive RAM, Crossbar Memory, Sneak Path Currents.

Nadomestna električna vezja za analizo kvarnih tokov in analiza bralne meje pri komplementarnih uporovnih stikalih na osnovi 3-D večplastnih križnih pomnilnikov

Izvleček: Velik problem uporovnih pomnilnikov predstavljajo kvarni tokovi, ki se, z večanjem pomnilnika, povečujejo. Za zmanjševanje uhajalnih kvarnih tokov so, kot alternativa enoceličnim uporovnim pomnilnikom, predlagane komplementarne uporovne celice. Nadalje lahko v literaturi, za zmanjševanje uhajalnih tokov, zasledimo večplastne uporovne pomnilniške topologije. Trenutno se raziskuje tudi 3D uporovne pomnilnike. Glede na naše znanje, trenutno nihče še ni uspel podati ekvivalentnega vezja za 3D uporovne pomnilnike na osnovi komplementarnih uporovnih stikal. V tem delu je podano ekvivalentno vezje kvarnih uhajalnih tokov za različne plasti 3D uporovnega pomnilnika s komplementarnimi uporovnimi celicami in primerjava uhajalne upornosti ter bralne meje tega koncepta in enoslojnega križnega pomnilnika. Dobljeni so bili zanimivi in odločilni rezultati. Za minimiziranje uhajalnih tokov so predlagani alternativni 3D uporovni pomnilniki s komplementarnimi uporovnimi stikali in izolacijskimi plastmi.

Ključne besede: komplementarna uporovna stikala, 3D večplastni uporovni pomnilniki, križni pomnilniki, kvarni tokovi

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1 Introduction

Resistive switch memories are also memristive devices and they are under consideration for non-traditional memory applications [1 – 3]. Resistive switch memories may help to speed up the booting of computers, reducing their energy consumption and open the way for high density memories. Optimization and minimization of their leakage current and power consumption has emerged as an exciting new research area [4, 5]. Complementary resistive switching (CRS) memories have been suggested to minimize leakage currents in [6, 7]. Multilayer resistive memories are suggested so that the decreased number of cells in the selected layer results in less leakage current. 3D multilayer crossbar array memories are also suggested to maximize memory density [8 – 12]. Previously, 3D multilayer crossbar array memories with CRS cells are considered and their leakage is examined using simulations [10, 11, 13]. However, to the best of our knowledge, no equivalent circuit model for their leakage paths does exist in the literature yet. In this study, for the first time in literature, leakage equivalent circuits of a CRS based 3D Resistive RAM (CB-3D-ReRAM) have been given and leakage resistances and reading margin of one layer and CB-3D-ReRAM leakage currents are compared using the equivalent circuits.

The paper is arranged as follows. In the second section, a CRS cell is briefly explained. In the third section, equivalent leakage circuit of one layer CRS based quadratic memory is given. In the fourth section, the CB-3D-ReRAM is briefly explained and its equivalent circuits for reading a cell at the bottom, the top and middle layers are given. In the fifth section, comparison of leakage resistance and reading margin for different layers of CB-3D-ReRAM to that of a one layer quadratic memory are given using the ratio of the maximum CRS resistance to the minimum CRS resistance when both memories have the same size. In the sixth section, alternative CB-3D-ReRAM topologies with insulating layers are suggested to minimize leakage currents. The paper is finished with conclusion section.

2 Complementary Resistive Switches

Anti-series connected resistive switches are called complementary resistive switches and used to minimize leakage currents in crossbar arrays. A detailed explanation for CRS topology can be found in [6]. The CRS cell model in [6] is also used within this study and redrawn in Figure 1. A resistive switch can be made of a solid electrolyte sandwiched between copper and platinum electrodes as shown in Figure 1.a. The lower resistive switch consists of the copper contact, the bottom solid electrolyte and the bottom platinum contact. The upper resistive switch consists of the upper platinum contact, the upper solid electrolyte and the copper contact. When the CRS is exited by an AC voltage, its zero-crossing hysteresis loop is shown in Figure 1.b.

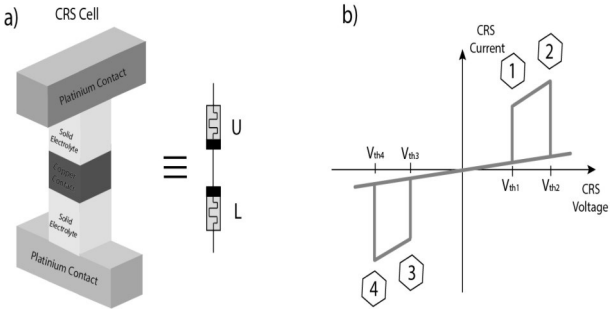

Figure 1: a) The CRS, which is made of the anti - series connected memristive elements or resistive switches U and L, b) Idealized zero crossing current - voltage hysteresis loop of the CRS cell.

If a resistive switch or a memristive element has a high resistance, it is in high resistance state (HRS) and, if it has a low resistance, it is in low resistance state (LRS). When the resistive switch U is in HRS and the resistive switch L is in LRS, the CRS state is logic 0. If the resistive switch U is in LRS and the resistive switch L is in HRS, the CRS state is logic 1. R_{ON} and R_{OFF} are the maximum and the minimum CRS resistances respectively. They are given as

$$R_{OFF} = R_{HRS} + R_{LRS} \tag{1}$$

And

$$R_{ON} = R_{LRS} + R_{LRS} \tag{2}$$

Where
R_{HRS} is the maximum resistance of a CRS switch (either U or L).
R_{LRS} is the minimum resistance of a CRS switch (either U or L).

The maximum CRS resistance, R_{OFF}, is a little higher than R_{HRS} and almost equal to R_{HRS} because of the high ratio between R_{HRS} and R_{LRS}. In [6], it has been shown that, under its threshold voltage, a CRS cell behaves as if a linear resistor with a resistance value of R_{OFF}. When a voltage whose magnitude less than the threshold voltage V_{th1} is applied and it draws a low current and does not switch its state as shown in Figure 1.b.

Reading a CRS cell of logic 1 destroys the cell state and it should be rewritten again [6]. However, the states of the CRS cells in sneak path are not destroyed. Using the CRS model, reading margin and leakage resistance of a

one layer quadratic memory and a CB-3D-ReRAM will be inspected in the next section and the fourth section respectively.

3 The equivalent leakage circuit of a CRS based of one-layer quadratic memory

A CRS based one layer NxN quadratic crossbar memory is shown in Figures 2 and 3. Its equivalent leakage circuit, given in [11,13], is shown in Figure 4. In Figure 4, R_{sel} is the selected cell resistance, R_{pu} is the pull-up resistor, and R_{leak} is the equivalent leakage resistance of one layer crossbar memory. The row number of the memory is designated as N and is equal to the column number of the memory. Equivalent leakage resistance decreases with increasing memory size (N^2) and it is given as

$$R_{Leak} = \frac{(2N-1).R_{OFF}}{(N-1)^2} \tag{3}$$

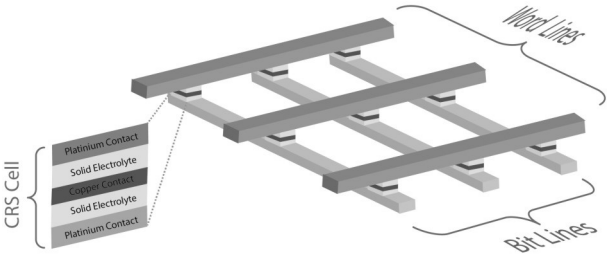

Figure 2: One layer quadratic memory with CRS.

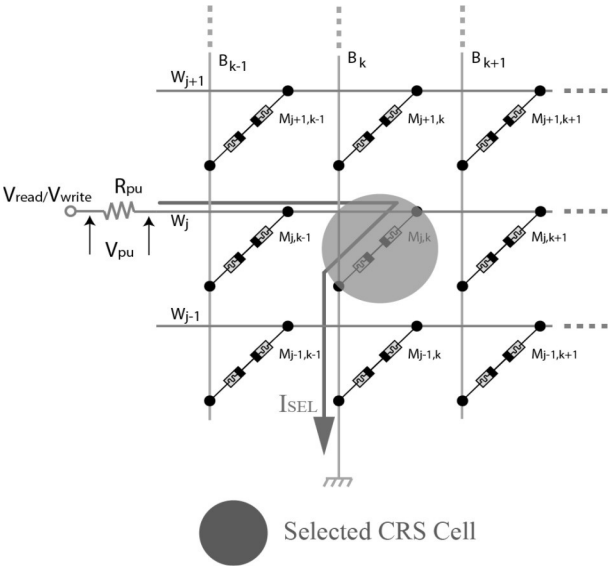

Figure 3: Reading a cell of a CRS based one layer quadratic memory. The reading voltage is applied to the row, W_j, and the column, B_k.

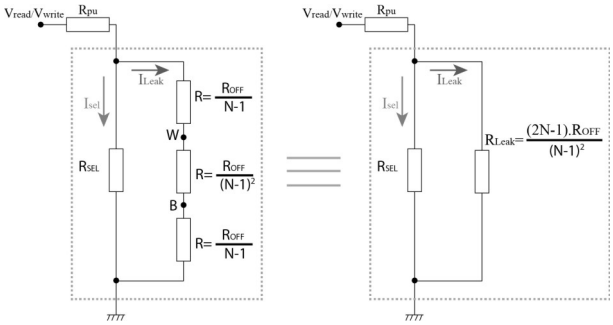

Figure 4: Equivalent circuit of a CRS crossbar array [11,13].

4 A CRS based 3D resistive RAM and its equivalent leakage circuits for different layers

A CB-3D-ReRAM structure is shown in Figure 5. It has L layers. It has either common rows or common columns between adjacent layers. Neighboring layers are constructed in an inverted manner. If only one cell at a layer is read at a time, that the top and the bottom layers shown in Figure 6 must have the same leakage because of symmetry. The equivalent circuit of an L layer CB-3D-ReRAM for reading/writing a cell which is at either the top or the bottom layers is shown in Figure 6. Its leakage resistance is found as

$$R_{Leak} = \frac{(3N-1).R_{OFF}}{(N-1).(2N-1)} \tag{4}$$

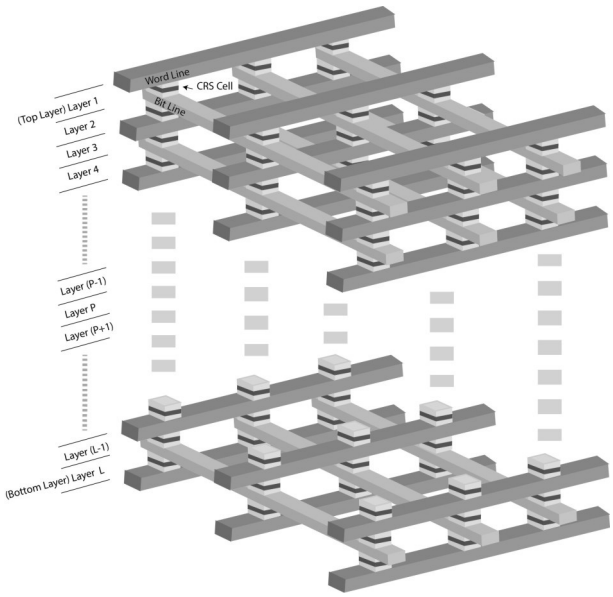

Figure 5: A CB-3D-ReRAM structure.

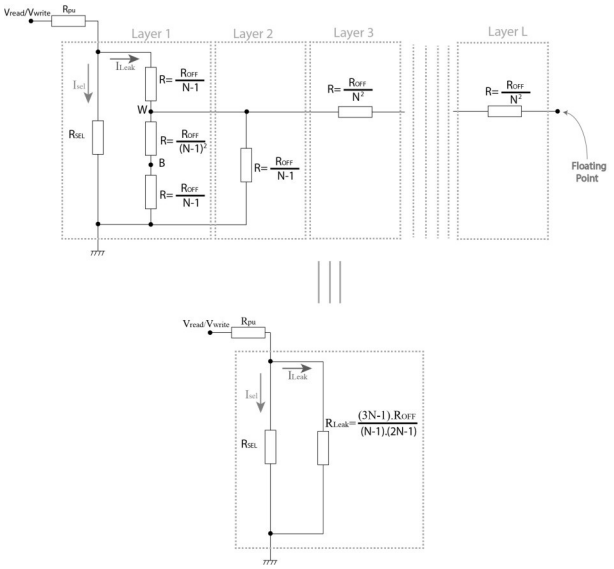

Figure 6: Equivalent circuit of the CB-3D-ReRAM with L layers when a cell at the top or the bottom layer is read / written.

It can be said that the reason of increasing number of layers not increasing sneak-path currents so much is the rest of unselected rows and columns have floating potentials and behave as equipotential surfaces.

If a cell at a middle layer of the CB-3D-ReRAM is read ($2 \le P < L$), its equivalent leakage circuit is shown in Figure 7. Its leakage resistance is found as

$$R_{Leak} = \frac{R_{OFF}}{(N-1)} \tag{5}$$

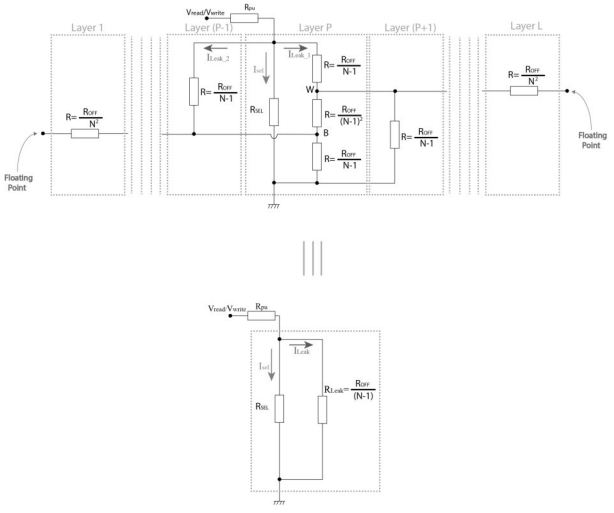

Figure 7: Equivalent circuit of the CB-3D-ReRAM when a cell at layer P, is read. For a middle layer: $2 \le P < L$.

5 Comparison of leakage resistance and reading margin for different layers of the CB-3D-ReRAM to that of one layer quadratic memory

Equivalent leakage circuits of the different layers of the CB-3D-ReRAM are given in the previous section. The equivalent leakage resistances of one layer quadratic memory, the top, the bottom and the middle layers of the CB-3D-ReRAM are calculated and then normalized by the maximum CRS resistance. The normalized leakage resistances are shown in Figure 8. One layer quadratic memory has highest leakage resistance (the least leakage current). The middle layer of CB-3D-ReRAM has the lowest leakage resistance (the worst leakage current). The leakage resistance of the top layer of the CB-3D-ReRAM is same as that of the bottom layer. It is higher than that of a middle layer of the CB-3D-ReRAM and less than that of one layer quadratic memory. If N>>1, Eq. (3) can be approximated as

$$R_{Leak} \cong \frac{2R_{OFF}}{N} \tag{6}$$

If N>>1, Eq. (4) can be assumed as equal to

$$R_{Leak} \cong \frac{3R_{OFF}}{2N} \tag{7}$$

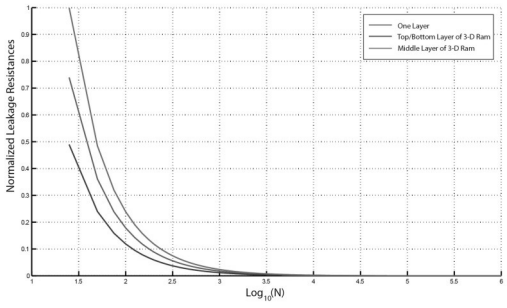

Figure 8: Leakage resistances normalized by the maximum CRS resistance.

If N>>1, Eq. (7) is only 25% less than the leakage resistance of one layer quadratic memory with CRS of the same size. V_{pu}, which is the voltage across the pull-up resistor R_{pu}, can be found as

$$V_{pu} = \frac{R_{pu}}{R_{pu} + R_{leak} // R_{sel}} V_{read} \tag{8}$$

In this study, the pull-up resistor is chosen to be equal to R_{ON} and the reading margin is defined as

$$\Delta V = \frac{V_{min} - V_{max}}{V_{read}} \quad (9)$$

Where
V_{min} is the voltage across the pull-up resistor R_{pu} when the cell has minimum resistance.
V_{max} is the voltage across the pull-up resistor R_{pu} when the cell has maximum resistance.
V_{read} is the reading voltage.

Reading margins of an NxN one layer quadratic memory and the top/the bottom layer and a middle layer of an NxN CB-3D-ReRAM are calculated shown in Figure 9. The ratio of the maximum CRS resistance to the minimum CRS resistance, R_{OFF}/R_{ON} is used as a parameter for all the drawings to show that both the reading margin and the leakage resistance go up when R_{OFF}/R_{ON} increases. For the same size, one layer quadratic memory has the highest (the best) reading margin, the reading margin of a middle layer of the CB-3D-ReRAM has the worst reading margin, the reading margin of the top layer of the CB-3D-ReRAM is same as that of the bottom layer of the CB-3D-ReRAM and it is higher than that of a middle layer and less than that of one layer quadratic memory. After all, if the same memory size is divided into layers, the CB-3D-ReRAM becomes advantageous. As an example, the memory size is chosen to be 4 Mbit for both the CB-3D-ReRAM and one layer quadratic memory. The layer numbers of the CB-3D-ReRAM can be chosen to be 4, 16, and 64. As a function of the layer numbers, the reading margins are shown in Figure 10. The leakage resistances normalized by the maximum top layer leakage resistance are shown in Figure 11. Increasing the layer number results in a less leakage current for the CB-3D-ReRAM than that for one layer quadratic memory or a higher leakage resistance than that for quadratic memory for the same memory size as shown in Figure 11, the CB-3D-ReRAM shows a better performance for the same memory size but it is difficult to construct. On the other hand, it would increase both reading margin and leakage resistance, it is not practical to make the layer number higher than necessary considering manufacturing difficulties and cost issues. Accordingly, for the same memory size, it could be preferable to choose the number of layers of the CB-3D-ReRAM is 4 instead of 16 or 64.

6 Alternative CB - 3D - ReRAM Topology Suggestions

Based on the findings of the last sections, alternative CB-3D-ReRAM topologies with insulating layer(s) can be suggested considering that insulating layers are going to less expensive in the future. Since the top and the bottom layers have higher equivalent leakage resistance than the middle layers with only one cell selected for reading, the number of the middle layers must be minimized for less leakage current during

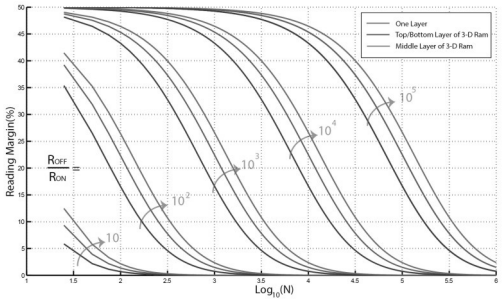

Figure 9: Reading margins of the top or the bottom layer of the CB-3D-ReRAM, a middle layer of the CB-3D-ReRAM, and a one layer quadratic memory.

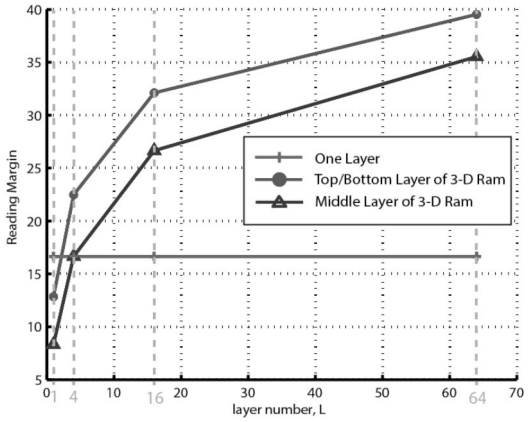

Figure 10: Reading margins of the CB-3D-ReRAM layers and one layer quadratic memory for the memory size,N^2,= 4 Mbit and R_{OFF}/R_{ON}=1000.

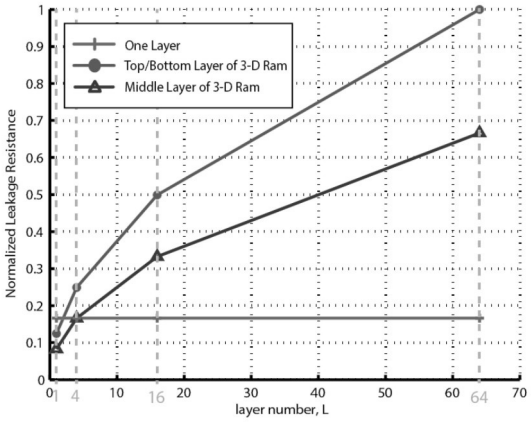

Figure 11: Normalized leakage resistances of the CB-3D-ReRAM layers and one layer quadratic memory when the memory size, N^2, = 4 Mbit and R_{OFF}/R_{ON}=1000.

operation. The suggested new topologies are shown in Figures 12–14. The 3D RAM topology seen in Figure 12 is obtained placing one insulating layer after every other two layers, there is one insulating layer between two layers. As a result, it has the lowest leakage during its operation since it does not have any middle layers. Still, it needs insulating layers whose number are almost half of the crossbar layers and it might be the most expensive to produce among the topologies shown in Figures 12–14.

The 3D RAM topology seen in Figure 13 is obtained placing one insulating layer after every other three layers, there is one insulating layer between three layers. For it has only one middle layer, its leakage current increases if the middle layer is read or written. Otherwise, its leakage is same as that of the topology given in Figure 12. If the topology is used, it has less insulating layers than that of the one in Figure 12 for a high number of crossbar layers. However, it has a higher leakage current with a probability of 1/3. The 3D RAM topology seen in Figure 14 is obtained placing one insulating layer after every other four layers, there is one insulating layer between four layers. Since it has only two middle layers, its leakage current increases if the middle layers are read or written. Otherwise, its leakage current is same as that of the topology given in Figure 12. If the topology is used, it has the least insulating layer among the ones given in Figures 12–14 for a high number of crossbar layers. Yet, it has a higher leakage current with a probability of 1/2.

If the technique to make insulating layers become easier and less expensive, the results of the analyses done in this study can be used to develop new CB-3D-ReRAM topologies with less leakage current and higher reading margin.

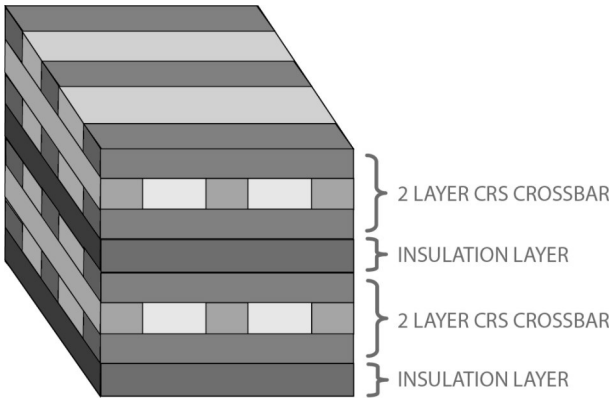

Figure 12: An alternative topology obtained placing one insulating layer after every other two layers, there is one insulating layer between two layers.

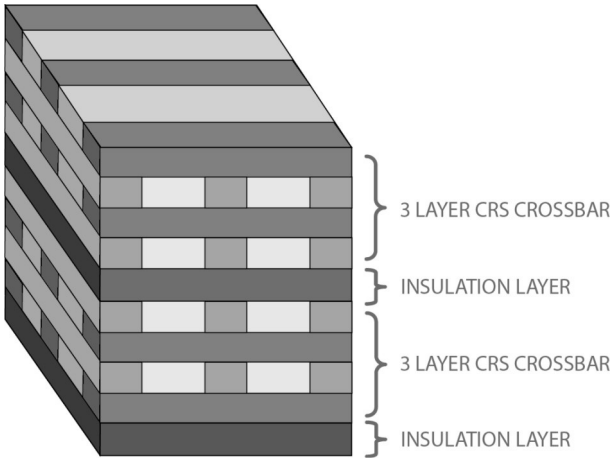

Figure 13: An alternative topology obtained placing one insulating layer after every other three layers, there is one insulating layer between three layers.

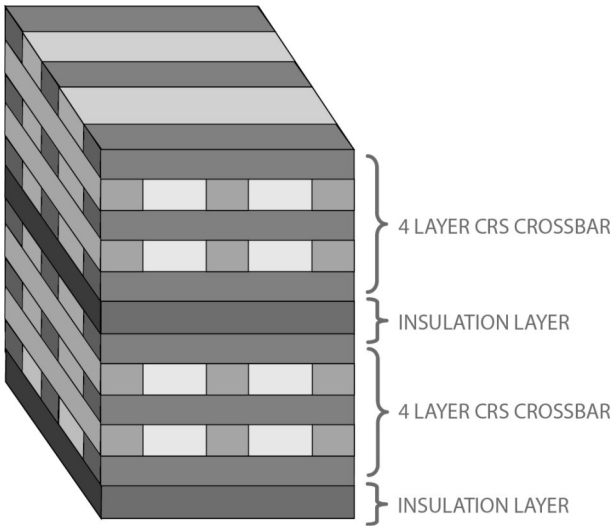

Figure 14: An alternative topology obtained placing one insulating layer after every other four layers, there is one insulating layer between four layers.

7 Conclusion

Leakage resistances of different layers of a CB-3D-ReRAM are examined using the equivalent circuits. It has been found that reading a cell at the top or the bottom layers of the CB-3D-ReRAM results in less leakage current than reading a cell at middle layers of the CB-3D-ReRAM. Leakage currents are same for all middle layers of the CB-3D-ReRAM. Leakage current of an NxN one layer quadratic memory is less than that of an L layer NxN CB-3D-ReRAM. However, the L layer memory array has less leakage current than a one layer quadratic memory for the same memory size when the layer number is more than or equal to four. Results show that the CB-3D-ReRAM for the same memory size and using

just a few layers is a promising candidate for the future memories.

Alternative CB-3D-ReRAM topologies with insulating layers are also suggested to minimize leakage currents during operation and they have less leakage current than the CB-3D-ReRAM examined at first. Besides, if the technique to make the insulating layers becomes cheaper, perhaps, the alternative topologies given in this paper can be used in the future CB-3D-ReRAMs.

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