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CCM and DCM Analysis of Quasi-Z-Source Derived Push-Pull DC/DC Converter

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Abstract: This paper presents a steady state analysis of the operation modes of the quasi-Z-source (qZS) derived push-pull DC/DC converter topology. It was derived by the combination of the qZS network and coupled inductors. The output stage of the converter consists of a diode bridge rectifier and an LC-filter. This topology provides a wide regulation range of the input voltage and galvanic isolation. These features fit the requirements for the integration systems of renewable energy sources, such as PV panels, variable speed wind turbines, and fuel cells. A converter can operate in continuous (CCM) and discontinuous conduction mode (DCM). Switching period is divided into four and six intervals for CCM and DCM, respectively. Equivalent circuits and analytical expressions for each interval are presented. The DC gain factor for each mode is derived. To simplify our analysis, coupled inductors were substituted with a model that consists of an ideal transformer and magnetizing inductance. Leakage inductances are neglected because the coupling coefficient in this topology should be close to unity. In DCM the converter operation depends on the active duty cycle and the duty cycle of the zero current condition. Two solutions are possible for the DC gain factor in DCM. It is theoretically impossible to achieve the unity DC gain factor in DCM if the turns ratio of coupled inductors is equal to or more than one. The proposed topology was simulated with PSIM software in two operating points. Experimental verification proves our theoretical and simulation results.

Keywords: DC/DC converter, quasi-Z-source converter, galvanic isolation, renewable energy, steady state analysis.

Analiza CCM in DCM Push-Pull DC/DC pretvornika z impedančnim prilagodilnim vezjem

Izvleček: Članek opisuje statično analizo delujočih stanj push-pull DC/DC pretvornika z impedančnim prilagodilnim vezjem (qZS). Izveden je s kombinacijo qZS omrežja in sklopljenih tuljav. Izhodna stopnja pretvornika je sestavljeno iz diodnega usmerniškega mostiča in LC filtra. Topologija omogoča široko regulacijsko območje in galvansko ločitev. Lastnosti ustrezajo zahtevam integriranih sistemov obnovljivih virov energije, kot so PV moduli, vetrne turbine s spremenljivo hitrostjo in gorivne celice. Pretvornik lahko deluje v neprekinjenem (CCM) ali prekinjevalnem (DCM) prevodnem režimu. Perioda preklapljanja je razdeljena na štiri ali šest intervalov za CCM oziroma DCM. Predstavljeno je ekvivalentno vezje in analiza za vsak interval ločeno. Za vsak način je izračunano faktor DC ojačenja. Za poenostavljeno analizo so bili, za sklopljene tuljave, uporabljeni modeli z idealnim transformatorjem in magnetno induktivnostjo. Uhajalne induktivnosti so zaradi enotnosti koeficienta enotnosti v tej topologiji zanemarjene. Pri DCM je delovanje odvisno od aktivnega obratovalnega ciklusa in obratovalnega ciklusa pri ničelnem toku. Možni sta dve rešitvi za DC ojačenje pri DCM. Teoretično je nemogoče doseči enotno ojačenje pri DCM če je razmerje ovojev sklopljenih tuljav večje ali enako ena. Predlagana topologija je bila simulirana s programskim paketom PSIM v dveh točkah delovanja. Ekperimentalen preizkus potrjuje teorijo in rezultate simulacij.

Ključne besede: DC/DC pretvornik, impedančno prilagodilno vezje, galvanska ločitev, obnovljivi viri, statična analiza

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1 Introduction

Quasi-Z-source inverters (qZSIs) providing logical improvement of Z-source inverters were proposed in 2008 [1]. QZSIs extend the family of single stage buck-boost inverters. The concept of the QZSI provides improved reliability due to high EMI withstandability, wide input voltage regulation possibility, and continuous input

current. These features make the qZSI appropriate for the realization of renewable energy systems (PV panels, fuel cells, wind turbines, etc.) [2]-[5] and electric vehicle applications [6]. Output voltage of the renewable energy sources (RES) usually is by far lower than grid voltage. An intermediate DC/DC converter can be used for voltage stabilization when high step-up is needed for RES integration into the grid [7-9]. DC/DC qZSI-based converters have been widely used because of their good performance as voltage matching converters that interconnect the RES and the grid-tied inverter [10]-[12].

The recent push-pull converter derived from the quasi-z-source (qZS) concept is shown in Fig. 1 [13]. This topology has ample opportunities for DC gain regulation [14]. Continuous input current can be achieved in a wide range even for the discontinuous conduction mode (DCM) in branches. The converter contains small component count and only two active switches that lead to a simple control circuit. Topology derivation is based on the combination of two qZS networks implemented with two three-winding coupled inductors.

The converter utilizes two qZS networks: C_1, C_2, D_1, TR_1 and C_3, C_4, D_2, TR_2, as shown in Fig. 1. Three-winding coupled inductors TR_1 and TR_2 provide galvanic isolation and store energy in the form of equivalent magnetizing current (i.e. field in the core of the coupled inductors). Transistors T_1 and T_2 work interleaved. The turn-on state of the transistor corresponds to the shoot-through behavior of the qZS network. Capacitors of the qZS network transfer part of the stored energy to the coupled inductor and the output load during the equivalent shoot-through state. Voltage across the primary windings can be described similarly to that of the conventional qZS network. Current in the primary windings of the coupled inductors differs from the current in the conventional qZS network due to the energy transfer process in the coupled inductors. From the input side the converter looks like two independent branches. These branches are connected in series by means of secondary windings. Summarized voltage of the secondary windings $v_S(t)$ is applied to the diode bridge rectifier $D_3 \ldots D_6$. Rectified voltage feeds the output load with the rectified voltage through the LC-filter L_f, C_f. The frequency of the current ripple of the input current and the output inductor current is twice higher than the switching frequency of the transistors. Voltage regulation is achieved by the adjusting of the turn-on state (active) duty cycle of the transistor.

The aim of this article is to present an analytical description for possible operation modes of the qZS derived push-pull converter. Like most of step-up switching power converters, the investigated topology can operate in the continuous conduction mode (CCM) and DCM. In DCM the transistors and diodes of the qZS networks suffer from high voltage stress. DCM occurs at low DC gain and low input power. The DC gain characteristic depends strongly on the operation mode. This paper is based on our earlier preliminary version [15] and includes substantially revised theoretical analysis and additional experimental results, not presented there.

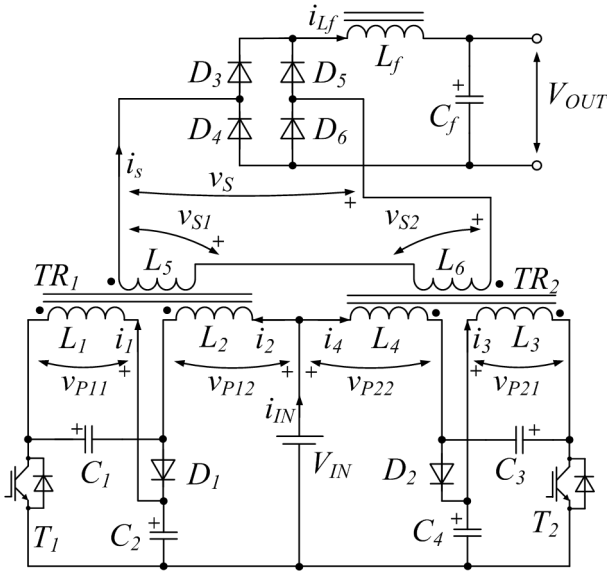


Figure 1: qZS-derived push-pull converter topology.

Several assumptions should be made for our further analysis. In this topology a coupled inductor should have the coupling coefficient close to unity. Primary windings should have an equal number of turns N_{12}. It means that in each qZS network voltages across the primary windings are equal: $v_{P11}(t) = v_{P12}(t)$, $v_{P21}(t) = v_{P22}(t)$. The secondary winding utilizes N_3 turns. The turns ratio $k = N_3/N_{12}$ defines the minimum achievable DC gain. Voltage across the secondary winding depends on the turns ratio and the voltage of the primary windings: $v_{S1}(t) = k \cdot v_{P11}(t)$, $v_{S2}(t) = -k \cdot v_{P21}(t)$, $v_{S1}(t) + v_{S2}(t) = v_S(t)$. In this case coupled inductors can be substituted with a simplified model that consists of the magnetizing inductance L_M reflected to one of the windings and an ideal transformer with N_{12}:N_3 primary to secondary turns ratio. Also, in any mode currents in the primary windings of each coupled inductor are equal: $i_1(t) = i_2(t)$, $i_3(t) = i_4(t)$. Let us assume that the voltage ripple of all capacitors in the converter is well below the corresponding average voltage. These assumptions and the symmetry of branches result in equal average voltages across the capacitors: $V_{C1} = V_{C3}$, $V_{C2} = V_{C4}$. Let us assume that the current of the filter inductor $i_{Lf}(t)$ is continuous in any mode. None of the losses are considered in this article. It means that the input power P and the output power are equal: $I_{OUT} = I_{Lf} = P/V_{OUT}$. The lower case letter of the voltage and the current corresponds to an instantane-

ous value, and the upper case letter or angle brackets correspond to an averaged (or constant in some cases) value. The input power is represented as *P*. For the symmetry operation of the branches, each of them should operate at half of the rated power: $I_4 = I_2 = P/(2 \cdot V_{IN})$.

2 Circuit Steady-State Analysis in CCM

Current and voltage waveforms for an idealized converter in CCM are shown in Fig. 2. The figure shows that the switching period of the converter *T* can be divided into four time intervals: two equal active intervals during which only one of the transistors is turned on (i.e. active states with the time duration t_A each) and two inactive intervals when both transistors are not conducting (i.e. zero state, t_0 each):

$$\frac{t_A}{T} + \frac{t_0}{T} = D_A + D_0 = 0.5. \tag{1}$$

where D_A is the duty cycle of an active state and D_0 is the duty cycle of a zero state. It is clear from (1) that $D_A < 0.5$ and $D_0 < 0.5$. In CCM, as well as in DCM, the current $i_{Lf}(t)$ has a double switching frequency ripple. Also, in both modes $i_{Lf}(t)$ always rises during active states and falls during a zero state.

Figure 3a shows the equivalent circuit of the converter for the time interval *t1-t2* when the transistor T_1 is turned on, diode D_1 is blocked and D_2 is conducting. Equations (2)-(6) describe the behavior of the converter during this time interval.

$$v_{C1}(t) = v_{C2}(t) - V_{IN}, \tag{2}$$

$$v_{C2}(t) = v_{P11}(t) = L_M \cdot \frac{di_{LM1}(t)}{dt} = \\ = L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - k \cdot i_{Lf}(t)\right), \tag{3}$$

$$v_{C3}(t) = -v_{P21}(t) = -L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) + k \cdot i_{Lf}(t)\right), \tag{4}$$

$$v_{C4}(t) = V_{IN} + v_{C3}(t), \tag{5}$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(v_{C2}(t) + v_{C3}(t)\right) = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - i_3(t) - i_4(t) - 2 \cdot k \cdot i_{Lf}(t)\right). \tag{6}$$

where $v_{C1}(t)$, $v_{C2}(t)$, $v_{C3}(t)$, $v_{C4}(t)$ are the capacitor voltages, $v_{S1}(t)$ and $v_{S2}(t)$ are the voltages of the corresponding secondary windings of the transformer, $v_S(t)$ is the summarized voltage of the secondary winding applied to the rectifier, $i_1(t)$, $i_2(t)$, $i_3(t)$, $i_4(t)$ are the currents of the corresponding primary windings of the transformer, L_M is the magnetizing inductance of the coupled inductors, *k* is the turns ratio of the coupled inductors, and $i_{Lf}(t)$ is the current of the filter inductor L_f.

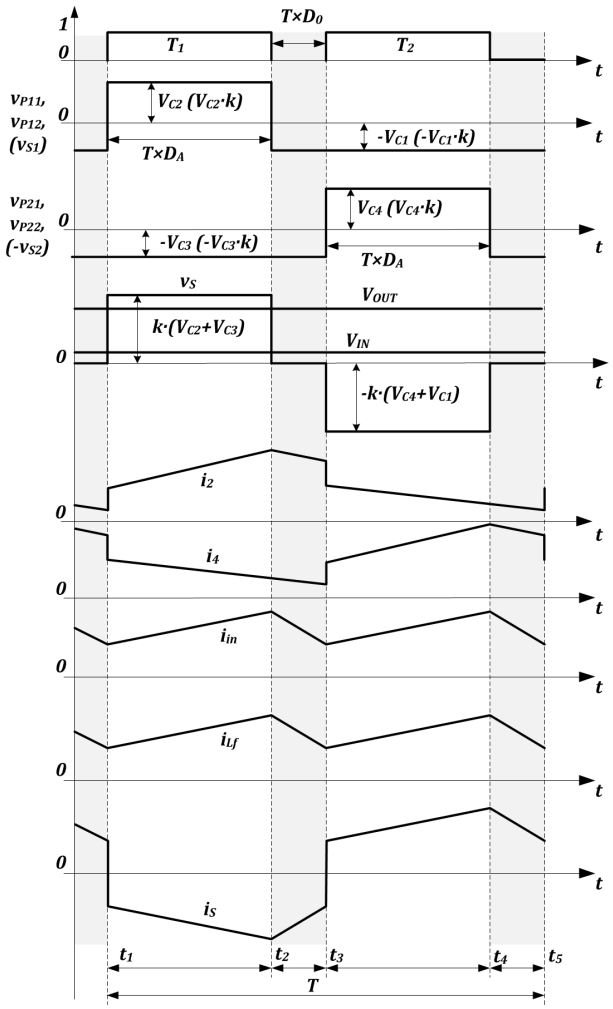


Figure 2: Generalized converter voltage and current waveforms during the operation in CCM.

During the interval t_2-t_3 both transistors are not conducting, diodes D_1 and D_2 are conducting. The equivalent circuit of the converter is depicted in Fig. 2b. Equations (7)-(11) describe the operation of the converter for that time interval. Summarized voltage of the secondary windings $v_S(t)$ is equal to zero if the voltage ripple of the qZS capacitors is negligible.

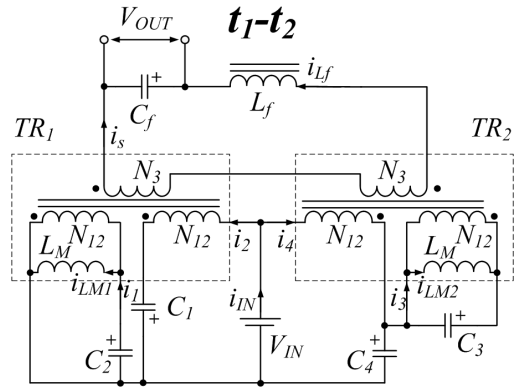
$$v_{C1}(t) = -v_{P11}(t) = -L_M \cdot \frac{di_{LM1}(t)}{dt} \\ = -L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - k \cdot i_{Lf}(t)\right), \tag{7}$$

$$v_{C2}(t) = V_{IN} + v_{C1}(t), \tag{8}$$

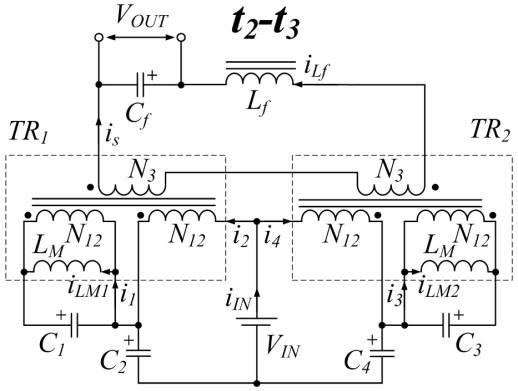
$$v_{C3}(t) = -v_{P21}(t) = -L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) + k \cdot i_{Lf}(t)\right), \tag{9}$$

$$v_{C4}(t) = V_{IN} + v_{C3}(t), \tag{10}$$

(a)



(b)



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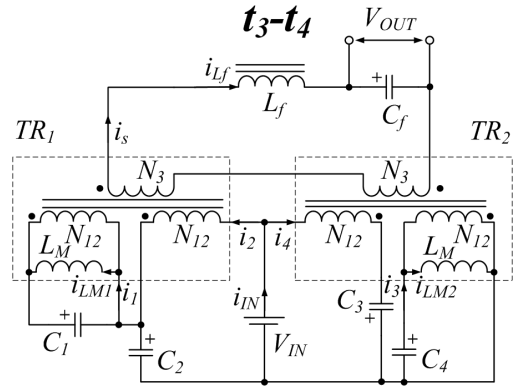

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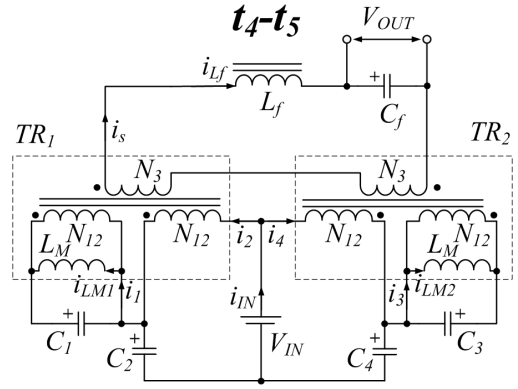

Figure 3: Equivalent circuits of the investigated converter in CCM.

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(v_{C3}(t) - v_{C1}(t)\right) = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - i_3(t) - i_4(t) - 2 \cdot k \cdot i_{Lf}(t)\right) \approx 0. \quad (11)$$

Figure 2c depicts the equivalent circuit of the converter for the time interval t_3-t_4 when the transistor T_2 is turned on, the diode D_2 is reverse based and D_1 is conducting. Equations (12)-(16) define the operation of the converter during the time interval t_3-t_4:

$$v_{C1}(t) = -v_{P11}(t) = -L_M \cdot \frac{di_{LM1}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) + k \cdot i_{Lf}(t)\right), \quad (12)$$

$$v_{C2}(t) = V_{IN} + v_{C1}(t), \quad (13)$$

$$v_{C3}(t) = v_{C4}(t) - V_{IN}, \quad (14)$$

$$v_{C4}(t) = v_{P21}(t) = L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) - k \cdot i_{Lf}(t)\right), \quad (15)$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(-v_{C1}(t) - v_{C4}(t)\right) = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - i_3(t) - i_4(t) - 2 \cdot k \cdot i_{Lf}(t)\right). \quad (16)$$

During the interval t_4-t_5 both transistors are switched off, diode D_1 and diode D_2 are conducting. The equivalent circuit for the fourth interval is shown in Fig. 2b. Equations (17)-(21) define the behavior of the converter for the time interval t_4-t_5. Summarized voltage of the secondary windings $v_S(t)$ is equal to zero if the voltage ripple of the qZS capacitors is negligible. The fourth interval differs from the second in the direction of the current $i_{Lf}(t)$ via the secondary windings, i.e. $i_S(t)$ has an opposite sign.

$$v_{C1}(t) = -v_{P11}(t) = -L_M \cdot \frac{di_{LM1}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) + k \cdot i_{Lf}(t)\right), \quad (17)$$

$$v_{C2}(t) = V_{IN} + v_{C1}(t), \quad (18)$$

$$v_{C3}(t) = -v_{P21}(t) = -L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) - k \cdot i_{Lf}(t)\right), \quad (19)$$

$$v_{C4}(t) = V_{IN} + v_{C3}(t), \quad (20)$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(v_{C3}(t) - v_{C1}(t)\right) = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - i_3(t) - i_4(t) + 2 \cdot k \cdot i_{Lf}(t)\right) \approx 0. \quad (21)$$

At the time moments t_1, t_3 and t_5 currents in the primary windings change by step:

$$\Delta i_2(t_1) = -\Delta i_4(t_1) = k \cdot i_{Lf}(t_1),$$

$$\Delta i_4(t_3) = -\Delta i_2(t_3) = k \cdot i_{Lf}(t_3),$$

$$\Delta i_2(t_5) = -\Delta i_4(t_5) = k \cdot i_{Lf}(t_5).$$

This step change could be explained by the change of the direction of the current $i_S(t)$. Also, these steps are equal because $i_{Lf}(t_1) = i_{Lf}(t_3) = i_{Lf}(t_5)$. These steps are not reflected in the input current because the steps of currents $i_2(t)$ and $i_4(t)$ compensate each other.

According to the voltage-second balance principle, the average voltage across the primary winding of the coupled inductor over one switching period equals zero. That can be used for the calculation of the average voltage across the qZS capacitors:

$$V_{P11} = \langle v_{P11}(t) \rangle = \frac{1}{T}\int_0^T v_{P11}(t)dt = 0, \tag{22}$$

$$V_{P21} = \langle v_{P21}(t) \rangle = \frac{1}{T}\int_0^T v_{P21}(t)dt = 0. \tag{23}$$

In order to solve Eqs. (22) and (23) we need to assume that the voltage across the capacitors is close to the average value over the switching period:

$$v_{C1}(t) \approx \langle v_{C1}(t) \rangle = V_{C1}, \tag{24}$$

$$v_{C2}(t) \approx \langle v_{C2}(t) \rangle = V_{C2}, \tag{25}$$

$$v_{C3}(t) \approx \langle v_{C3}(t) \rangle = V_{C3}, \tag{26}$$

$$v_{C4}(t) \approx \langle v_{C4}(t) \rangle = V_{C4}. \tag{27}$$

The following expressions are right for all the intervals according to Eqs. (24)-(27) and (2)-(21):

$$V_{C2} = V_{IN} + V_{C1}, \tag{28}$$

$$V_{C4} = V_{IN} + V_{C3}. \tag{29}$$

$$V_{C1} = V_{C3}, \tag{30}$$

$$V_{C2} = V_{C4}. \tag{31}$$

From Eqs. (22)-(31) it is easy to find expressions for the capacitor voltages:

$$V_{P11} = V_{C2} \cdot D_A - V_{C1} \cdot (1 - D_A) =$$
$$= D_A \cdot (V_{IN} + V_{C1}) - V_{C1} \cdot (1 - D_A) = 0,$$

$$V_{C1} = V_{C3} = \frac{D_A}{1 - 2 \cdot D_A} V_{IN}, \tag{32}$$

$$V_{C2} = V_{C4} = \frac{1 - D_A}{1 - 2 \cdot D_A} V_{IN}. \tag{33}$$

Using Eqs. (1)-(33) and considering all the abovementioned assumptions, the summarized voltage of the secondary windings of the coupled inductors could be analytically expressed for each time interval:
Time interval t_1-t_2:

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot (V_{C2} + V_{C3}). \tag{34}$$

Time interval t_3-t_4:

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = -k \cdot (V_{C1} + V_{C4}). \tag{35}$$

Time intervals t_2-t_3 and t_4-t_5:

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot (V_{C3} - V_{C1}) = 0. \tag{36}$$

In CCM the output voltage of the converter can be expressed as

$$V_{OUT} = \frac{1}{T}\int_0^T |v_{S1}(t) + v_{S2}(t)| \cdot dt =$$
$$= k \cdot \frac{2}{T}\int_0^{T \cdot D_A} (V_{C3} + V_{C2}) \cdot dt = \frac{N_3}{N_{12}} \cdot \frac{2 \cdot D_A}{1 - 2 \cdot D_A} \cdot V_{IN}. \tag{37}$$

The resulting DC voltage gain of the proposed DC/DC converter is

$$G = k \cdot \frac{2 \cdot D_A}{1 - 2 \cdot D_A}. \tag{38}$$

In Fig. 4 the DC voltage gain of the converter (38) is depicted as a function of an active state duty cycle for different turns ratios of the coupled inductors. As is seen, a very wide regulation range of the DC voltage gain could be achieved for the lossless system. Also, high step-up can be reached using coupled inductors with a high turns ratio. In real systems the DC voltage gain of the step-up converter usually is seriously influenced by the losses in the components, especially in semiconductors.

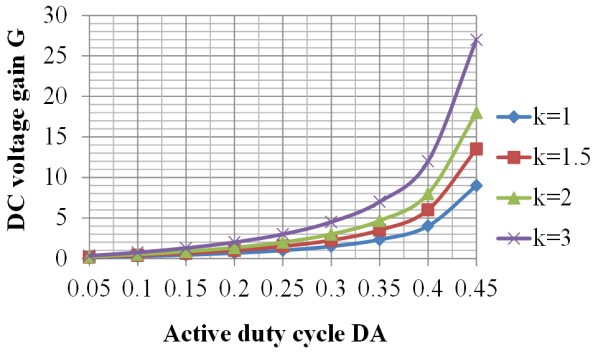

Figure 4: DC voltage gain G as a function of the active state duty cycle D_A for the proposed DC/DC converter operated in CCM.

3 Circuit Steady-State Analysis in DCM

In general, the converter operation mode is considered as DCM when the input current falls to zero. However, in the investigated topology, DCM will be considered as a mode when the current in the primary winding of the coupled inductor drops to zero. In DCM the input current can still remain continuous. Typical waveforms

for DCM are shown in Fig. 5. Two additional equivalent circuits that are needed for the analysis of DCM are shown in Figs. 6a and 6b. These figures correspond to the time intervals t'_1-t_2 and t'_3-t_4, respectively. During other time intervals converter operation is the same as for CCM. If the duty cycle of the DCM state γ less than the D_0 converter operation is almost similar to CCM.

Figure 6a shows the equivalent circuit of the converter during the time interval t'_1-t_2 when the transistor T_1 is turned on, diode D_1 is reverse based, and diode D_2 is not conducting. This mode is possible only if $\gamma > D_0$. Voltage is applied to the diode D_2: $v_{D2}(t) = v_{C3}(t) + \alpha$, where $\alpha = v_{P21}(t)$. Voltage α is constant during this time interval. Equations (39)-(43) describe the operation of the converter during this time interval when $i_3(t) = i_4(t) = 0$.

$$v_{C1}(t) = v_{C2}(t) - V_{IN}, \quad (39)$$

$$v_{C2}(t) = v_{P11}(t) = L_M \cdot \frac{di_{LM1}(t)}{dt} = \\ = L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - k \cdot i_{Lf}(t)\right), \quad (40)$$

$$v_{P21}(t) = v_{P22}(t) = \alpha = k \cdot L_M \cdot \frac{di_{Lf}(t)}{dt}, \quad (41)$$

$$v_{C4}(t) = V_{IN} + v_{C3}(t), \quad (42)$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(v_{C2}(t)\right) - k \cdot L_M \cdot \frac{di_{Lf}(t)}{dt} = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - 2 \cdot k \cdot i_{Lf}(t)\right) \approx V_{C2} - \alpha. \quad (43)$$

Figure 6b shows the equivalent circuit of the converter for the time interval t'_3-t_4 when the transistor T_2 is conducting, the diode D_1 is not conducting, and the diode D_2 is reverse based. Voltage is applied to the diode D_1: $v_{D1}(t) = v_{C3}(t) + \alpha$, where $\alpha = v_{P11}(t)$. Equations (44)-(48) describe the behavior of the converter over this time interval considering that $i_1(t) = i_2(t) = 0$.

$$v_{P11}(t) = v_{P12}(t) = \alpha = k \cdot L_M \cdot \frac{di_{Lf}(t)}{dt}, \quad (44)$$

$$v_{C2}(t) = V_{IN} + v_{C1}(t), \quad (45)$$

$$v_{C3}(t) = v_{C4}(t) - V_{IN}, \quad (46)$$

$$v_{C4}(t) = v_{P22}(t) = L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) - k \cdot i_{Lf}(t)\right), \quad (47)$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(-v_{C4}(t)\right) + k \cdot L_M \cdot \frac{di_{Lf}(t)}{dt} = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(-i_3(t) - i_4(t) + 2 \cdot k \cdot i_{Lf}(t)\right) \approx -V_{C4} + \alpha. \quad (48)$$

3.1 DCM mode 1

If the duty cycle of the DCM state is less than the duty cycle of the zero state ($0 < \gamma < D_0$), the operation of the converter will remain unchanged. In this case the behavior of the converter could be described by Eqs. (2)-(6).

3.2 DCM mode 2

In case the duty cycle of the DCM state lies in the range $D_0 < \gamma < 0.5$, the average voltage of the qZS capacitors and the DC voltage gain of the converter should be recalculated. It can be done using Fig. 5, taking into account (22)-(31), and assuming that α is equal to zero in order to simplify the calculations:

$$V_{P11} = V_{C2} \cdot D_A - V_{C1} \cdot (1 - D_A - \gamma + D_0) = \\ = D_A \cdot (V_{IN} + V_{C1}) - V_{C1} \cdot (1.5 - \gamma - 2 \cdot D_A) = 0,$$

$$V_{C1} = V_{C3} = \frac{2 \cdot D_A}{3 - 2 \cdot \gamma - 6 \cdot D_A} V_{IN}, \quad (49)$$

$$V_{C2} = V_{C4} = \frac{3 - 2 \cdot \gamma - 4 \cdot D_A}{3 - 2 \cdot \gamma - 6 \cdot D_A} V_{IN}. \quad (50)$$

The output voltage of the converter operated in DCM when $D_0 < \gamma < 0.5$ can be expressed as

$$V_{OUT} = \frac{1}{T}\int_0^T \left|v_{S1}(t) + v_{S2}(t)\right| \cdot dt \approx \\ \approx k \cdot \frac{2}{T}\left(\int_0^{T \cdot (0.5-\gamma)} (V_{C2} + V_{C3}) \cdot dt + \int_{T \cdot (0.5-\gamma)}^{T \cdot D_A} V_{C2} \cdot dt\right) = \\ = \frac{N_3}{N_{12}} \cdot \frac{8 \cdot D_A \cdot (1 - \gamma - D_A)}{3 - 2 \cdot \gamma - 6 \cdot D_A} \cdot V_{IN}. \quad (51)$$

The resulting DC voltage gain of the proposed DC/DC converter is

$$G = k \cdot \frac{8 \cdot D_A \cdot (1 - \gamma - D_A)}{3 - 2 \cdot \gamma - 6 \cdot D_A}. \quad (52)$$

In the DCM, when $\gamma = 0.5$ each branch consumes current only during $T/2$. In this case, time t_1 equals t'_1, and time t_3 equals t'_3. The input current of the converter is in the boundary conduction mode and reaches zero twice per switching period at the time moments t_1 and t_3. Current steps occur due to the change of the sign of the current $i_S(t)$ at the same time moments.

The condition $\gamma > 0.5$ is theoretically possible when the converter needs to operate at very low input power compared to the rated power value. This mode corresponds to the discontinuous input current. It should be avoided because of high overvoltage across the power semiconductor components. This mode could be avoided practically due to the losses in the converter. Also, renewable energy systems usually require high step-up at low power, or do not require ultra-light-load operation. On the other hand, in this mode the converter needs enormous inductance at the output filter

to satisfy the assumption about the continuous inductor current.

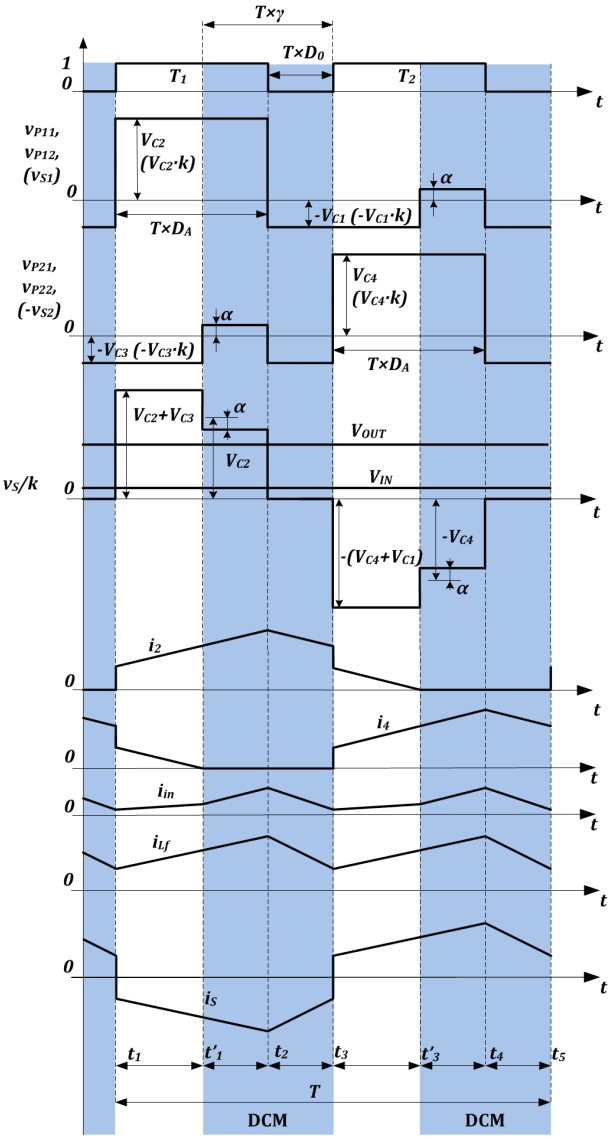

Figure 5: Generalized converter voltage and current waveforms during the operation in DCM.

4 Experimental Verification

Theoretical assumptions were verified by means of modeling. The model was rated for the power of 600 W in compliance with the topology shown in Fig. 1. Component values and given modeling conditions are listed in Table I. Simulation results are shown in Figs. 8 and 10. In the first case, the model of the converter operates in CCM (input voltage of 70 V and D_A = 0.43), while in the second modeling, the converter operates in DCM (input voltage of 250 V and D_A = 0.25).

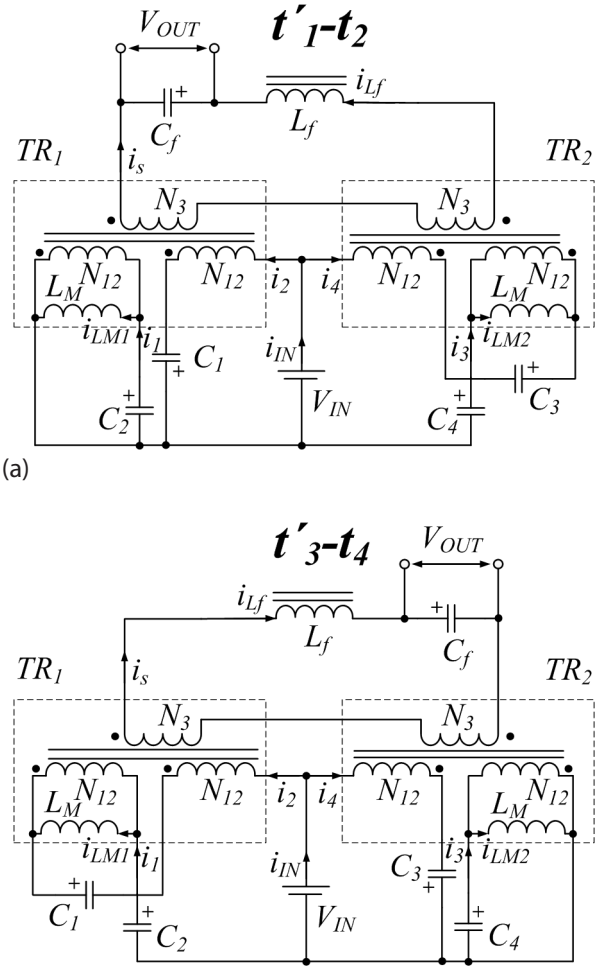

Figure 6: Additional equivalent circuits of the investigated converter for DCM.

Theoretical and simulation results were verified using a 600 W laboratory prototype, which is shown in Fig. 7. It was assembled in compliance with schematics in Fig. 1. Experimental waveforms including the input voltage are presented in Figs. 9 and 11. In the case of 70 V at the input, the converter operates in CCM. For CCM, experimental results are in good agreement with the theoretical assumption. On the other hand, when the input voltage equals 250 V, and the converter operates in DCM, the parasitic parameters in the experimental prototype cause major oscillations. Distinctions between the experimental and simulated waveforms are considerable.

Figure 12 shows experimentally measured curve of active state duty cycle D_A versus input voltage and DC voltage gain for constant output voltage 400 V and output power 600 W. CCM is achieved for input voltage below 150 V DC. Converter operates in DCM when input voltage is higher than 150 V DC. Measured curve has higher non-linearity in DCM, as it was expected.

Table 1: Operating Parameters and Passive Component Values of the Converter

Main operating parameters	Value
Minimal input voltage VIN, min	70 V
Maximal input voltage VIN, max	250 V
Desired output voltage VOUT	400 V
Nominal power P	600 W
Switching frequency fsw=1/T	100 kHz
Turns ratio of the isolation transformers N3:N12	1:1
Passive component values	
Capacitance value of the capacitors C1...C4	60 µF
Magnetizing inductance of the isolation transformers LM	1 mH
Inductance of the filter inductor Lf	1 mH
Capacitance of the filter capacitor Cf	220 µF

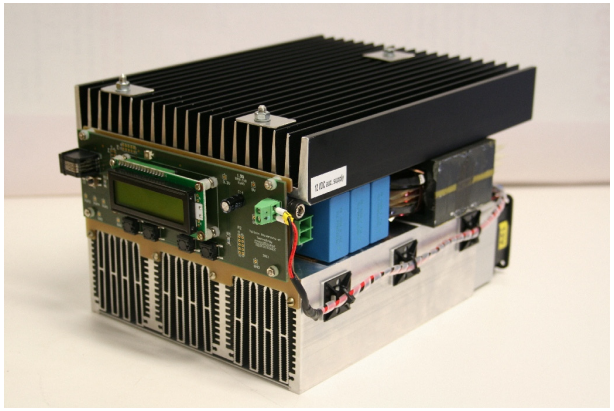

Figure 7: Converter prototype used for experimental verification.

5 Conclusions

The paper has presented a steady state analysis of the operation of the qZS derived push-pull DC/DC converter in the continuous and discontinuous conduction mode. The mathematical analysis provides a general solution for waveforms and values of voltage and current in the passive components. Some differences between the theoretical results and the simulation and experimental results are related to an idealized model (losses in components, leakage inductance are neglected). The converter reveals that the behavior in DCM is complicated. The DCM state duty cycle appears when half of the current ripple through the primary winding, defined by the magnetizing inductance, surpasses an average primary winding current defined by the load power. This mode of operation could occur at the gain factors closer to unity. This topology is a good solution

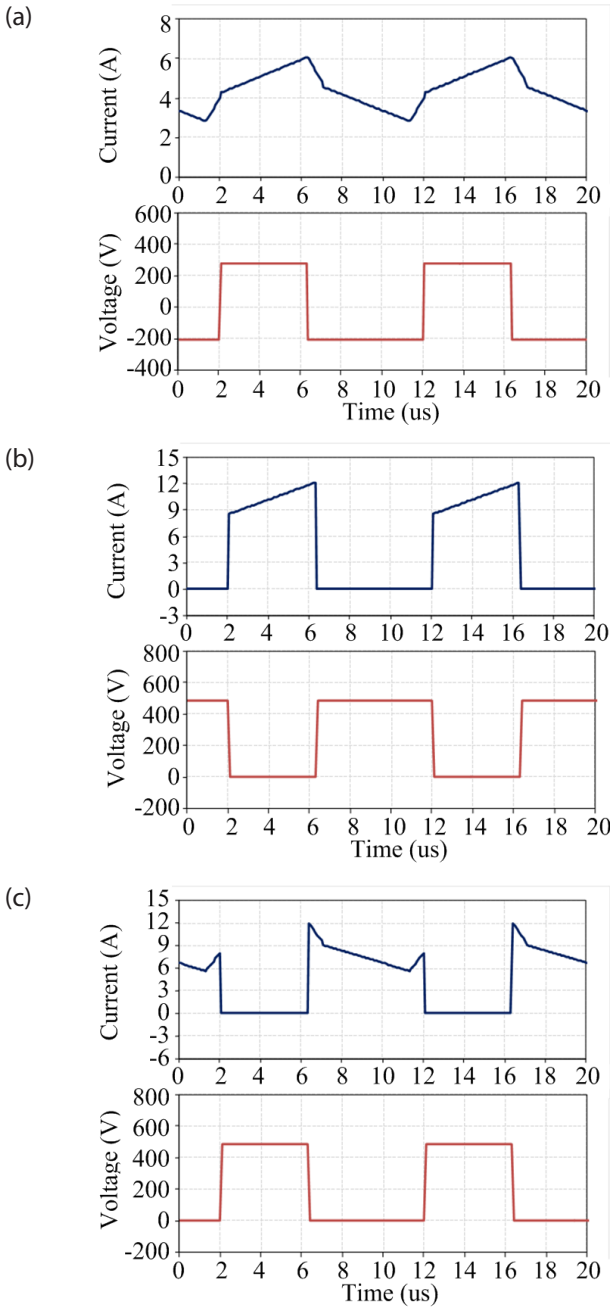

Figure 8: CCM simulated waveforms of the transformer primary (a), transistor (b) and qZS diode (c) at 600 W with the input voltage of 70 V

for the integration of a variable voltage variable speed small wind turbine. In this case the converter operates with a lower gain at a higher power. This condition combined with the features of the converter could ensure operation in CCM in a wide range of power

The mathematical analysis was verified by means of the simulation software and the experimental prototype. As shown, the results are in good agreement with the theoretical predictions.

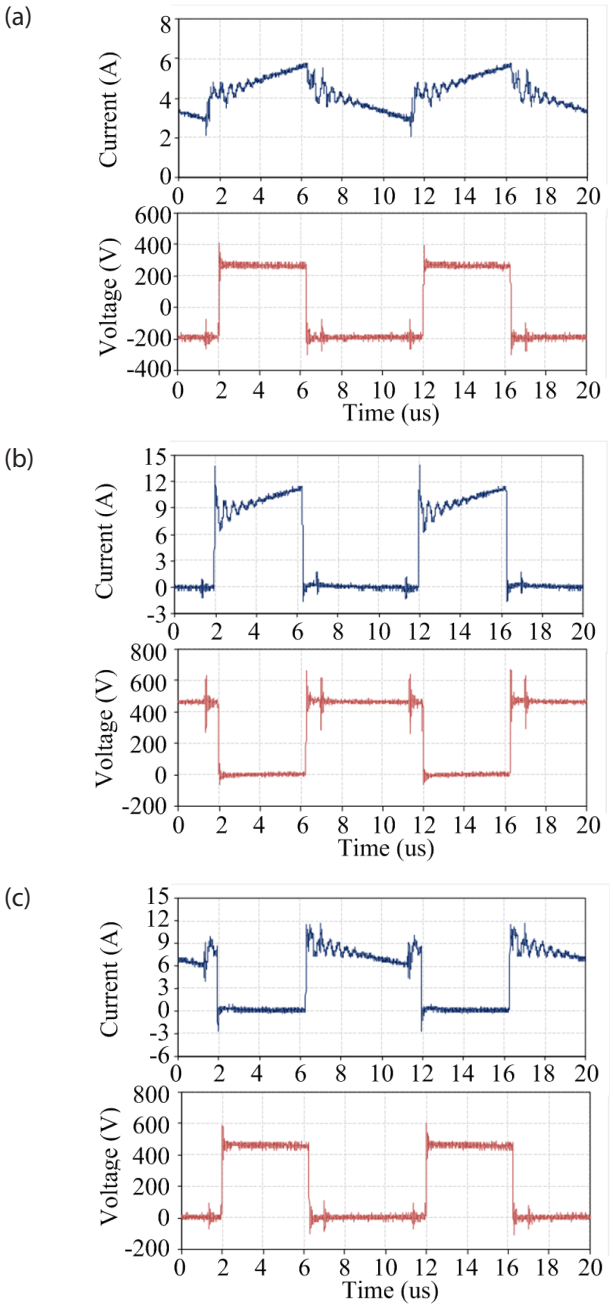

Figure 9: CCM experimental waveforms of the transformer primary (a), transistor (b) and qZS diode (c) at 600 W with the input voltage of 70 V.

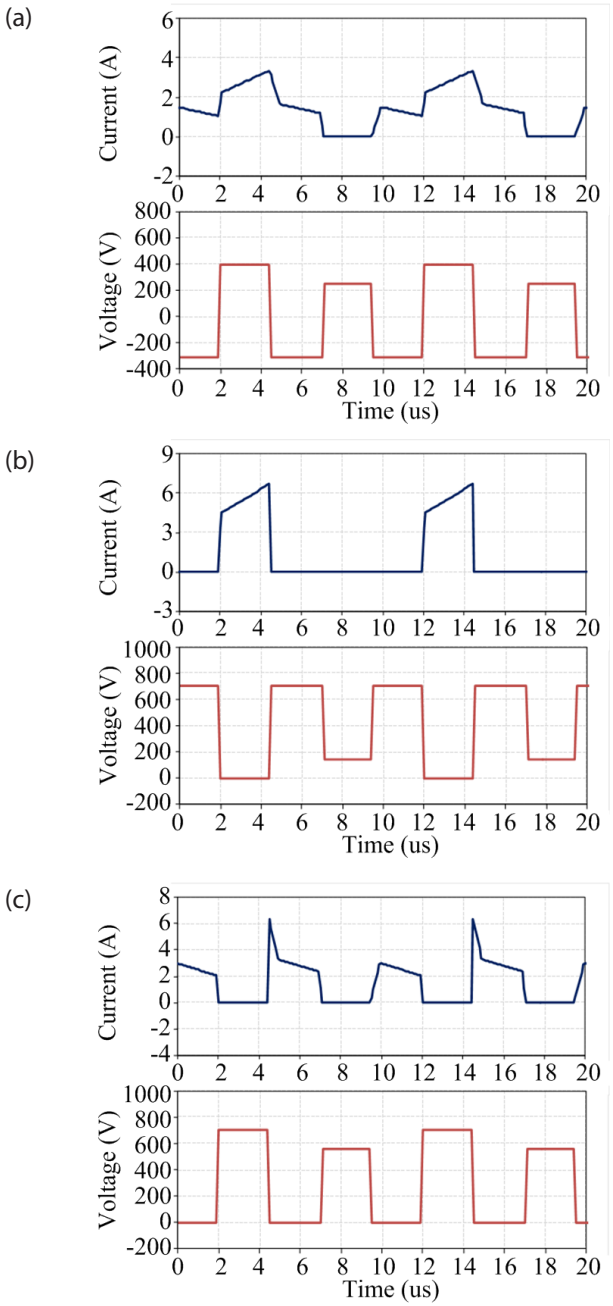

Figure 10: DCM simulated waveforms of the transformer primary (a), transistor (b) and qZS diode (c) at 600 W with the input voltage of 250 V.

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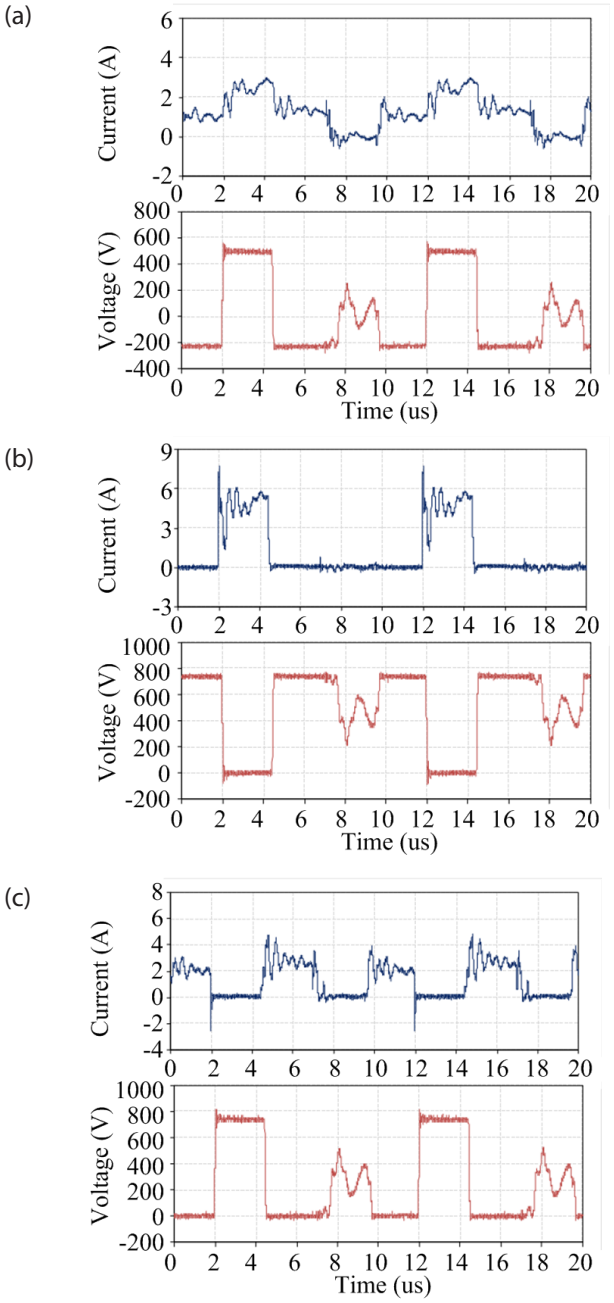

Figure 11: DCM experimental waveforms of the transformer primary (a), transistor (b) and qZS diode (c) at 600 W with the input voltage of 250 V.

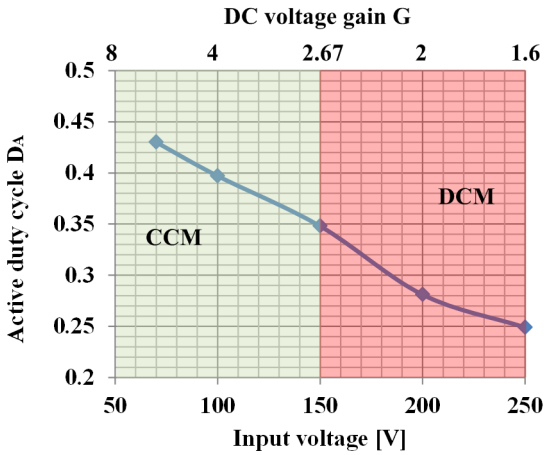

Figure 12: Experimentally measured active state duty cycle D_A versus input voltage and DC voltage gain.

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