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DTMOS Based High Bandwidth Four-Quadrant Analog Multiplier

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Abstract: Analog multiplication circuits are very important blocks widely used in analog signal processing applications. In analog multiplication circuits, low power consumption is expected with wide bandwidth, low nonlinearity and high input range according to the supply voltage. In this work, folded Gilbert cell structure was resized using dynamic threshold MOS (DTMOS) transistors. The proposed circuit is laid out with 491.4 μm2 chip area. Post layout simulations show that the proposed circuit has high bandwidth (1.2 GHz), low supply voltage (0.2 V), and low power consumption (44.6 μW). In addition, the proposed circuit is examined for temperature variation, total harmonic distortion, intermodulation products and Monte Carlo analysis of the dimensioning of the circuit. The post layout results show that the proposed circuit has promising performance against its counterparts in the literature.

Keywords: Four-quadrant; analog multiplier; DTMOS.

Štiri-kvadranten širokopasovni množilnik na osnovi DTMOS

Izvleček: Analogna množilna vezja imajo zelo pomemben del pri analognem procesiranju signalov. Od njih se pričakuje nizka poraba, velika pasovna širina, nizka nelinearnost, in visoko vhodno območje glede na napajalno napetost. V tem delu je bila uporabljena povečana Gilbertova struktura z uporabo tranzistorjev z dinamičnim pragom (DTMOS). Vezje je narejeno na površini 491.4 μm2. Simulacije so pokazale, da je pasovna širina vezja 1.2 GHz, napajalna napetost 0.2 V in poraba 44.6 μW. Dodatno je bil raziskan vpliv temperature, skupna harmonična distorzija, intermodulacija in Monte Carlo analiza.

Ključne besede: štiri kvadranten; analogni množilnik; DTMOS.

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1 Introduction

Analog multipliers that are commonly used in analog signal processing applications such as analog and frequency modulation, phase locked-loop, phase shifting and detection, frequency converter, automatic control, artificial neural networks, Neuro-fuzzy systems. The analog multipliers are electronic circuits with two input ports and one output port. Output signal of the multiplier is defined by the transfer function $z = K \times x \times y$, where x and y are two continuous input signals and K is a constant value appropriately dimensioned. Analog multipliers are classified according to the polarization of their inputs. The classifications are as follows: i) One quadrant [1] whose inputs are non-polarized, ii) Two quadrant [2], [3] whose one of the inputs are polarized, iii) Polarized both inputs are called four quadrant [4–7]. In addition, the multipliers are divided into two types: current mode [8], [9] and voltage mode [4–7].

The first bipolar analog multiplier known as the Gilbert cell was published in 1968 by Barrie Gilbert [10]. Since analog multipliers based on CMOS technology have been classified (i) according to the form of the input signal; current or voltage mode (ii) with regard to the operating region of the transistors; weak inversion [8], [11], [12] strong inversion [13], [14], saturation region [15] and linear region [16], [17]. Although the input signal range and bandwidth of analog multipliers operating in the weak inversion region are quite narrow, they are frequently used in low power consumption applications. Analog multipliers operating in the saturation region have wide bandwidth, dynamic input range and high speed. In multipliers operating in the strong inversion region, the error caused by the body effect causes mismatch in the threshold voltage.

In recent years, the increasing popularity of portable devices such as smartphones and tablet computers has brought restrictions on battery capacity, weight and size. It has created serious restrictions on power consumption and led to the emergence of low-power and high-performance circuitry techniques. Thus, several methods have been suggested to concentrate the power consumption of the analog multipliers. Some of these techniques are as follows: weak-inversion [8], [11], [12], [18], subthreshold MOSFETs [19–23], bulk driven [11], [12], DTMOS [24][25], and floating gate MOSs [5], [26], [27]. It is seen that transistor multipliers working in weak inversion region have poor dynamic range, limited voltage swing and low bandwidth. In the study of Soltany and Razai [12], although the power consumption was reduced by bulk-input, it was seen that the speed and output voltage range were also very low. Even though, analog multipliers designed with transistors operating in the subthreshold region [19–23] show low power consumption, but the dynamic range and operating speed of the multiplier are low. In the study, using DTMOS transistor [24], low power consumption and full-scale input voltage were provided, but -3dB bandwidth was obtained as 1.11 MHz. In articles [26] and [27] a low power consumption analog multiplication circuit was implemented using FGMOS, but their bandwidth was specified as 10 MHz and 200 MHz, respectively. In the study of Keles and Kuntman [5], FGMOS technique has been achieved with high bandwidth such as 1.5 GHz, but there is no information about power consumption here.

In this article, a low power, wide bandwidth four-quadrant analog multiplier by using DTMOS based folded Gilbert cell is proposed. The simulation results are given using Cadence Environment using 0.18 µm TSMC CMOS technology under a supply voltage of 0.2 V.

Gilbert cell is one of the first studies of analog multiplication circuits proposed by Barrie Gilbert in 1968 [10]. Gilbert cell is popular in bipolar integrated circuits (IC) due to its wide dynamic range and bandwidth. In this study, the analog multiplier was realized with the folded Gilbert cell by using DTMOS technology and the bandwidth is obtained pretty much wider.

Due to undesirable behavior in nonlinearity, the range of the input signal is limited to half or generally much less of the supply voltage. In this study, full-scale supply voltage can be used for an input signal range [26]. In order to demonstrate its technological strength, Monte Carlo analyses were performed in AC form with 10% mismatch of process parameters (t_{ox} and V_{TH}) and transistor widths.

The rest of the paper is arranged as follows: Information on the DTMOS structure and the proposed multiplication circuit structure as well as equations are given in Section 2. AC/DC characteristics, intermodulation products, temperature sensitivity, total harmonic distortion and Monte Carlo analysis are given in Section 3. Finally, Section 4 concludes the paper.

2 DTMOS based four-quadrant analog multiplier

Today, the increase in the use of portable devices has brought limits on battery capacity, weight and size. These restrictions have contributed to an increase in studies on low power and high performance circuit techniques.

The need to reduce power consumption has led to a reduction in the supply voltage of the circuits. Excessive lowering of the supply voltage causes standby power and speed problems of the memory elements. MOSFET with dynamic threshold voltage was proposed by Assaderaghi et al. in 1994 to meet low voltage performance requirements [28]. The topology and symbol of the DTMOS obtained by connecting the body and gate of a MOSFET are given in Figure 1.

The threshold voltage of DTMOS is as follows:

$$V_{th} = V_{t0} + \gamma\left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{2\phi_F}\right) \quad (1)$$

V_{th} is threshold voltage, V_{t0} is the zero body bias threshold voltage. γ is the body effect coefficient and it depends on the gate oxide capacitance, silicon permittivity and substrate doping ϕ_F. is the Fermi potential. V_{SB} is the source to body voltage. The threshold voltage

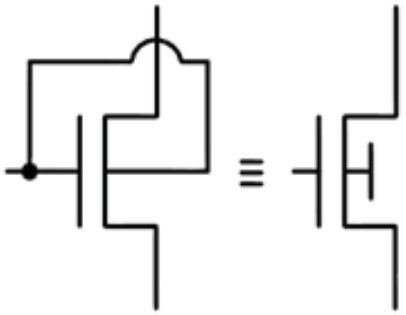

Figure 1: Topology and symbol of DTMOS.

equation is written for a long channel NMOS transistor where drain-induced barrier lowering (DIBL) effect is neglected. The proposed DTMOS has a high threshold voltage at zero bias and low threshold voltage when the gate-source voltage is equal to supply voltage($V_{gs} = V_{dd}$)[29].

By reduction of threshold voltage, inversion charge (Q_N) is increased; so, larger inversion charge leads to a higher current drive in DTMOS in comparison to the regular MOSFETs

MOS transistor's drain current is given by below Eq. (2).

$$I_D = I_S\left(\frac{W}{L}\right)exp\left(q\frac{V_{GS}-V_{TH}}{nkT}\right)\left[1-exp\left(-q\frac{V_{DS}}{kT}\right)\right] \quad (2)$$

According to the equation the transistor will saturate in weak inversion when $V_{DS} \geq 3kT/q$ [17]. Under some limitations, bulk-DTMOS technique can be applied to cheap standard CMOS fabrication process without additional processing steps. The transconductance g_m is described by

$$g_m = q\frac{I_D}{nkT} \quad (3)$$

DTMOS reduces the junction width and consequently the depletion region charge density, which contributes to a decrease in the threshold voltage. In case of reverse bias, the depletion region width increases, and the increase in the body charges causes the threshold voltage to increase. DTMOS-based circuits in case of forward biasing, the threshold voltage will be low. When the transistor is turned off, the V_{TH} becomes high, resulting the leakage current will also be low. Thus, the threshold voltage is changed dynamically with respect to the gate input, whereas operating state of the circuit is also changed.

The DTMOS based four-quadrant analog multiplier circuit by using the folded Gilbert cell is presented in Figure 2. M3-M4 forms one differential pair, while M5-M6 transistors form another differential pair. The drain of M3-M5 and M4-M6 transistors are cross connected. The input signal V_X is applied to the cross connected differential pairs, while the input signal V_Y is applied to another differential pair consisting of M1 and M2. The bias currents (I_{SS1}, I_{SS2}, I_{SS3}) are the tail currents and $I_{SS1} = I_{SS2} = I_{SS3}$. The output current expression of the circuit is:

$$I_{OUT} = k_n V_X\left[\sqrt{\frac{k_p}{k_n}\left(\sqrt{\frac{I_{SS}}{k_p}-\frac{V_Y^2}{2}}+\frac{V_Y}{\sqrt{2}}\right)^2-V_X^2}-\sqrt{\frac{k_p}{k_n}\left(\sqrt{\frac{I_{SS}}{k_p}-\frac{V_Y^2}{2}}-\frac{V_Y}{\sqrt{2}}\right)^2-V_X^2}\right] \quad (4)$$

Where k_n and k_p are the transconductance of the n-channel and p-channel transistors, respectively. $k_n = (\mu_n C_{OX}/2)(W/L)$, μ_n, is the electron mobility, C_{OX} is the gate oxide capacitance of the NMOS transistor. W and L are the width and length of the NMOS transistors, respectively.

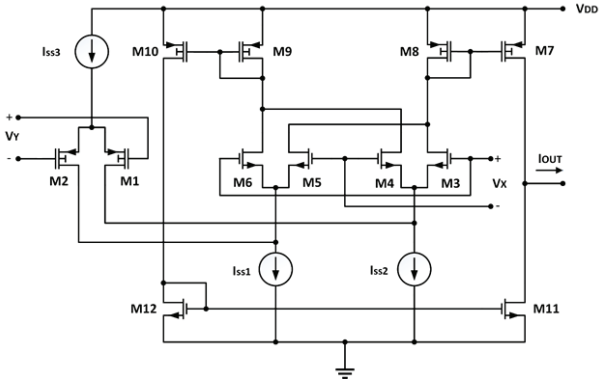

Figure 2: DTMOS based four-quadrant analog multiplier by using folded Gilbert cell

3 Simulation Results

Simulation results are presented in this section to evaluate the performance of DTMOS based folded Gilbert cell four-quadrant analog multiplier. The design verified by the Cadence Environment using 0.18 µm TSMC CMOS technology model parameters under 0.2 V supply voltage and $I_{SS1} = I_{SS2} = I_{SS3} = 100$ µA. Dimensions of the transistors are given in Table 1. Layout of the proposed DTMOS based Analog Multiplier is given in Figure 3.

Table 1: Aspect ratio of the analog multiplier

Transistor	W(µm)	L(µm)
M1, M2, M8, M9	20	0.26
M7, M10	10	0.26
M3-M6, M11, M12	1.3	0.26

The DC transfer characteristic of DTMOS based analog multiplier is given in Figures 4 and 5. For the proposed multiplier topology, the transfer curve I_{OUT} versus V_X and I_{OUT} versus V_Y are shown in Figure 4 and Figure 5 respectively. In Figure 4, V_Y is swept from −200 mV to 200 mV while V_X is varied from −200 mV to 200 mV in step size of 100 mV. In Figure 5, V_X is swept from −200 mV to 200 mV while V_Y is varied from −200 mV to 200 mV in step size of 100 mV. Figures 4 and Figure 5 show that the proposed multiplier can be easily used as four quadrant multiplier.

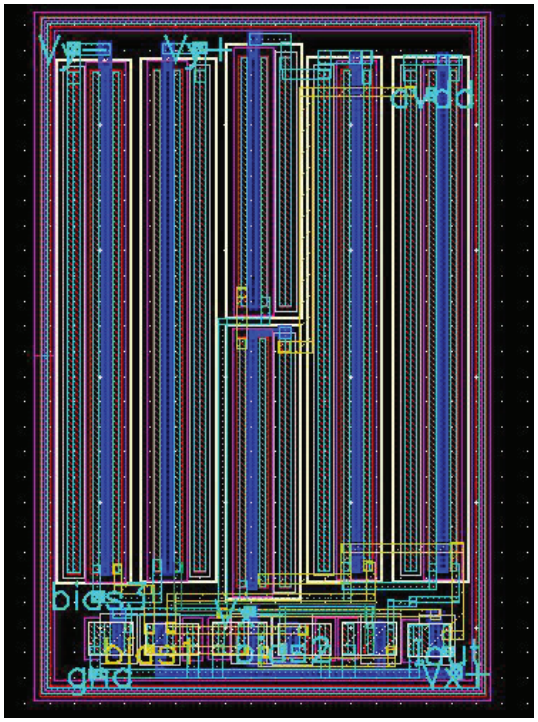

Figure 3: The layout of the proposed analog multiplier (Chip area of the proposed structure is 491.4 µm^2.)

In order to evaluate the AC transfer characteristics of DTMOS based analog multiplier, the input voltage V_X 100 mV DC is kept constant while the other input voltage V_Y 100 mVp-p AC is applied. The frequency response characteristics of the analog multiplier are shown in Figure 6. -3 dB bandwidth of the proposed structure is 1.4 GHz and 1.2 GHz for the schematic and post layout simulations respectively.

To evaluate the performance of the DTMOS-based analog multiplier as an amplitude modulator, two sinusoidal signals with 200 mV amplitude at 10 kHz and 300 kHz frequencies were applied to the inputs, respectively. The multiplier can be used as a modulator is shown in Figures 7 and 8.

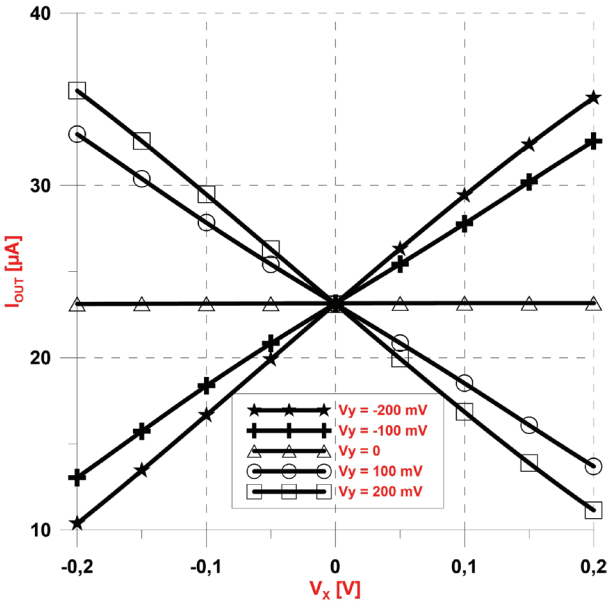

Figure 4: DC characteristics of the proposed multiplier versus V_X with V_Y as a parameter.

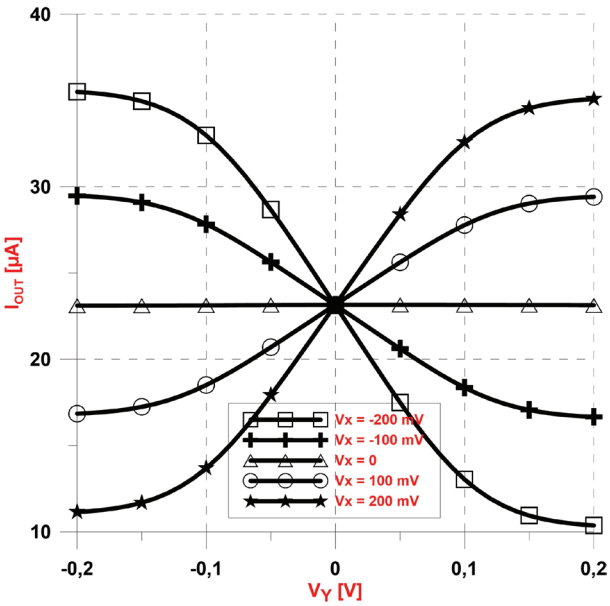

Figure 5: DC characteristics of the proposed multiplier versus V_Y with V_X as a parameter.

Intermodulation distortion for analog multipliers is a performance criterion just like total harmonic distortion. Ideally, the total harmonic distortion at the output of a multiplier is zero and no intermodulation products are presented. Intermodulation products arise as a result of the non-linearity of analog multipliers. Table 2

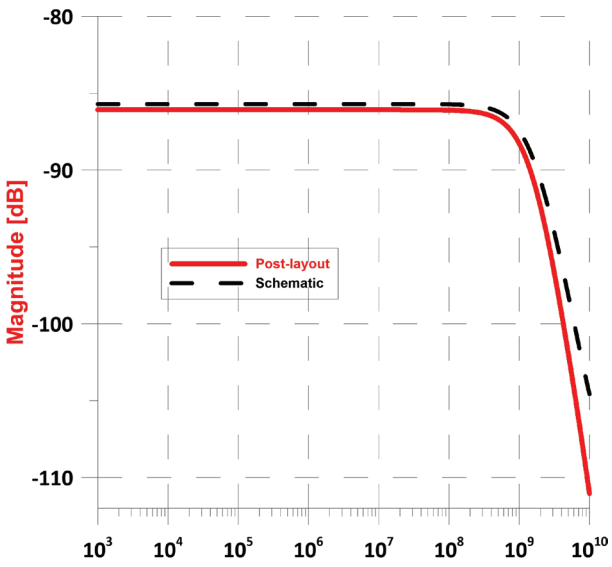

Figure 6: AC characteristics of the proposed multiplier for post layout and schematic simulations

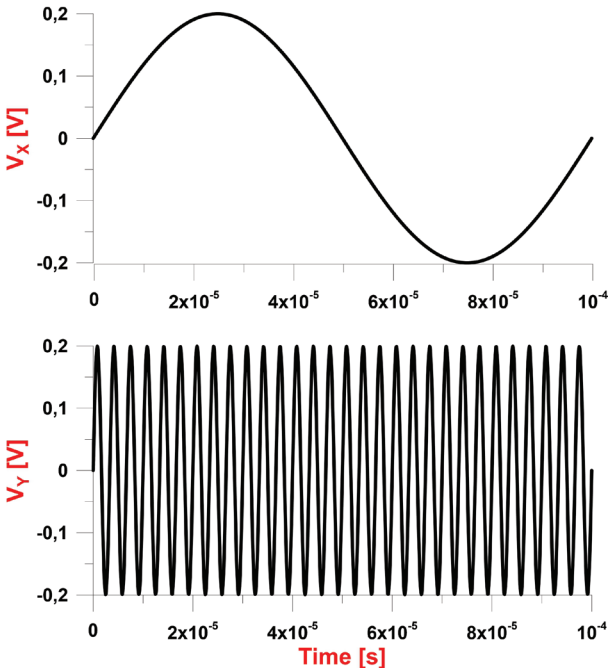

Figure 7: V_X (10 kHz) and V_Y (300 kHz) input signals applied to the proposed multiplier.

shows the 2nd, 3rd, 4th and 5th degree intermodulation products of the signal at the output of the proposed multiplier. Two sinusoidal signals were applied to the inputs of the analog multiplier at frequencies f_1 = 10 kHz and f_2 = 300 kHz. Furthermore, the frequency spectrum of the output of the proposed multiplier is given in Figure 9.

To evaluate the total harmonic distortion (THD) of the output signal of the proposed multipliers, a constant

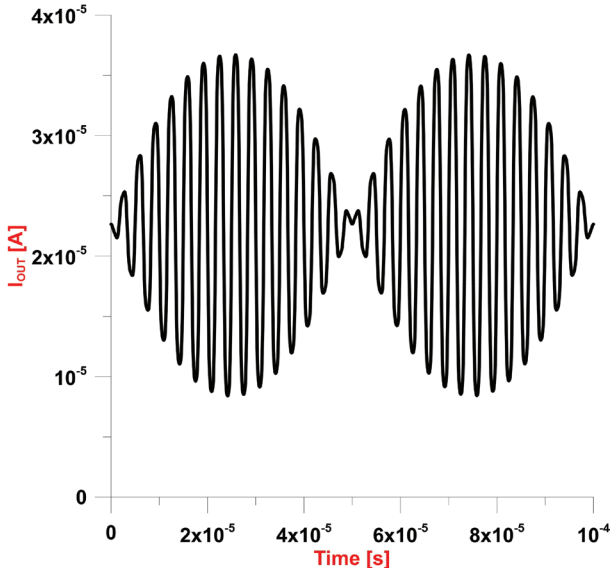

Figure 8: Output of the proposed multiplier as an amplitude modulator

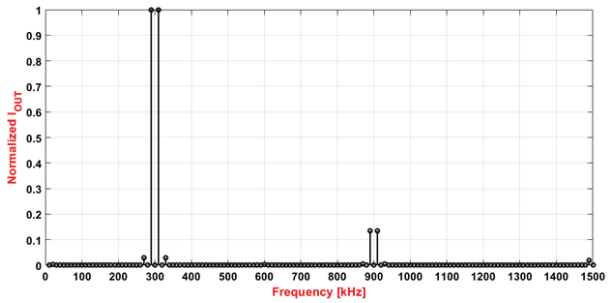

Figure 9: Frequency spectrum of the proposed multiplier as an amplitude modulator

DC voltage of 200 mV was applied to the V_Y input, while a sinusoidal signal with a frequency of 1 kHz, 10 MHz and 100 MHz were applied to the V_X input. The THD of the output voltage of the proposed multiplier is given in Figure 10 as a function of the input signal. THD [%] is composed of 9 harmonics and it is considered that the maximum THD is below 3% for the total scope of the input signal.

In order to evaluate the performance of the proposed multiplier as a frequency doubler, a sinusoidal signal of 100 mV amplitude and 10 kHz frequency was applied to both inputs of the multiplier. The accuracy of the frequency doubler function for the proposed multiplier is indicated in Figure 11.

The variation of AC and DC characteristics of the proposed multiplier with temperature is investigated. The temperature changes from 0 to 100 ° C, while the change in AC characteristic is shown in Figure 12. The DC characteristic change in the same temperature

Table 2: Intermodulation products of the proposed multiplier.

Order	Harmonics [kHz]	Fourier Components	Normalized Fourier Components (dB)	Intermodulation Products [kHz]	Fourier Components	Normalized Fourier Components (dB)
2	20	2.90×10^{-8}	-24.55	290	8.26×10^{-6}	0
	600	2.02×10^{-8}	-26.12	310	8.26×10^{-6}	0
3	30	9.50×10^{-11}	-49.39	320	3.10×10^{-9}	-34.25
	900	1.80×10^{-9}	-36.62	590	7.70×10^{-11}	-50.30
				610	1.12×10^{-10}	-48.69
4	40	1.68×10^{-9}	-36.92	330	2.48×10^{-7}	-15.22
				580	9.48×10^{-9}	-29.40
				620	9.45×10^{-9}	-29.42
	1200	6.04×10^{-9}	-31.36	890	1.11×10^{-6}	-8.70
				910	1.11×10^{-6}	-8.70
5	50	8.59×10^{-11}	-49.83	340	1.06×10^{-9}	-38.92
				630	1.10×10^{-10}	-48.74
				880	7.19×10^{-10}	-40.60
	1500	6.70×10^{-11}	-50.91	920	7.94×10^{-10}	-40.17
				1190	1.51×10^{-11}	-57.38
				1210	5.62×10^{-11}	-51.67

change is presented in Figure 13. V_Y is swept from –200 mV to 200 mV while V_X is varied from –200 mV to 200 mV in step size of 100 mV.

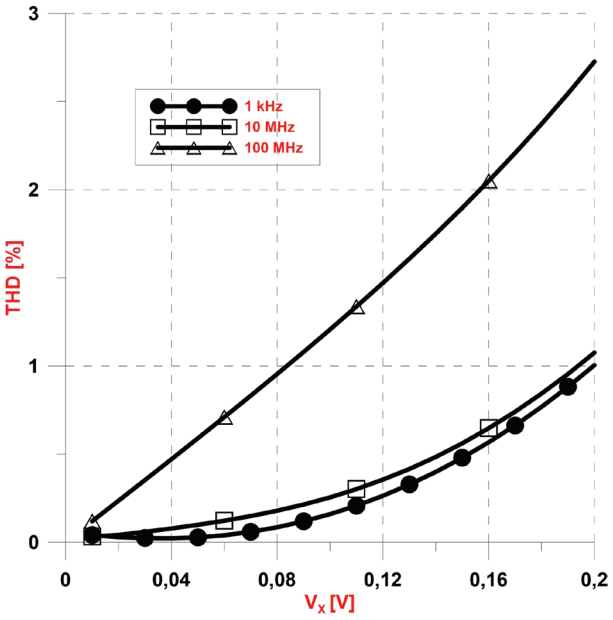

Figure 10: Relation between THD and V_X (peak) voltage with respect to 1 kHz, 10 MHz and 100 MHz frequencies.

The statistical distribution of the width (W) of the proposed multiplier circuit for 10% mismatch is given in Figure 13 for 200 runs. The histogram showing the statistical distribution in Figure 14 according to the 10% mismatch change in transistor width is given in Monte

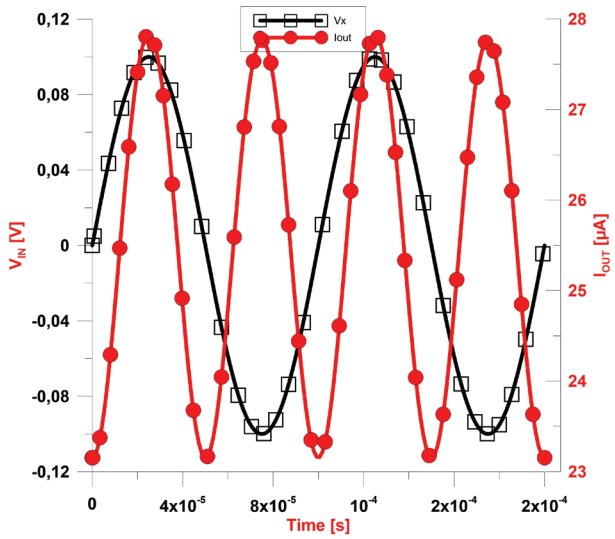

Figure 11: Output of the proposed multiplier as a frequency doubler.

Carlo analyses. According to the histogram, maximum bandwidth reaches up to 1.309 GHz whereas minimum bandwidth is 1.105 GHz. Also, average value is given as 1.230 GHz according to the post layout simulations. In addition to the 10% mismatch in width (W), the analysis made by adding 10% mismatch change in t_{ox} and V_{TH} process parameters is presented in Figure 15. In the histogram showing the statistical distribution here, the maximum bandwidth is 1.360 GHz and the minimum bandwidth is 1.114 GHz respectively. The average bandwidth is 1.23 GHz. All simulations have been done with post layout simulations.

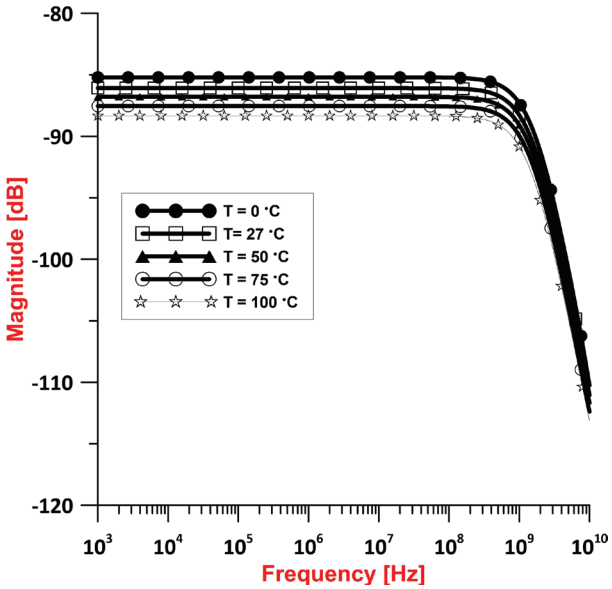

Figure 12: Post layout AC characteristic of the proposed multiplier when the temperature varies from 0 to 100 ° C.

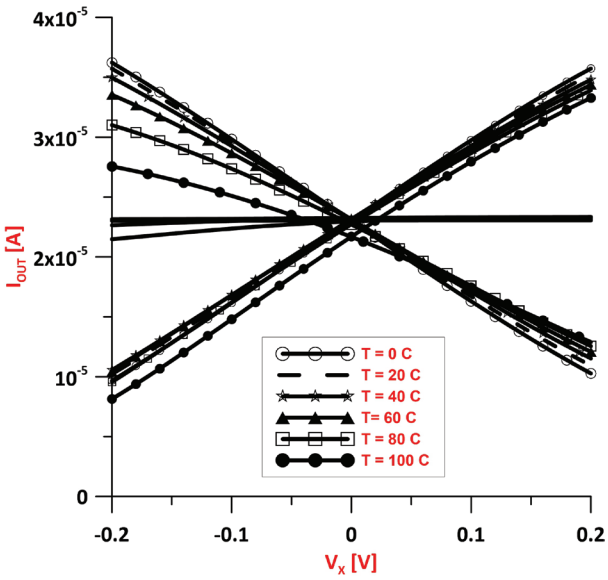

Figure 13: Post layout DC characteristic of the proposed multiplier when the temperature varies from 0 to 100 ° C.

Figure of Merit (FoM) is defined in order to compare the analog multiplier circuits in the literature with the proposed multiplier. Definition of FOM is:

$$\mathrm{FoM} = \frac{\mathrm{Bandwidth\,(MHz)}}{\mathrm{THD} \times \mathrm{Supply\_Voltage\,(V)} \times \mathrm{Power\_Consumption\,(\mu W)}} \quad (5)$$

where bandwidth is in (MHz), THD in (%), supply voltage in (V), and power consumption is evaluated in (μW). The FoM value of the proposed multiplier outperforms the other multipliers in the literature. Table 3 shows the comparison of the multiplier according to FoM value and various performance criteria with the existing multipliers in the literature. The circuits with higher FOM values are superior to the others. According to this, the FoM value of the circuit we recommend is 162.08, while the FoM value of the nearest circuit [30] is nearly four times less.

Table 3: Comparison table of the proposed multiplication circuit with previous studies

Ref	Year	Tech.	Power Supply	Bandwidth	THD (Frequency, Voltage)	Power Consumption	Input Range	FoM
[4]	2014	0.25 μm	±1.25 V	NA	1.62% (1 MHz, 125 mV)	4.02 μW	125 mV	-
[5]	2011	0.35 μm	2 V	1.5 GHz	2.67% (1 MHz, 1 V)	NA	±1 V	-
[6]	2018	0.25 μm	±0.75 V	NA	3% (1 MHz, 200 mV)	777 μW	±200 mV	0.002*
[7]	2005	0.5 μm	±1.5 V	25.34 MHz	4.667% (1 MHz, 1 V)	1.6 mW	±1 V	0.0011
[31]	2000	0.35 μm	±1.5 V	1.3 GHz	0.9% (1 MHz, 1V)	2.6 mW	±1 V	0.1851
[32]	2006	0.35 μm	±2.5 V	30 MHz	0.62% (NA)	1.2 mW	±400 mV	0.0080
[11]	2013	0.18 μm	0.5 V	221 kHz	5.8 % (1 kHz, 50 mV)	714 nW	±80 mV	0.1067
[33]	2010	0.35 μm	1.5 V	268 kHz	4.2 % (10 kHz, NA)	6.7 μW	±120 mV	0.0063
[34]	2015	0.18 μm	1.8 V	1.45 GHz	0.37 % (1 MHz, 0.5 V)	84 μW	500 mV	25.9187
[26]	2012	0.13 μm	0.5 V	10 MHz	1.4 % (NA, 0.5 V)	1.56 μW	±600 mV	9.157
[30]	2010	0.18 μm	1.2 V	2 GHz	1.5 % (NA)	25 μW	±200 mV	44.4444
[24]	2019	0.18 μm	±0.2 V	1.11 MHz	3.7 % (1 kHz, 100 mV)	18.4 nW	±200 mV	40.760
[35]	2009	0.25 μm	±0.5 V	250 MHz	NA	NA	NA	-
[23]	2019	0.5 μm	3.3 V	50 MHz	lower 1 % (1 kHz, 0.2 V)	660 μW	±200 mV	0.022
Proposed#	2020	0.18 μm	0.2 V	1.2 GHz	0.83 % (10 MHz, 100 mV)	44.6 μW	200 mV	162.08

*Bandwidth is defaulted to 10 MHz.
Data are post layout simulation results

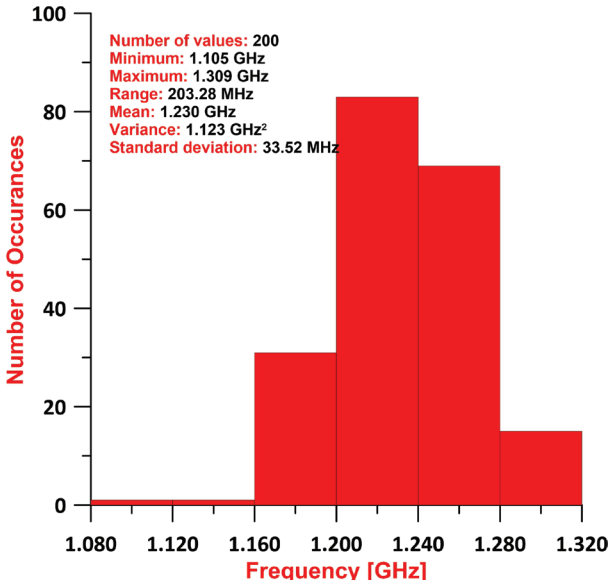

Figure 14: The bandwidth distribution of analog multiplier depending on MOSFET widths (W)

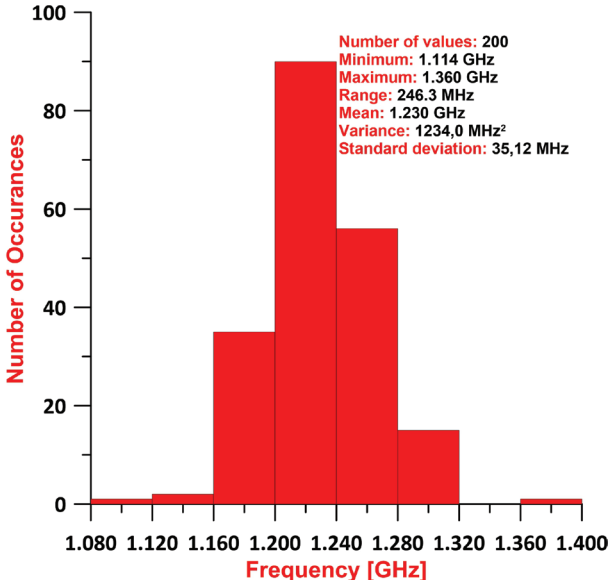

Figure 15: The bandwidth distribution of analog multiplier depending on process parameters (t_{ox} and V_{TH}) and MOSFET widths (W)

4 Conclusion

In this study, a four-quadrant analog multiplier in with voltage input and current output is presented. The circuit is designed using dynamic threshold MOS and folded Gilbert cell structure. The circuit has advantageous parameters such as wide bandwidth, low supply voltage, low power consumption and low THD. Also, the proposed structure is tested in various applications to evaluate circuit performance. Intermodulation products are given to show the efficiency as a modulator. Compared with the studies in the literature, it stands out with its wide bandwidth and low power consumption.

5 Acknowledgement

All simulations have done with Cadence Design Environment in 0.18µm TSMC CMOS technology. In this respect, we are thankful to Istanbul Technical University VLSI Laboratories for the Cadence Design Environment support.

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