

Multi-Port Memory Design in Quantum Cellular Automata Using Logical Crossing

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Abstract: Memory and its data communication play a vital role in deciding the performance of a Processor. In order to obtain a high performance computing machine, memory access has to be equally faster. In this paper, Dual port memory with Set/Reset is designed using Majority Voter in Quantum-dot Cellular Automata (QCA). Dual port memory consists of basic functional blocks such as 2 to 4 decoder, Control Logic Block (CLB), Address Checker Block (ACB), Memory Cell (MC), Data Router block and Input/Output block. These functional units are constructed using the 3-input majority voters. QCA is one of the recent technologies for the design of nanometer level digital components. The functionality of Dual Port Memory has been simulated and verified in QCADesigner 2.0.3. A novel crossover method called Logical Crossing is utilized to improve the area of the proposed design. The logical crossing does the data transmission with the support of proper Clock zone assignment. The logical crossing based QCA layouts are optimized in terms of area and number of cell counts. It is observed that 29.81%, 18.27%, 8.32%, 11.57% and 3.69% are the percentage of improvement in the number of cells in Decoder, ACB, CLB, Data Router and Memory Cell respectively. Also, 25.71%, 16.83%, 8.62%, 4.74% and 3.73% of improvement is achieved in the area for Decoder, ACB, CLB, Data Router and Memory Cell respectively. In addition to that the proposed Dual port memory using logical crossing attains improvement in the area by 8.26%; that is made possible due to the 8.65% reduction in the number of cells required for its construction. Moreover, the quantum circuits of the RAM are obtained using the RCViewer+ tool. The quantum cost, constant inputs, the number of gates, garbage output and total cost are estimated as 285, 67, 57, 50 and 516 respectively.

Keywords: Dual Port memory; Logical Crossing; Number of Cells; Total Cost

Večvhodni spominski dizajn kvantnih celičnih avtomatov z uporabo logičnega križanja

Izveček: Učinkovitost procesorja je odvisna od spomina in podatkovne komunikacije. Članek opisuje dvovhodni spomin s set/reset z uporabo večinskega volivca v kvantnem celičnem avtomatu (QCA). Dvovhodni spomin je sestavljen iz osnovnih funkcijskih blokov, kot so: 2-4 dekoder, kontrolni logični blok (CLB), blok preverjanja naslovov (ACB), spominska celica (MC), podatkovni usmerjevalni blok in vhodno izhodni blok. Te funkcionalne enote s zgrajene z uporabo trovhodnih večinskih volilcev. Funkcionalnost je bila simulirana in preverjena v QCADesigner 2.0.3. Uporabljen je nova metoda logičnega križanja, ki opravlja prenos podatkov s podporo pravilne ure. Izboljšave v številu celic v dekoderju, ACB, CLB, usmerjevalniku in spominski celici znašajo 29.81%, 18.27%, 8.32%, 11.57% in 3.69% in izboljšavi v površini dekoderja, ACB, CLB, usmerjevalnika in spomske celice v višini 25.71%, 16.83%, 8.62%, 4.74% in 3.73%. Skupna površina je manjša za 8.26%. Kvantna vezja RAM so narejena v RCViewer+ orodju.

Ključne besede: dvovhodni spomin; logično križanje; število celic; strošek

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1 Introduction

In a processor, the memory plays a critical role in deciding the performance of computation. The main characteristics of RAM are Reliability, Availability and Maintainability. The computation speed depends upon

the design of memory architecture and the speed of communication. The communication speed indirectly depends on the architectural design of memory. The improvement in architectural design increases the performance of the system.

In CMOS (Complementary Metal Oxide Semiconductor), the memory architecture has nearly reached its saturation point. There comes a need for technological improvement at this moment, which can be achieved through the realization of digital structures in nanometer quantum cellular automata (QCA) [1]. QCA is a fast, ultra-low power and provides high packing density compared to other emerging nanotechnologies [1]. Further, the performance of the QCA can be enhanced by incorporating novel architectures. Generally, coplanar (single layer) and multilayer crossing is adopted in QCA wiring. However, usage of Multilayer architecture consumes less area and exhibits higher performance compared to coplanar wiring [2]. Logical Crossing is a new kind of wire crossing that exhibits a better performance than its predecessors. [3].

Two kinds of memory architectures can be realized in QCA. They are (1) line based and (2) loop based memory. In line-based memory, the four QCA clocking signals are used for storing the values in the cell; whereas the loop-based structure maintains the data using feedback in the circuit [1, 4]. The line-based method is very simple, but the reliability is questionable. While the loop-based method has better reliability and it is realized using multiplexer logic and latches [5].

The remaining parts of the paper are organized as follows; Section 2 explains the definitions of performance measures. Section 3 discusses the outcomes of the RAM related literature reviews. Section 4 deals with the novel logical crossing for interconnections in QCA. Section 5 elaborates on the proposed RAM design and its QCA realization. The simulation results obtained are discussed in Section 6. Finally, the paper is concluded with suggestions for future research.

2 Preliminaries performance metrics

2.1 Quantum Cost

The Quantum Cost of a circuit is defined as the total number of elementary quantum gates (primitive gates) that are needed to realize a given function [6]. The quantum cost of reversible preliminary gates such as Feynman, Toffoli and Fredkin gates are 1, 5 and 5 respectively [6].

2.2 Garbage Output

Garbage Output is defined as the number of unused outputs of the reversible circuit. Based on the requirement, these outputs are introduced to maintain the property of reversibility in the circuit [7].

2.3 Constant Input

Constant Input is a predefined input (Logic '0' or '1') in order to obtain the desired output function from the reversible gate. The input is kept constant at either '0' or '1' during the entire computation.

2.4 Logical Calculations

It is defined as the number of NOT (γ), AND (β) and XOR (α) operations that are required to obtain a desirable output function in reversible logic [8]. It indicates the hardware complexity of the circuit.

2.5 Number of Gates

It is the total number of gates required to realize the desired function. It is measured from the circuit's input to its output.

2.6 Total Cost

It is a sum of the Quantum Cost, Constant Input, Garbage output and Number of Gates.

2.7 QCA

Due to the increasing growth of electronic tools, parameters such as speed, area, processing power, energy consumption and density in the design of these tools are highly important [9]. In this regard, new technologies and designs are always being presented to resolve the disadvantages and make necessary improvements. One of the proposed technologies that try to advance in the digital electronics industry is quantum cellular automata (QCA) nanotechnology. This technology, which progresses constantly, has higher speed, density; also consumes far lower area and energy compared to the existing technologies [10].

In QCA technology, there can be two types of cells, which are 45° and 90° cells. A QCA cell contains four quantum dots that are located in the square corners. The electrons occupy the two corners of the QCA cell diagonally. A QCA wire can be designed simply by placing QCA cells next to each other. The length of the QCA wires should not be high since it leads to signal drop and can cause trouble in the circuit operation. Once the polarization of a QCA cell is fixed, the encoded binary information is transferred to the adjacent cells [11].

The three input majority gate and inverters are the basic structures of QCA circuits. Designing this gate is difficult in other technologies, but in this technology, the five QCA cells are arranged in a way to generate the majority gate. According to the structure and equation

of three input majority gate, it is observed that the AND and OR gates can be constructed based on two inputs by inserting a fixed value into one of the three input cells (logical one for OR and logical zero for AND) [12].

2.8 QCA Clocking

Every QCA based circuit requires a clocking mechanism for synchronization, flow control management, and provision of power to stimulate a circuit. This synchronization process is performed through QCA Clocking [13] as shown in Fig.1. The clocking of QCA can be accomplished by controlling the potential barriers between adjacent quantum dots.

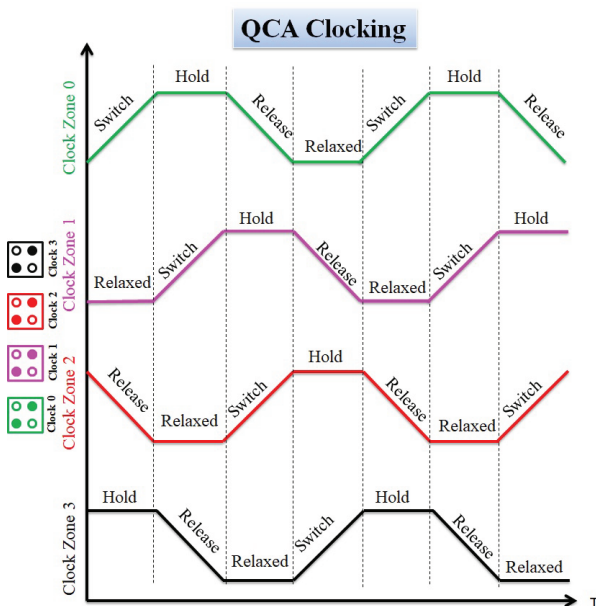


Figure 1: QCA Clocking (4 Clock Zones)

In QCA, the data flow path is based on the path along which the clocking phase increases [14]. It must be noticed that clocking phases should increase in turn unless the circuit does not function as expected. The control of data flow is one of the specific characteristics

of QCA. This inherent characteristic helps designers in developing more optimized novel structures for digital circuits [15].

3 Related works in RAM

Timing of the clocking zones requires two additional clocks to implement a four step process for reading/writing data to the memory in line based parallel memory [16]. The parallel hybrid memory architecture reduces the area and latency. The area, number of interconnection and latency can be improved by proper QCA layout [17].

Various kinds of RAM architectures are presented and their performances are analyzed in terms of number of cells, area, number of clocks and cell delay as shown in Table 1. Then the best and worst-case performances are identified based on the latency and area of the presented layout design [5]. Set/Reset signals are introduced in the recent RAM cell designs. The inclusion of Set/Reset does not increase the number of gates [18], but the number of gates is reduced in [19] through optimum realization. The number of QCA cells increases when the RAM layout is realized using regular clock zones with Latches (D or SR), but it reduces the clock latency [20]. The number of QCA cells, area, the number of gates and latency of RAM are reduced with the usage of 3-input and 5-input majority gate [19] in the architecture. Also, the removal of coplanar wires (crossover) [20, 21] and the effective layout arrangement of QCA cells make it a robust and noise free design [18, 19].

Initially, single port RAM is designed using SR/D Latch with Loop-based concept in QCA. The performance is improved by incorporating the 5-input majority gate and efficient layout design. But, the present-day processors are expecting RAM with multiple ports and high capacity. So recently, a 4x4 RAM is designed with two ports using majority voters in QCA [22, 23]. The major objective of this RAM design is to avoid cross-

Table 1: Comparison of RAM Designs present in the Literatures

RAM Design	Crossover	No. of Ports	Latch	Basic Building Blocks	Set / Reset	Number of Gates	Number of Clock Cells	Area (μm ²)	Latency
1x4 [21]	Coplanar (Loop Based)	Single Port Memory Cell	D	3-input Majority Voter & not Gate	No	8 (6+2)	158	0.16	2
1x1 [20]			SR		No	8 (6+2)	144	0.18	1
			D			6 (5+1)	132	0.21	1
1x1 [18]			D FF		Yes	8 (6+2)	109	0.13	1.75
1x1 [19]	No Crossover		D	5-input Majority Voter	Yes	4	88	0.08	1.5
4x4 [22]			-	3-input Majority Voter	Yes	6	40	0.048	0.75
4x4 [23]	Multilayer	Dual Port Memory Cell	-		Yes	-	-	-	-

ings in the entire layout [22]. But, multilayer crossing is adopted in [23] to reduce the number of cells and area.

3.1 Limitations of the existing design

From the above analysis of the existing RAM designs, the following observations are made,

- Single port memory is designed with or without crossover in [19-21].
- No array type architecture is presented so far except in [22, 23].
- Coplanar and multilayer crossings are used in [20, 21 and 23].
- In order to overcome the limitations of the existing designs, a Multiport 4x4 RAM is proposed in this paper, which is being realized in the QCA layout using Logical Crossing.

4 Logical crossing

Two major wire crossing techniques are popularly used in QCA data transmission: coplanar and multilayer. Each of them has its own advantages and disadvantages as shown in Table 2 [3, 24].

In order to combine the advantages of both methods, a new wire crossing technique is introduced in [3] named Logical Crossing. In logical crossing, the data are trans-

mitted to adjacent cells by operating them with clock signals shifted in phase by 180° clock phase. When two cells are in locked and locking stages, the Coulomb repulsion between them makes the data transmission possible. In other clock zones, the data transmission does not occur. The detailed clock zone information for data transfer in QCA is shown in Table 3.

Hence the cells in the hold and relax phase can cross each other without polarization effect. The diagrammatical view of data transmission in coplanar, multilayer and logical crossing are shown in Fig.2 and their corresponding QCA simulation waveforms are shown in Fig. 3. It is observed that the Logical Crossing uses Clock Zone 0 & 2 to pass Input A & B and Clock Zone 1 & 3 to transfer Input A & C to output.

The logical crossing method is used to construct XOR function [3], 2x1 multiplexer [25], Full Adder [26] and complex logical functions [24]. The incorporation of logical crossing in all these references reduces the number of cells and area in the QCA layout.

5 Proposed dual port RAM design

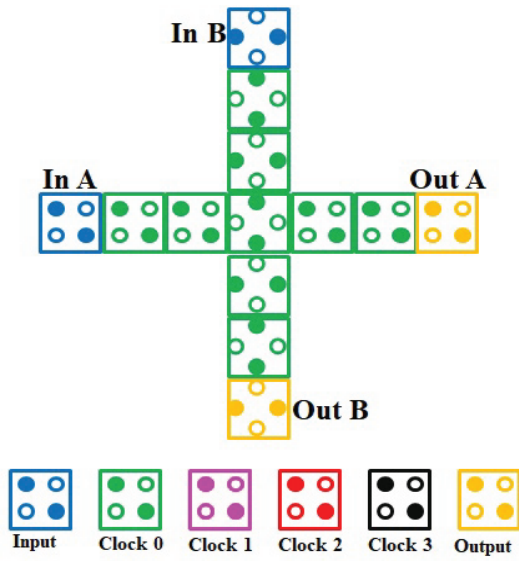
In dual port memory, a user can access two memory locations at a time. A data conflict may occur when two users access (among them at least one is write opera-

Table 2: Comparison of Wire Crossing Methods

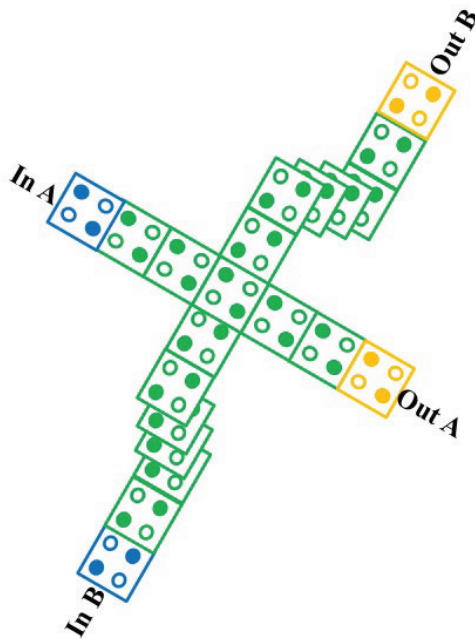
Wire crossing technique	Advantages	Disadvantages
Coplanar	<ol style="list-style-type: none"> 1. Single Layer. 2. Lower number of cells. 3. No additional layers and cells. 4. No noise interference. 	<ol style="list-style-type: none"> 1. Need additional space between (45° deg.) cells. 2. Decreased energy separation between the ground state and the first excited state. 3. Performance decreases (high operating temperature, resistance to entropy and switching time).
Multilayer	<ol style="list-style-type: none"> 1. No need to rotate the cells. 2. Good energy transformation. 3. Good performance (fast switching and high entropy). 	<ol style="list-style-type: none"> 1. Noise problem between intersection cells in the crossover area. 2. Number of layers, crossover and vertical cells are increased.

Table 3: Data Transfer in QCA

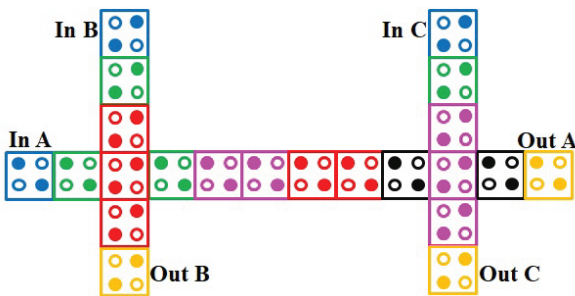
Clock Zones	State of Cells	Action & Data Transmission
Two adjacent clock cells (Clock Zone 1 & 3, Clock 2 & 4)	Locked and Locking stages pair.	Coulomb repulsion. Data transmission is performed within two cells.
Other Clock Zones Pairs	Locked and Relaxing stages.	Data transmission does not operate between two cells.
	Locking and Relaxed stages.	
	Locking and Relaxing Stages.	
	Locked and Relaxed stages pair.	Coulomb repulsion. Data transmission is not performed without any interference.



a. Coplanar Crossing



b. Multilayer Crossing



c. Logical Crossing

Figure 2: Wire Crossing Methods in QCA

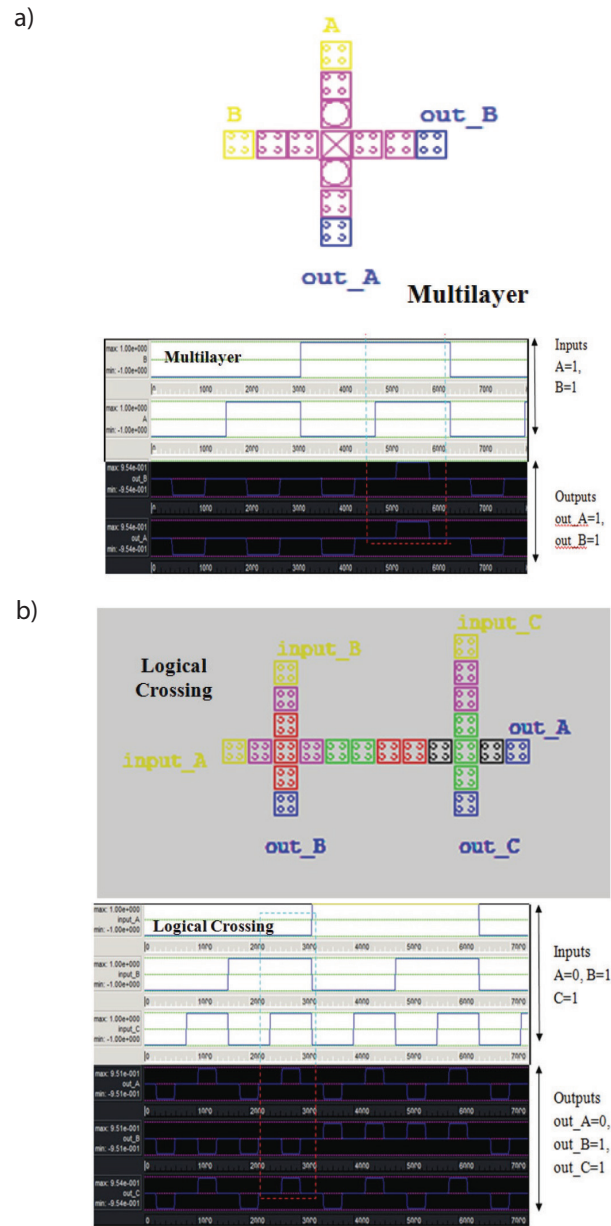


Figure 3: Simulation of Wire Crossing Methods in QCA, a) Multilayer Crossing and b) Logical Crossing.

tion) the same location at same time. The data conflicts can be avoided if one of the ports signal is stalled by delaying it. But this demands for additional buffers in QCA to introduce delay. So, to overcome this problem a priority-based dual port memory architecture is proposed. Fig.4. shows the proposed architecture..

Dual port memory architecture consists of decoder block, Address Checker Block (ACB), Control Logic Block (CLB), Data Router Block (DRB), Macro Memory Cell (MC) as shown in Fig. 5 (a to e). The decoder provides the address to the two ports (Port A and Port B). ACB checks the address of the two ports (i.e. to check whether the address of the two ports is the same). CLB

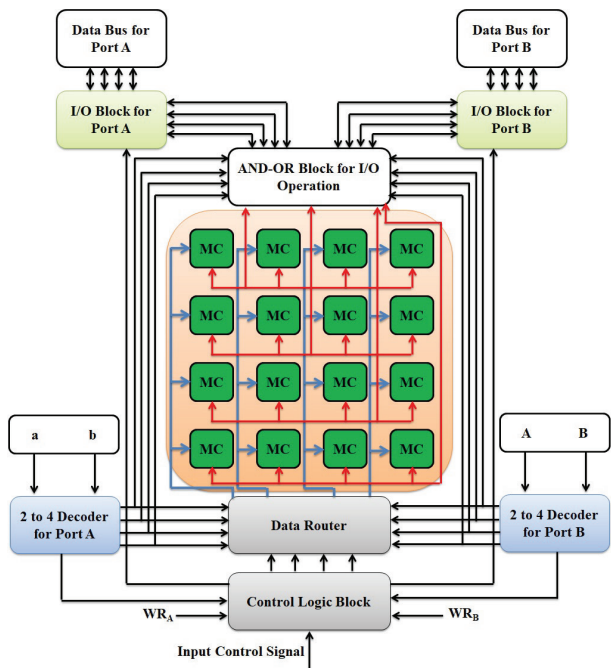


Figure 4: Block diagram of priority based Dual Port Memory.

generates the priority for the two ports, if Port A has higher priority, it accesses that memory cell first; followed by Port B. DRB provides the write/read operation (Data Route) to the two ports. Memory cell stores the single bit and it performs write/read operations.

5.1 Decoder

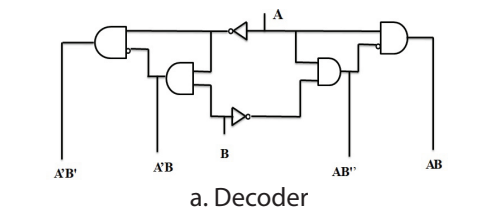
In dual port memory, two memory cells are selected at the same time for write/read operation. So, two decoders are used to generate the addresses for both the ports as shown in Fig.5a. The decoders are used to generate a ‘row select’ signal for addressing an appropriate memory array which is shown in Table 4.

Table 4: Truth Table of Decoder

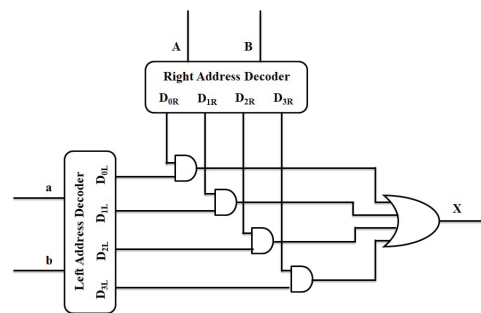
A	B	A'B'	A'B	AB'	AB
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

5.2 Address Checker Block (ACB)

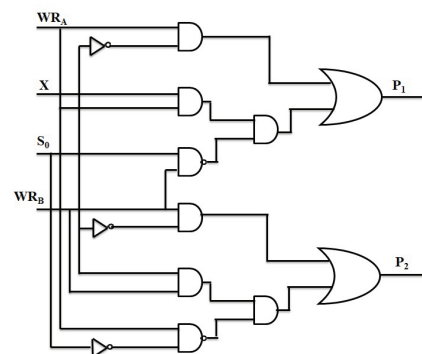
The addresses of the two decoders are compared to check whether they are similar or not. If the output of Address Checker Block (ACB) as shown in Fig.5b, X is ‘1’ then addresses of the ports are same. Table 5 shows the operational output of ACB, where D_{iR} and D_{iL} represent the right and left decoder outputs respectively. If D_{oR} and



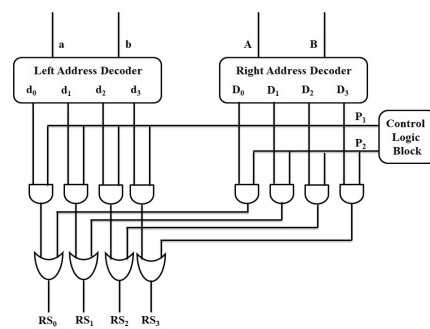
a. Decoder



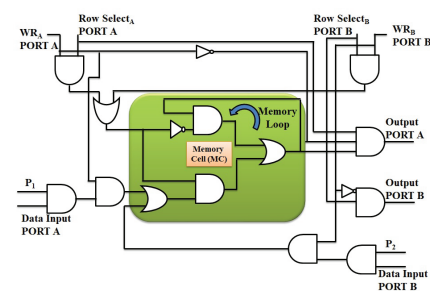
b. Address checker block



c. Control logic block



d. Data router



e. Memory cell

Figure 5: Block diagram of individual modules of Dual Port Memory a) Decoder b) Address Checker Block c) Control Logic Block d) Data Router and e) Memory cell.

D_{0L} have logic '1' the output is logic '1'. Similarly, all inputs logic is performed. The ACB works on a priority basis.

Table 5: Truth Table of ACB

D0R	D1R	D2R	D3R	D0L	D1L	D2L	D3L	X
1	X	X	X	1	X	X	X	1
X	1	X	X	X	1	X	X	1
X	X	1	X	X	X	1	X	1
X	X	X	1	X	X	X	1	1
0	0	0	0	0	0	0	0	0

5.3 Control Logic Block (CLB)

The control logic block (CLB) has inputs of Data Router signals of two ports and a control input. CLB produces the priorities as well as the Data Router for both ports. If the addresses are different, no conflict occurs at all. So, after the ACB block, if the addresses are unmatched, the control logic block simply passes the same Data Router data for both ports as supplied to the input lines of this block. For the same addresses, outputs will be chosen based on the control input (S_0) as per Table 6.

Table 6: Truth table for CLB priority calculation

S0	Inputs					Outputs	
	Address Port A	Address Port B	WR _A	WR _B	X	P ₁	P ₂
0	01	01	0	0	1	0	0
0	01	01	0	1	1	0	1
0	01	01	1	0	1	1	0
0	01	01	1	1	1	1	1
1	10	10	0	0	1	0	0
1	10	10	0	1	1	0	1
1	10	10	1	0	1	1	0
1	10	10	1	1	1	1	1
0	10	11	0	0	0	0	0
0	10	11	0	1	0	0	1
0	10	11	1	0	0	1	0
0	10	11	1	1	0	1	1
1	10	11	0	0	0	0	0
1	10	11	0	1	0	0	1
1	10	11	1	0	0	1	0
1	10	11	1	1	0	1	1

Table 7: Truth table for Data Router

a	b	d ₃	d ₂	d ₁	d ₀	A	B	D ₃	D ₂	D ₁	D ₀	P ₁	P ₂	RS ₀	RS ₁	RS ₂	RS ₃
0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0
0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1	0	0
1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	1	0
1	1	1	0	0	0	1	1	1	0	0	0	1	1	0	0	0	1

If the addresses are same and X is logic '1', S_0 is the conflict resolver, WR_A and WR_B have logic '0' then the priority outputs P_1 and P_2 are logic '0'. The priority and the port for write/read A/B is selected based on the address port and WR signal. In order to remove the conflicts, the conflict resolve factor (0 or 1) is used. When the same memory location is selected for both ports with at least one operation is write operation, then the priority of the two ports must be different. These priorities also work as the final write/read signals as shown in the following equations 1 to 4.

B_1 and B_2 can be defined by the following functions.

$$B_1 = XWR_A (S_0WR_B)'$$
 (1)

$$B_2 = XWR_B (S_0WR_A)'$$
 (2)

Therefore, conflict resolver functions as the write/read signals which satisfies all the following conditions (access of the same or different memory location),

$$P_1 = X'WR_A + XWR_A (S_0WR_B)' = X'WR_A + B_1$$
 (3)

$$P_2 = X'WR_B + XWR_B (S_0WR_A)' = X'WR_B + B_2$$
 (4)

Where, P_1, P_2 are the priority of port A and port B respectively.

5.4 Data Router

Priority generated in the CLB is used as the Data Router for ports A & B. At any point of time, one row is selected for port A/port B, for the intended operation. Hence, the Data Router and the address lines have to be combined as shown in Fig.5d. In Table 7, d_i is the left address decoder while D_i is the right address decoder, P_i is Port A/B and RS_i is memory array i for write/read operation. If the same memory location is selected for both the ports, then the write/read signal of the prior port is selected. Output signals $RS_1, RS_2, RS_3,$ and RS_4 are the Data Router signals for four rows.

5.5 Memory Cell

The memory architecture used in [27, 28] is modified according to dual port mode as shown in Fig. 5e. The

Table 8: Truth table of memory cell for Dual port memory

P ₁	P ₂	Data input		WR _A	RS _A	WR _B	RS _B	Output A	Output B
		Port A	Port B						
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	1	1	1
0	0	1	1	1	0	1	0	0	0
0	0	1	1	1	1	1	1	0	0
0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	1	0	1	1	1
0	1	1	1	1	0	1	0	0	0
0	1	1	1	1	1	1	1	0	0
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	1	1	1
1	0	1	1	1	0	1	0	0	0
1	0	1	1	1	1	1	1	0	0
1	1	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	1	1	1
1	1	1	1	1	0	1	0	0	0
1	1	1	1	1	1	1	1	0	0

stored data are constantly updated inside the memory loop until both the write/read and row select wires of the same port are enabled. If the row select is enabled and the write/read is logic '0', then the current memory value inside the loop is forwarded to the output. The data input of the prior port is considered as the input line of the memory cell. In Table 8, WR_i and RS_i are the write and the read operation of Port A and B, respectively.

5.6 I/O Operation

There are individual data inputs for each port. The selected input port data are forwarded to the Memory cell or data are transferred to the output port based on the CLB control signals. The operation is performed using AND-OR combinational logic.

6 Results and discussions

The above discussed dual port memory components are realized in quantum cellular automata (QCA) using logical crossing as shown in Fig.6 (a to e). It shows the QCA realization of Decoder, ACB, CLB, Data Router and Memory cell using Logical crossing based crossover. QCADesigner 2.0.3 [29] is used for this QCA layout design. The simulation waveforms of the individual modules of the RAM are shown in Fig.7. The simulation waveforms confirm the functional verification of the proposed RAM design. In Fig.7, the sample input and output simulation waveforms are shown, in which, for

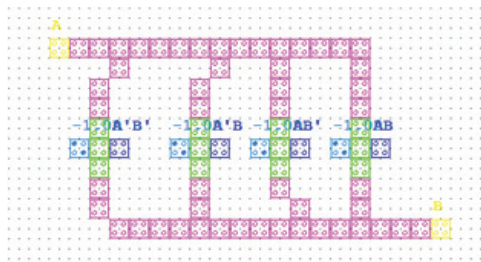
each module, one of the possible inputs and outputs is highlighted on the waveform and its logical value is represented on the right side.

Table 9: Comparison of Memory Cell implementation in QCA

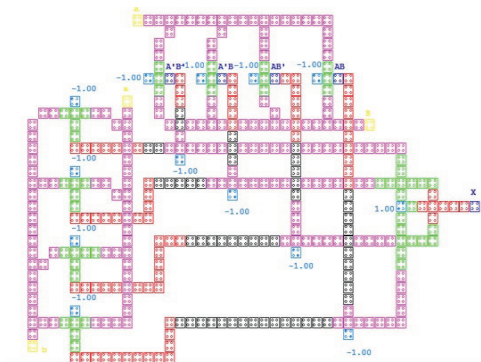
S. No.	Memory Cell References	Number of Cells
1.	[21]	158
2.	[20] with D Latch	132
3.	[18]	109
4.	[20] with SR Latch	100
5.	[19]	88
6.	Proposed	77

The QCA layout of individual modules of dual port RAM is realized using the logical crossing. The AND, OR and NOT are the basic logic units of the functional blocks of RAM. These logic units are constructed using 3-input majority voter and they are incorporated to build the decoder, ACB, CLB, Data Router and Memory cell. The interconnections between them are introduced by logical crossing, which has a positive impact on the performance measures.

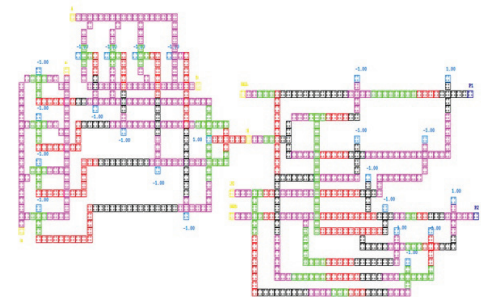
In [18-20], memory cell structure alone is implemented in QCA using multilayer/coplanar architecture. In [20], the inherent QCA capability is used to derive the Latch function. From Table 9, it is observed that the logical crossing in memory cell design reduces the required number of cells. When observing the logical crossing realization in Table 10, the inverter realization has 20%



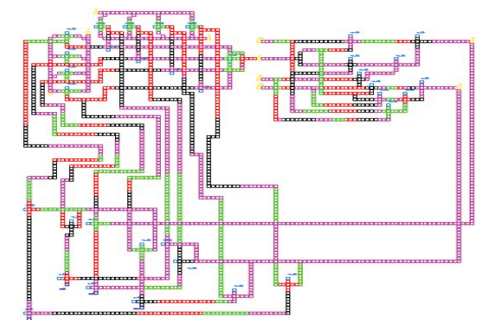
a. 2 to 4 Decoder



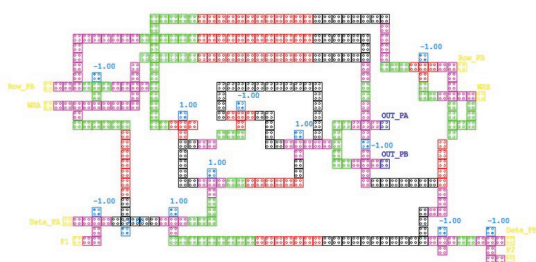
b. Address checker block



c. Control logic block



d. Data router



e. Memory Cell

Figure 6: QCA Realization of Dual port memory blocks

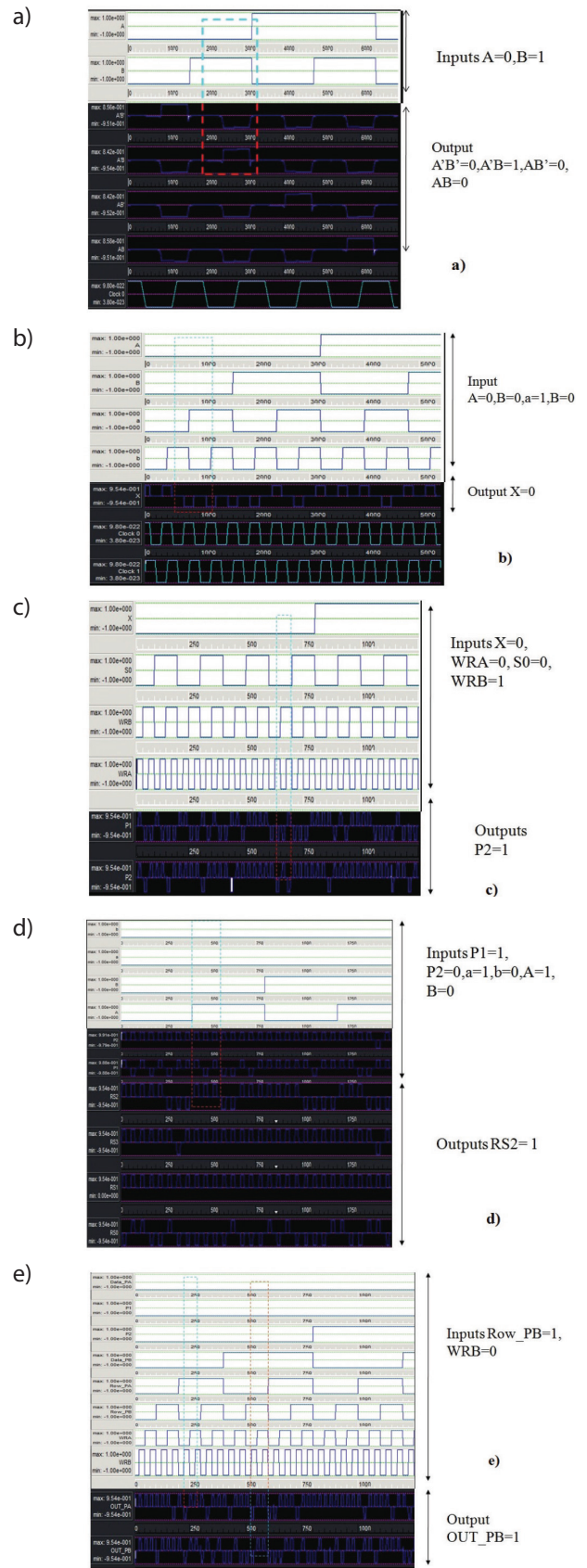


Figure 7: QCA Simulation of Dual Port RAM a) Decoder b) Address Checker Block and c) Control Logic Block d) Data Router and e) Memory cell.

Table 10: Comparison of Dual Port Memory

Components of RAM	Type and Number of functional units	Existing [22]			Proposed (Logical Crossing)			% of Improvement w.r.t. [22]		
		Number of Cells	Wires	Total	Number of Cells	Wires	Total	Number of Cells	Wires	Total
AND	-	5	0	5	5	0	5	0	0	0
OR	-	5	0	5	5	0	5	0	0	0
NOT		5	0	5	4	0	4	20	0	20
Decoder	4 AND, 2 NOT	30	74	104	28	45	73	6.67	39.19	29.81
ACB	2 Decoders, 4 AND, 1 OR	233	194	427	171	178	349	26.61	8.25	18.27
CLB	8 AND, 2 OR	477	328	805	421	317	738	11.74	3.35	8.32
Data Router Signal	2 Decoders, 1 CLB, 2 ACB, 8 AND, 2 OR	1917	530	2447	1676	488	2164	12.57	7.92	11.57
Memory Cell (MC)	3 NOT, 10 AND, 3 OR	80	300	380	77	290	367	3.75	3.33	3.42
4x4 MC	16 MC	1520	650	2170	1468	622	2090	3.42	4.31	3.69
Complete architecture	2 Decoders, Data Router, 4x4 MC, CLB, ACB	13620	11892	25512	12882	10423	23305	5.42	12.35	8.65

Table 11: Area comparison of Dual Port Memory

Modules of Dual Port Memory	Area occupied by		% of improvement w.r.t. [22]
	Existing layout [22]	Proposed (Logical crossing)	
2:4 Decoder	0.14	0.104	25.71%
Address checker block	1.01	0.84	16.83%
Control logic block	2.32	2.12	8.62%
Data Router	2.74	2.61	4.74%
Memory cell	0.51	0.491	3.73%
Total	6.72	6.165	8.26%

area reduction. In the decoder, the number of cells needed for providing interconnections is reduced by

39%. The decoder area is reduced by 29.81% compared to existing designs. The area reduction in the decoder

Table 12: Performance of Dual Port RAM

Modules of Dual Port Memory	Number of Primitive Gates		Quantum Cost	Constant Input	Number of Gates	Garbage Output	Logical Calculations	Total Cost
	Toffoli	Fredkin						
2:4 Decoder	4	2	30	8	6	4	$4\alpha + 2\beta + 4\gamma$	54
ACB	4	3	35	7	7	12	$4\alpha + 3\beta + 4\gamma$	68
CLB	10	4	70	18	14	12	$10\alpha + 4\beta + 10\gamma$	128
Data Router	12	-	60	12	12	10	$12\beta + 12\gamma$	106
Memory cell	15	3	90	22	18	12	$10\alpha + 4\beta + 10\gamma$	160
Total	45	12	285	67	57	50	$28\alpha + 27\beta + 50\gamma$	516

Where α is XOR, β is AND, γ is NOT gate functions

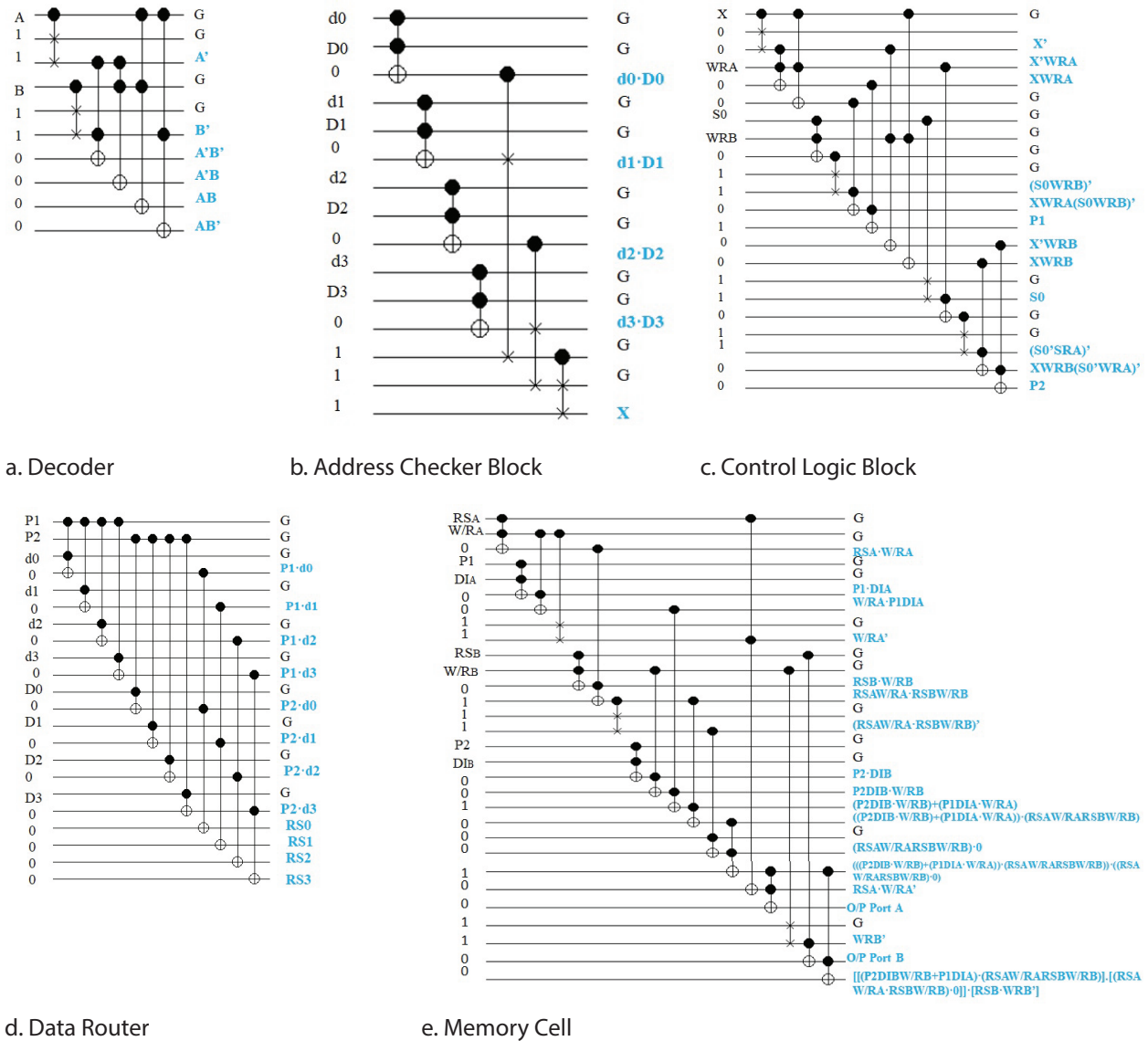


Figure 8: Quantum Equivalent Circuit of Dual Port RAM

is mostly due to the results of the area reduction of the ACB (up to 18.27%). Similarly, the control logic block has an 8.32% smaller area due to logical crossing. The AND and OR gates are the only logical elements in CLB, where the area is not reduced with logical crossing. Hence, the area reduction was possible only in the interconnections for CLB. Data router is a combination of CLB and ACB (for which the area is already reduced). This has a positive effect on the construction of data router resulting in area reduction up to 11.27%. The number of cells required for wire connections in the proposed methodology has been reduced significantly.

The realization of memory cell leads to a small area reduction of 3.42%. The area occupied by the 4x4 memory array is reduced by 3.69%. The complete architecture of the RAM is obtained by combining all the individual

modules, which results in a 12.35% area reduction compared to the existing designs due to the use of the logical crossing. Hence, the overall area reduction of 8.65% is achieved for RAM. Upon summarizing the obtained results, the functional units are integrated together to construct the 4x4 Dual Port RAM. In addition to that, it is observed from Table 11 that the reduction of number of cells in the RAM layout has been up to 8.26%.

The quantum circuit of the functional modules of RAM is obtained from Toffoli-Fredkin Code (.tfc) using RCViewer+ software [30]. In Fig.8, logic '1' and '0' denote the constant inputs and 'G' refers to garbage output. Here, Toffoli and Fredkin primitive gates are used to construct the RAM and their quantum cost is 5 [6]. The quantum cost of RAM is the sum of the quantum cost of the primitive gates used in the circuit. The quantum

cost, constant input, number of gates and garbage output are listed in Table 12.

From Table 12, the total cost of RAM is 516, which is the sum of quantum cost (285), number of constant inputs (67), number of gates (57) and number of garbage outputs (50). The number of logical calculations show the hardware complexity of the circuits.

7 Conclusion and future work

Quantum Cellular Automata is a low-power technology compared to present-day CMOS technology. In this paper, various functional blocks of Dual port memory such as 2 to 4 decoder, Control Logic Block (CLB), Address checker block (ACB), Data Router block and 4×4 memory cell block are designed using majority voters. The design unit consists of basic logic gates such as AND, OR, Inverter and connecting wires. All the functional modules are realized in the QCA layout with Logical Crossing. In Logical crossing method, the alternate clock signals are used to control the flow of data transmission rather than orientation and multiple layers for crossover. It has a positive impact on the cell count and reduces the area.

In comparison to the best published results from recent literature, it is worth mentioning that the number of cells is reduced by 29.81% (Decoder), 18.27% (ACB), 8.32% (CLB), 11.57% (Data Router) and 3.69% (Memory Cell) in the proposed work. Also, the area of the aforementioned blocks is reduced by 25.71%, 16.83%, 8.62%, 4.74% and 3.73%, respectively. In addition to that, the proposed logical crossing based complete Dual port memory achieves an improvement of 8.26% in area and 8.65% in number of cells. Moreover, the quantum cost, the number of constant inputs, the number of gates, the number of garbage output and the total cost are 285, 67, 57, 50 and 516 respectively. The work can be extended towards adding Asynchronous/Synchronous Set/Reset abilities to the dual port memory with increased memory array size.

8 Conflict of interest

The Authors of this Manuscript do not have any Conflict of Interest (COI) in publishing this paper.

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Arrived: 06. 04. 2020
 Accepted: 29. 01. 2021