

# *Superior Performance of a Negative-capacitance Double-gate Junctionless Field-effect Transistor with Additional Source-drain Doping*

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**Abstract:** In this work, we propose a negative-capacitance double-gate junctionless field-effect transistor (NC-JLFET) with additional source-drain doping. Superior performance of the NC-JLFET due to source and drain doping concentration is explained in detail. Additionally, the effects of the drain induced barrier lowering (DIBL) and negative differential resistance (NDR) are precisely analyzed in the NC-JLFET. Sentaurus TCAD simulation demonstrates that the additional source-drain-doped NC-JLFET exhibits a higher on/off current ratio ( $I_{ON}/I_{OFF}$ ) and steeper subthreshold swing ( $SS < 60$  mV/dec) compared to a traditional JLFET. Besides, the negative capacitance effect causes the internal voltage of the gate to be amplified, resulting in negative DIBL and NDR phenomena. Finally, the performance of NC-JLFET can also be optimized by choosing suitable ferroelectric material parameters, such as ferroelectric thickness, coercive field, and remnant polarization. Our simulation study provides theoretical and experimental support for further performance improvement of low-power NCFETs by local structure adjustment.

**Keywords:** Negative-capacitance double-gate junctionless field-effect transistor; additional source-drain doping; on/off current ratio; subthreshold swing; drain induced barrier lowering

## *Odlična učinkovitost dvovratnega brezspojnega poljskega tranzistorja z negativno kapacitivnostjo z dodatnim dopiranjem izvor-ponor*

**Izvleček:** V članku je predlagan dvovratni brezspojni poljski tranzistor z negativno kapacitivnostjo z dodatnim dopiranjem izvor-ponor (NC\_JLFET). Natančno je predstavljena odlična učinkovitost NC\_JLFET zaradi dodatnega dopiranja izvora in ponora. Analizirano je znižanje bariere (DIBL) zaradi ponora in negativna diferencialna rezistivnost (NDR). Sentaurus TCAD simulacije kažejo, da dodatno dopiranje izvora in ponora vodi v višjo tokovno razmerje ( $I_{ON}/I_{OFF}$ ) in strmejši podpragovni nihaj ( $SS < 60$  mV/dec). Negativna kapacitivnost povzroča ojačenje notranje napetosti vrat, ki se izkazuje v negativni DIBL in NDR efektu. Učinkovitost NC-JLFET je lahko optimiziran s pravilnimi parametri feroelektričnega materiala, kot je debelina, prisilno polje in preostale polarizacije. Simulacije ponujajo teoretično in eksperimentalno pomoč pri optimizaciji NCFET tranzistorja nizkih moči.

**Ključne besede:** dvovratni brezspojen poljski tranzistor z negativno kapacitivnostjo; dopiranje izvor-ponor; on/off tokovno razmerje; podpragovni nihaj; znižanje bariere

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### *1 Introduction*

With the continuous development of integrated circuits (ICs), device sizes have been gradually shrinking. The performance of traditional metal-oxide-semicon-

ductor field-effect transistors is approaching its limit. The off-state leakage current is increasing exponentially caused by the short-channel effect (SCE), resulting in unacceptable static power [1]. At the same time,

it has become difficult for inversion-mode field effect transistors (FETs) (IMFETs) to achieve ultra-deep doping concentration gradients at the device junctions, inducing increasing thermal budget [2]. To overcome these obstacles, some novel device structures have been proposed, including junctionless FETs (JLFETs) and ferroelectric negative-capacitance FETs (NCFETs) [3]-[5].

Compared with traditional inversion-mode transistors, JLFETs have stronger immunity to the SCE [6]. In the actual manufacturing process, there is no super-steep junction, and no additional dopants must be injected into the source and drain regions because the source and drain have the same doping polarity and concentration as the channel. Thus, JLFETs have a simpler manufacturing process and a lower thermal budget than IMFETs [7]. In JLFETs, the majority carriers are conducted in the center of the channel instead of the surface, and the majority carriers in the channel are completely depleted by the gate bias to shut down the device. Moreover, the multigate structure can effectively improve the gate-to-channel control capability, so JLFET devices usually use a double gate to achieve complete channel depletion [8]. It has been verified that the gate metal of JLFETs must have a work function greater than 5.0 eV to completely deplete the Si body to reach the off state [2]. However, it is difficult for a gate metal with a relatively large work function to meet the thermal stability requirement and achieve good adhesion to the gate dielectric [7]-[9]. Therefore, a novel mechanism or structure must be found to overcome this problem.

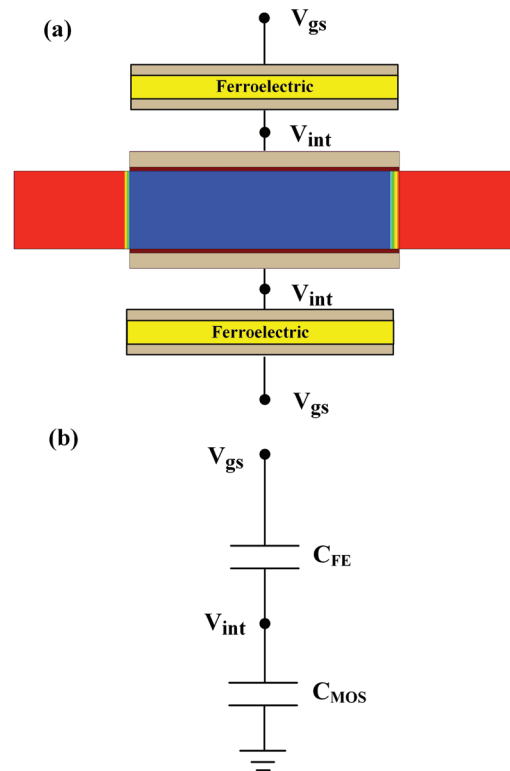
Since the NCFET was first proposed [4], there have been many reports on both IM and JL structures. A new transistor concept is proposed that combines ultra-thin body and NCFET in [10], It has been proved that performance improvement with low-power NCFETs is realized by amplifying the internal gate voltage caused by the negative-capacitance effect. Hu et al. studied the effects of the variation of ferroelectric material properties (thickness, polarization, and coercivity) on the performance of negative capacitance FETs (NCFETs) in [11]. In our previous studies, we discussed the capacitance matching problem caused by the change of ferroelectric parameters in IM devices, and the performance of NCFET in RF applications [12,13]. Yejoon Choi studied the electrical characteristics of NC-JL-NWFET based on HfO<sub>2</sub> through TCAD and MATLAB simulations [14].

In addition, some studies have shown that additional source-drain doping ( $N_{s/d}$ ) of a JLFET can increase the on-state current, but it also causes the higher subthreshold swing (SS) and the drain induced barrier lowering (DIBL) effect to become more prominent [15,16]. NCFETs can achieve steep SS and improve the DIBL effect, while greatly reducing operating voltage and power con-

sumption [17]-[18]. Therefore, by combining the above two points, the advantages of NCFET can offset the negative effects brought by the additional source-drain doping of JLFET, which can make NC-JLFET have more excellent performance. However, the effect of structure adjustment, such as additional source-drain doping, on the performance of an NC-JLFET has not yet been understood. So, in this work, we construct an NC-JLFET by stacking ferroelectric layers on the gate of the baseline JLFET and investigate the influence of additional source-drain doping on its electrical characteristics. Using Sentaurus TCAD simulation, it is demonstrated that additional source-drain doped NC-JLFETs have improved performance over traditional JLFETs, such as higher  $I_{ON}/I_{OFF}$ , steeper SS, and negative DIBL.

## 2 Device Structure and Simulation

Figure 1a shows a two-dimensional diagram of an NC-JLFET using a metal-ferroelectric-metal-oxide-semiconductor (MFMSIS) structure. The material of the insulating layer is SiO<sub>2</sub>; the channel, source, and drain are all N-type doped; source, drain, and channel. The channel is uniformly doped and the concentration remains fixed at  $1 \times 10^{19} \text{ cm}^{-3}$ . The source and drain are additionally doped with a concentration range of  $1 \times 10^{19} - 5 \times 10^{19} \text{ cm}^{-3}$ .



**Figure. 1:** Schematic of (a) NC-JLFET and (b) capacitance equivalent model.

Table I lists other specific device parameters for the proposed NC-JLFET. Among them, the parameters of the baseline transistor JLFET are the gate length  $L_g=28\text{nm}$ , the silicon channel thickness  $W=10\text{nm}$ [14], and the metal work function  $WK$  is  $5.0\text{eV}$ [2], these values of  $P_r$  and  $E_c$  are in the same range as those of ferroelectrics such as Hf- and Zr-based binary oxide ferroelectrics[11]. It is assumed that the inner and outer metals have the same work function and that the work function variation is not considered. Figure 1b is a schematic of the equivalent capacitance of the NC-JLFET, where  $C_{FE}$  is the ferroelectric layer capacitance and  $C_{MOS}$  is the gate equivalent capacitance of the baseline JLFET, including the insulation layer capacitance ( $C_{ox}$ ) and channel depletion capacitance ( $C_{dm}$ ).  $V_{gs}$  and  $V_{int}$  are the external gate voltage and internal node voltage, respectively. The baseline JLFET is connected in series with the ferroelectric capacitor to form the NC-JLFET. The Landau-Khalatnikov (LK) equation with Gibbs free energy is the standard model of the ferroelectric capacitor, specifically described as the electric field in a ferroelectric as a function of polarization [19]:

$$E_{FE} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{dP}{dt} \quad (1)$$

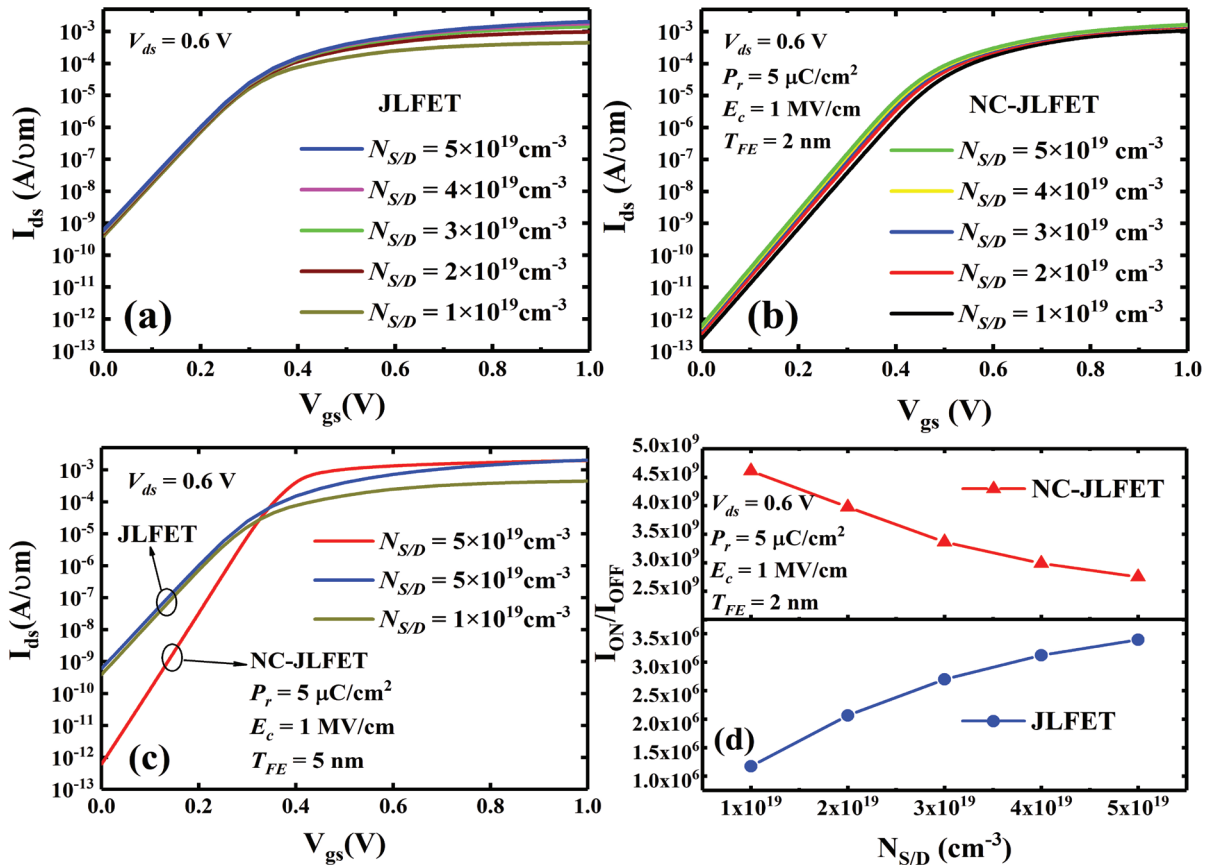
where  $\alpha$ ,  $\beta$ , and  $\gamma$  are material-dependent parameters of the ferroelectric,  $\alpha=-3\sqrt{3}/4 \times E_c/P_r$ ,  $\beta=-3\sqrt{3}/8 \times E_c/P_r^3$ , and  $\gamma = 0$  [20], the values of which fit the parameter range in  $\text{HfO}_2$ -based ferroelectrics [21]. The voltage across the ferroelectric capacitor can be obtained from:

$$V_{FE} = \left( 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{dP}{dt} \right) \times T_{FE} \quad (2)$$

**Table 1:** NC-JLFET device parameters

Parameter	Physical Meaning	Value
$L_g$	Gate length	28 nm
$W$	Thickness of channel	10 nm
$T_{ox}$	Oxide thickness	0.5 nm
$T_{FE}$	Ferroelectric thickness	1-5 nm
$WK$	Metal work function	5.0 eV
$E_c$	Coercive field	1-1.2 MV/cm
$P_r$	Remnant polarization	3-5 $\mu\text{C}/\text{cm}^2$

Poisson's equation and the continuity equation are solved self-consistently with the LK equation at the same time using Sentaurus TCAD. In simulation, we used some physical models, including doping de-



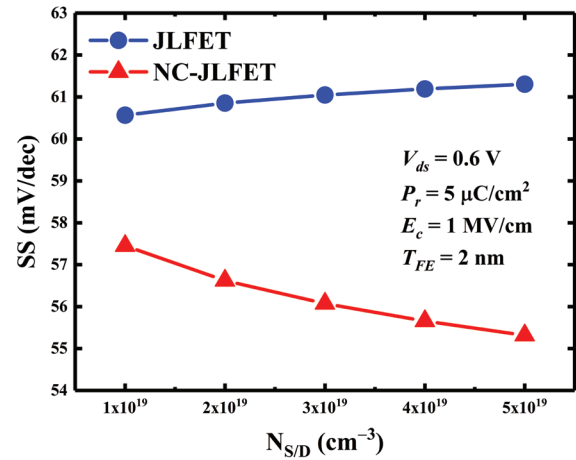
**Figure 2:** (a) Transfer characteristics of JLFET for different source and drain doping concentrations of source and drain ( $N_{S/D}$ ). (b) Transfer characteristics of NC-JLFET for different source and drain doping concentrations ( $N_{S/D}$ ). (c) Transfer characteristics of NC-JLFET and JLFET. (d)  $I_{ON}/I_{OFF}$  with source and drain doping concentrations ( $N_{S/D}$ ).

pendence, high-field saturation (velocity saturation) and considering the silicon bandgap narrowing, the old Slotboom model of band gap narrowing and the Shockley-Read-Hall model for recombination generation are also considered. In view of the highly doped source-drain regions, Fermi (also called Fermi-Dirac) statistics is necessary to make it more physically accurate. In addition, because the device dimension is very small, some quantum modification terms (eQuantum-Potential) are added for the simulation results to be closer to the real condition.

### 3 Results and Discussion

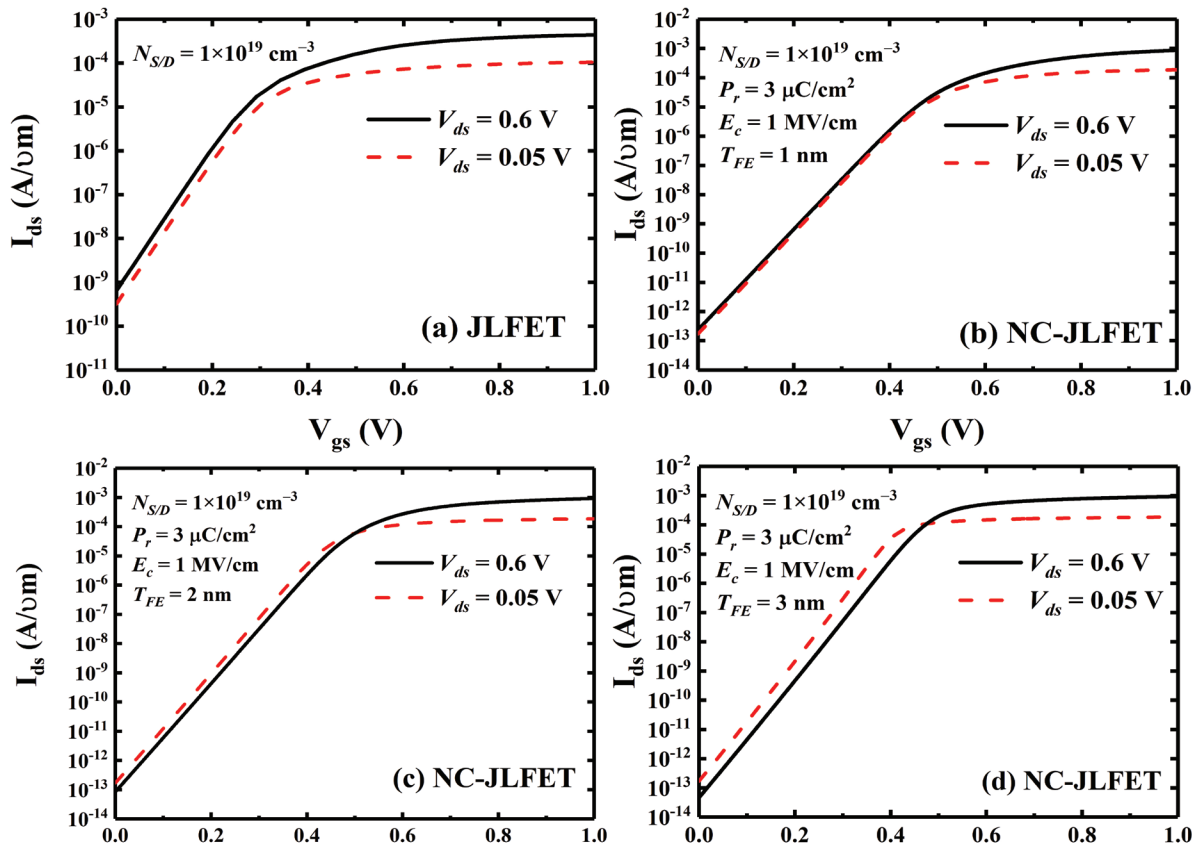
Discussed herein are details of the effects of different source and drain doping concentrations ( $N_{S/D}$ ), ferroelectric thickness ( $T_{FE}$ ), and  $E_c$  and  $P_r$  values on the on/off current ratio ( $I_{ON}/I_{OFF}$ ), SS, DIBL, and output characteristics ( $I_{ds}-V_{ds}$ ).

Figures 2a and b show the  $I_{ds}-V_{gs}$  transfer characteristics of JLFETs and NC-JLFETs with different  $N_{S/D}$  values, respectively. It is clear that, as  $N_{S/D}$  increases, the on current ( $I_{ON}$ ) increases more and the off current ( $I_{OFF}$ ) is al-



**Figure. 3:** Subthreshold swing (SS) of JLFET and NC-JLFET varying with source and drain doping concentration ( $N_{S/D}$ ).

most constant in JLFETs, but  $I_{ON}$  and  $I_{OFF}$  both increase slightly in NCJLFETs. Figure 2c is a comparison of the transfer characteristics of NC-JLFET and JLFETs. It is obvious that  $I_{OFF}$  is significantly reduced for NC-JLFETs, which leads to the result that the switching characteristic becomes steeper because of the voltage amplifi-



**Figure. 4:** DIBL characteristics of (a) JLFET and NC-JLFET with different ferroelectric thicknesses  $T_{FE}$  of (b) 1, (c) 2, and (d) 3 nm.

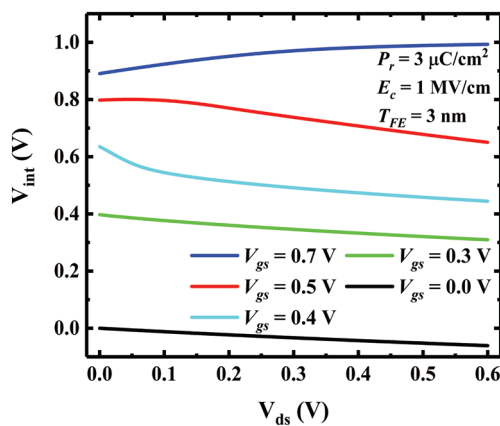
cation contributed by the ferroelectric layer. As shown in Fig. 2d, the on/off current ratio ( $I_{ON}/I_{OFF}$ ) of JLFETs increases with increasing  $N_{S/D}$  because increased  $N_{S/D}$  reduces the resistance of the source and drain, which increases the drive current. This trend is also in line with the conclusions obtained in [16,22]. However, for NC-JLFETs, the  $I_{ON}/I_{OFF}$  decreases as  $N_{S/D}$  increases. This is because increased  $N_{S/D}$  values induce doping-dependent electron mobility degradation [14]. Moreover, as the source and drain doping concentrations increase but the channel concentration remains constant, the  $I_{ON}/I_{OFF}$  values do not change much. When  $N_{S/D} = 5 \times 10^{19} \text{ cm}^{-3}$ , the  $I_{ON}/I_{OFF}$  value of the NC-JLFET is still larger than in the JLFET by a factor of nearly  $10^3$ .

Figure 3 gives the SS values of the JLFET and NC-JLFET for different  $N_{S/D}$  values. The SS in JLFET increases slowly with increasing  $N_{S/D}$  but, in the NC-JLFET, SS shows a downward trend and all are below 60 mV/dec. These two phenomena can be explained by the following two equations:

$$SS = \ln 10 \frac{kT}{q} \left( 1 + \frac{C_{dm}}{C_{ox}} \right) \approx 60 \times \left( 1 + \frac{C_{dm}}{C_{ox}} \right) \quad (3)$$

$$SS = 60 \times \left( 1 + \frac{C_{dm}}{C_{ox}} - \frac{C_{dm}}{|C_{FE}|} \right) \quad (4)$$

where  $C_{ox}$  is the gate oxide capacitance and  $C_{dm}$  is the depletion capacitance. As is well known, in JLFETs, the higher the doping concentration, the larger the  $C_{dm}$ , and therefore the larger the SS. In contrast, in NC-JLFETs, the larger the  $C_{dm}$ , the greater the increase of  $C_{dm}/|C_{FE}|$  compared with the increase of  $C_{dm}/C_{ox}$ , so the smaller the SS will be, that is, less than 60 mV/dec. This is the same as the change trend of SS caused by different doping concentrations of NC-JLGAAFET in [14].

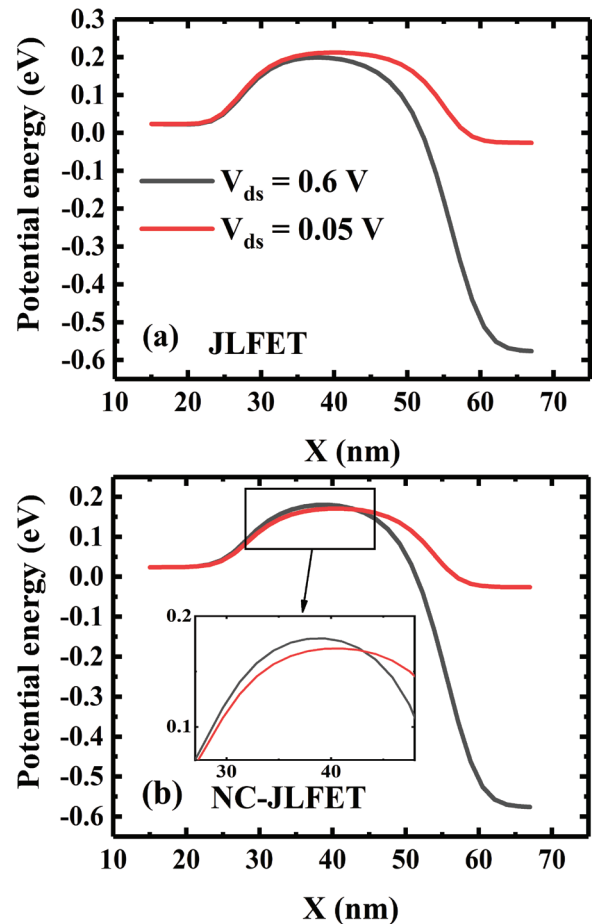


**Figure 5:** Gate internal voltage ( $V_{int}$ ) versus drain voltage ( $V_{ds}$ ) for NC-JLFET with  $T_{FE} = 3 \text{ nm}$ .

For conventional JLFETs, when the drain voltage ( $V_{ds}$ ) increases, the source-drain depletion layer width is close to the channel length, which reduces the source barrier height. The decrease of the barrier height allows the source electrons to easily cross the barrier to reach the drain, and the channel charge controlled by the gate voltage is reduced, which leads to increased leakage current and lowered threshold voltage. This mechanism is known as the DIBL effect. For traditional JLFETs, increasing  $V_{ds}$  will tend to increase current ( $I_{ds}$ ), as can be seen in Fig. 4a. However, for NC-JLFETs, the relationship between the  $V_{gs}$  and  $V_{int}$  is:

$$V_{int} = V_{gs} - V_{FE} = V_{gs} + |V_{FE}| \quad (5)$$

where  $V_{FE}$  is the voltage across the ferroelectric. Owing to drain and channel coupling, when  $V_{ds}$  increases, the gate charge decreases, which results in a decrease in  $V_{FE}$ . In addition, the  $V_{int}$  will also decrease, as shown in Fig. 5, which will definitely reduce the channel current intensity. Figures 4b, c, and d show the DIBL characteristics of the NC-JLFET with different  $T_{FE}$  values, and it



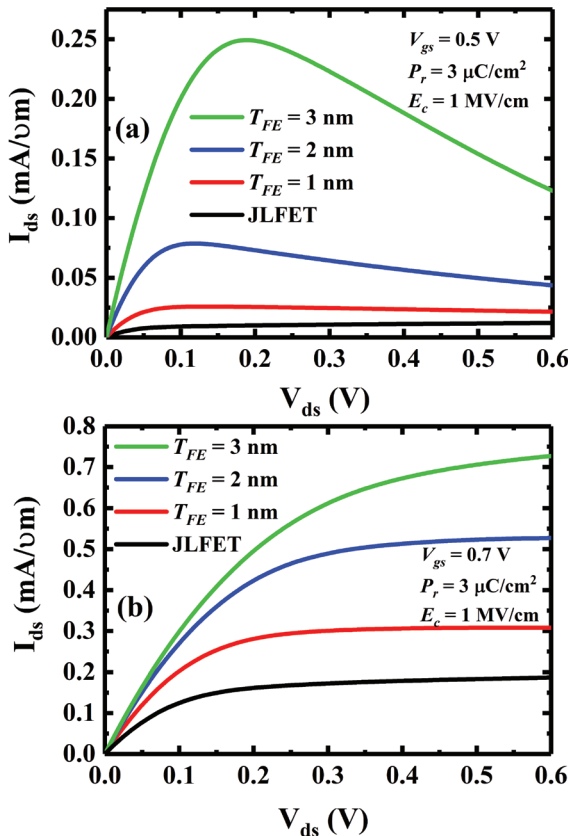
**Figure 6:** Potential profile at high and low drain voltages ( $V_{ds}$ ). Applied voltage of  $V_{gs} = 0.3 \text{ V}$ . (a) JLFET and (b) NC-JLFET at  $T_{FE} = 3 \text{ nm}$ .



can be clearly seen that negative DIBL characteristics appear when  $T_{FE} = 2\text{ nm}$  and  $3\text{ nm}$ .

At the same time, negative DIBL can also be proved by comparing the potential distribution in the channel region of JLFETs and NC-JLFETs as shown in Fig. 6. For a traditional JLFET, the potential barrier height will decrease with increasing  $V_{ds}$ . For an NC-JLFET, the opposite trend is shown in Fig. 6b. That is, with increasing  $V_{ds}$ , the height of the barrier near the source will increase causing the negative DIBL phenomenon.

Figure 7 shows the  $I_{ds}$ - $V_{ds}$  output characteristic of NC-JLFET for different  $T_{FE}$  values at  $V_{gs} = 0.5\text{--}0.7\text{ V}$ . As mentioned earlier, when  $V_{ds}$  increases,  $V_{int}$  decreases, which reduces the drain current. This exhibits a negative differential-resistance (NDR) characteristic as depicted in Fig. 7a. When  $V_{gs} = 0.5\text{ V}$ ,  $I_{ds}$  and  $V_{ds}$  have a positive correlation in the linear region. As  $V_{ds}$  continues to increase,  $I_{ds}$  decreases. This NDR effect can also be seen

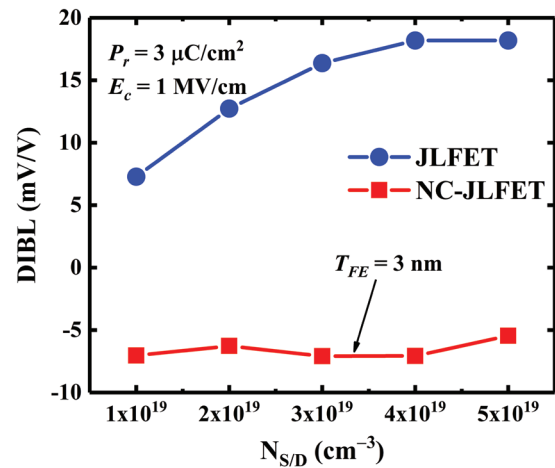


**Figure. 7:** Output characteristics of NC-JLFET for different values of  $T_{FE}$  at (a)  $V_{gs} = 0.5\text{ V}$  showing NDR and (b)  $V_{gs} = 0.7\text{ V}$  showing saturation in the ON current.

in the relationship between  $V_{int}$  and  $V_{ds}$  shown in Fig. 5. However, when  $V_{gs} = 0.7\text{ V}$ , only a positive correlation exists between  $V_{int}$  and  $V_{ds}$ , so the NDR effect will not appear [see Fig. 7b]. In addition, as the negative DIBL is

related to  $C_{FE}$ , the NDR can be controlled by changing  $T_{FE}$ . Despite the NDR, an NC-JLFET still provides a larger current than a traditional JLFET. It is worth mentioning that the simulation results of negative DIBL and NDR in our research are consistent with the results of [18].

Figure 8 shows the DIBL values of a JLFET and NC-JLFET for different  $N_{S/D}$ . It can be clearly seen that as  $N_{S/D}$  increases the DIBL effect becomes more serious for the JLFET. This can also be seen in the potential profile diagram. It can be observed from Fig. 9a that the barrier height is significantly reduced when  $N_{S/D} = 5 \times 10^{19}\text{ cm}^{-3}$ , resulting in a more serious DIBL effect. However, for the NC-JLFET, increasing  $N_{S/D}$  has little impact on its DIBL, which can also be observed in the potential profile diagram. Figure 9b also shows that  $N_{S/D}$  increased from  $1 \times 10^{19}$  to  $5 \times 10^{19}\text{ cm}^{-3}$  and the barrier height shows a downward trend. Due to the negative capacitance effect, the negative DIBL phenomenon still occurs.



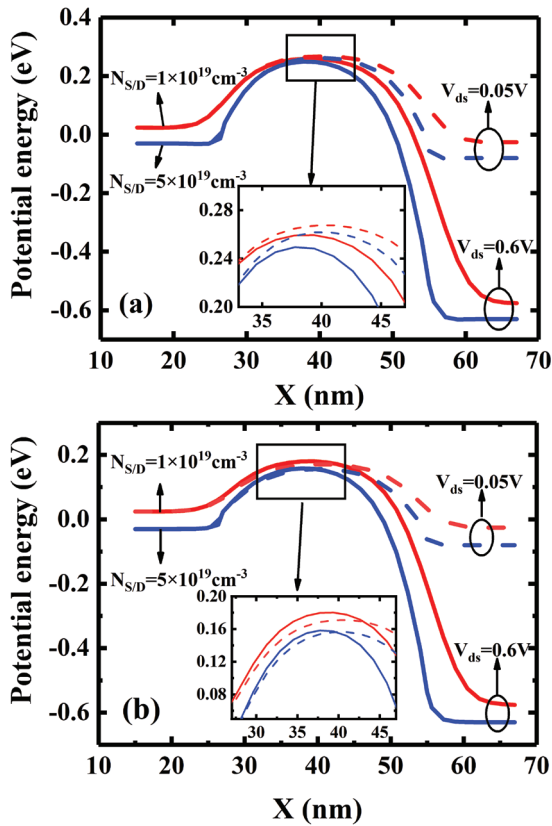
**Figure. 8:** DIBL of JLFET and NC-JLFET varying with source and drain doping concentration ( $N_{S/D}$ ).

Figure 10 exhibits the effect of ferroelectric thickness ( $T_{FE}$ ) on SS for different ferroelectric material parameters ( $E_c$  and  $P_r$ ). It can be clearly seen that SS decreases with increasing  $T_{FE}$ . This is mainly because as  $T_{FE}$  increases,  $C_{FE}$  will decrease, which will make  $C_{MOS}$  more closely match  $C_{FE}$ :

$$C_{FE} = \frac{dQ}{dV_{FE}} \approx \frac{1}{2aT_{FE}} = \frac{2}{3\sqrt{3}} \frac{P_r}{E_c T_{FE}} \quad (6)$$

$$A_G = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \quad (7)$$

$$SS = 60 \times \left(1 + \frac{C_{dm}}{C_{ox}}\right) \times \frac{1}{A_G} \quad (8)$$

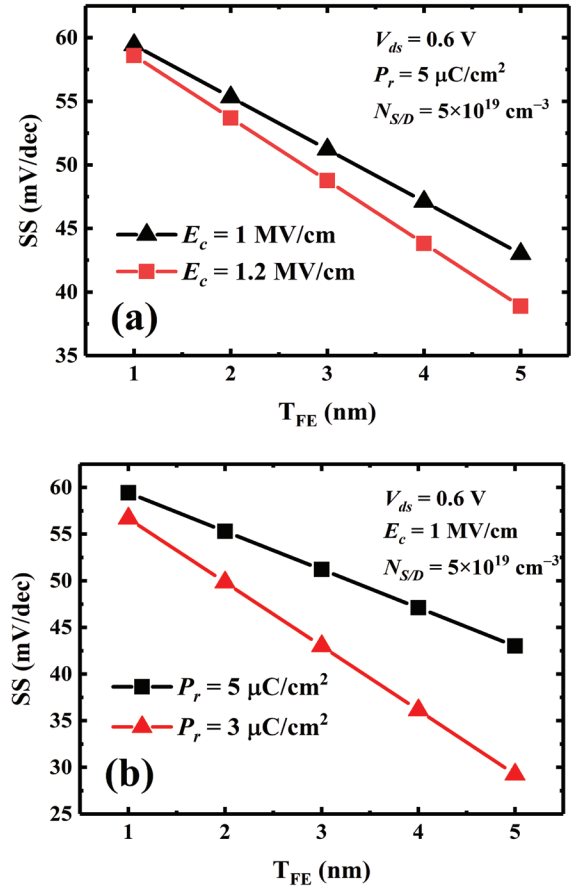


**Figure. 9:** Potential profile for different  $N_{s/D}$ . Applied voltage of  $V_{gs} = 0.3V$ . (a) JLFET and (b) NC-JLFET at  $T_{FE} = 3$  nm.

According to Eq. 7 [23], the voltage amplification factor ( $A_c$ ) increases due to the improved matching between the  $C_{MOS}$  and  $C_{FE}$  ( $|C_{FE}| - C_{MOS} > 0$ ). The relationship between  $A_c$  and  $SS$  is obtained by Eq. 8 [24],  $A_c$  and  $SS$  have a negative correlation, so  $SS$  decreases with increasing  $T_{FE}$ . The relationship between the ferroelectric capacitance ( $C_{FE}$ ) and the ferroelectric material parameters ( $E_c$  and  $P_r$ ) is shown in Eq. 6 [11]. When  $P_r$  ( $E_c$ ) and  $T_{FE}$  remain unchanged,  $C_{FE}$  decreases as  $E_c$  increases ( $P_r$  decreases), and results in lower  $SS$ . The results obtained in the simulation also conform to this rule, as shown in Fig. 10a and b.

#### 4 Conclusions

The electrical performance of a negative-capacitance double-gate junctionless transistor with additional source-drain doping determined by simulation analyses is presented in this paper. It was observed that the negative-capacitance effect and additional source-drain doping can increase the gate voltage and depletion capacitance, respectively, which makes the proposed NC-JLFET have higher  $I_{ON}/I_{OFF}$  and lower  $SS$  values. Then, the NDR and negative DIBL phenomenon are explained through the relationship between inter-



**Figure. 10:**  $SS$  for NC-JLFET with different (a)  $E_c$  and (b)  $P_r$  values for different ferroelectric thicknesses ( $T_{FE}$ ).

nal voltage and gate voltage. In addition, the influence of ferroelectric parameters on the NC-JLFET with additional source-drain doping is explored and shown to have better performance when the proper coercive field, remnant polarization, and ferroelectric thickness are chosen. The additional source-drain doped NC-JLFET studied can achieve superior performance and meet the requirements of low-power IC applications in the future.

#### 5 Acknowledgments

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#### 6 Conflict of Interest

The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in

the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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