

A Concurrent Dual-Band Inverter-Based Low Noise Amplifier (LNA) for WLAN Applications

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Abstract: In this paper, a two-stage concurrent dual-band low noise amplifier (DB-LNA) operating at 2.4/5.2-GHz is presented for Wireless Local Area Network (WLAN) applications. The current-reused structure using resistive shunt-shunt feedback is employed to reduce power dissipation and achieve a wide frequency band from low frequency to 5.5-GHz in the inverter-based LNA. The second inverter-based stage is employed to increase the gain and obtain a flat gain over the frequency band. An LC network is also inserted at the proposed circuit output to shape the dual-band frequency response. The proposed concurrent DB-LNA is designed for RF-TSMC 0.18- μm CMOS technology, which consumes 10.8 mW from a power supply of 1.5 V. The simulation results show that the proposed DB-LNA achieves a direct power gain (S_{21}) of 13.7/14.1 dB, a noise figure (NF) of 4.2/4.6 dB, and an input return loss (S_{11}) of -12.9/-14.6 dBm at the 2.4/5.2-GHz bands.

Keywords: low noise amplifier (LNA); concurrent; dual-band; inverter-based

Sočasni dvopasovni ojačevalnik z nizkim šumom (LNA) za aplikacije WLAN

Izvleček: V prispevku je predstavljen dvostopenjski sočasni dvopasovni ojačevalnik z nizkim šumom (DB-LNA), ki deluje na frekveni 2,4 / 5,2 GHz za aplikacije brezžičnega lokalnega omrežja (WLAN). Trenutno uporabljena struktura, ki uporablja uporovno povratno povezavo, se uporablja za zmanjšanje porabe moči in doseganje širokega frekvenčnega pasu od nizkih frekvenc do 5,5 GHz v pretvorniškem LNA. Druga stopnja, ki temelji na pretvorniku, se uporablja za povečanje ojačenja in doseganje enotnega ojačenja v celotnem frekvenčnem pasu. LC omrežje je vstavljeno tudi v izhodno vezje za oblikovanje dvopasovnega frekvenčnega odziva. Predlagani sočasni DB-LNA je zasnovan za RF-TSMC 0,18 μm CMOS tehnologiji, s porabo 10,8 mW pri napajalni napetosti 1,5 V. Rezultati simulacije kažejo, da predlagani DB-LNA doseže neposredno ojačenje (S_{21}) 13,7 / 14,1 dB, vrednost šuma (NF) 4,2 / 4,6 dB in vhodno povratno izgubo (S_{11}) -12,9 / -14,6 dBm v pasovih 2,4 / 5,2 GHz.

Ključne besede: ojačevalnik z nizkim šumom (LNA); sočasnost; dvopasovnost; pretvornik

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1 Introduction

Over the past few years, various and new wireless communication standards have been developed to extend transceiver functionalities. The development of the IEEE 802.11a/b (2.4/5.2-GHz) standard has been widely used in Wireless Local Area Network (WLAN) applications due to support for high data rate communication (up to 54 Mb/s) and the wide range of its applications [1-3]. Therefore, the new trend in RF front-end receiver features a low noise amplifier (LNA) capable of receiv-

ing multiband frequencies with a proper performance at each frequency band, as shown in Figure 1 [4].

The low noise amplifier (LNA) with dual bandwidth plays a critical role in the overall performance of the dual-band receiver. The design of the dual-band LNA (DB-LNA) includes some challenges such as high gain, low noise performance, low power dissipation, and proper input matching for both bands. Several approaches have been presented to implement the DB-LNAs with

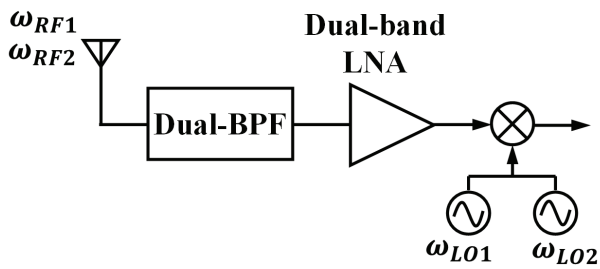


Figure 1: A concurrent dual-band receiver.

high performance operating at two different frequencies. The two single-band parallel LNAs configuration is one of the initial designs presented for DB-LNAs [5-8]. The measurement results show good performance at each frequency band at the expense of a larger chip area and higher power dissipation. The conventional methods use the switched inductors or switched capacitors in the input/output networks [9-14]. The structures consume low power, but generally degrade the gain and noise figure (NF) because of the insertion loss of their switches. Furthermore, LNA in such an approach can only operate with one band at a time. Another approach is to use a wideband LNA. Although this is a simple method for receiving multiple frequency bands simultaneously, the receiver sensitivity can be degraded due to the presence of unwanted signals in the wide frequency band. The most effective technique to achieve DB-LNA is to insert the notch filters in a wideband LNA [15-20]. Compared to the switchable LNAs, in this approach, the LNA supports simultaneous dual-band operations and consumes lower power. Hong et al. [17] used the cascode topology with gain boosting technique to achieve high gain and proper input matching. In addition, it employs the passive elements as bandpass/bandstop filters in the output network circuit to shape the frequency response, and to obtain a concurrent DB-LNA operating at 2.4/5.2GHz. Although this method results in a good performance in terms of linearity and power dissipation, it suffers from the unbalanced amplitude of the gain at the operating frequencies and weak roll-off in gain at the high band. Yu and Neihart [21] proposed a transformer-based multimode LNA using a reconfigurable multi-tap transformer as the gate inductor. The proposed LNA can dynamically achieve a single-band, or concurrent dual-band frequency response. However, it cannot provide high attenuation in the stopband and proper roll-off in gain at both bands in concurrent dual-band mode. In this paper, a two-stage concurrent DB-LNA in 0.18- μm CMOS technology is designed that operates at 2.4/5.2-GHz. The desired frequency bands are realized by using the LC network at the LNA output. The stagger tuning technique is also used to enhance the gain and provide a flat gain over the frequency band. Therefore, a concurrent DB-LNA with high balanced gain, proper

roll-off in gain, and good input matching is obtained. The paper is organized as follows: Section 2 presents the design parameters of the proposed circuit, including the voltage gain, input impedance matching, noise figure, and band selection. In Section 3, the simulation results are presented and discussed. Finally, the conclusion is given in Section 4.

2 Design of proposed circuit

The schematic of the proposed DB-LNA is shown in Figure 2. It consists of two inverter-based stages using resistive shunt-shunt feedback along with an LC network connected at the circuit output.

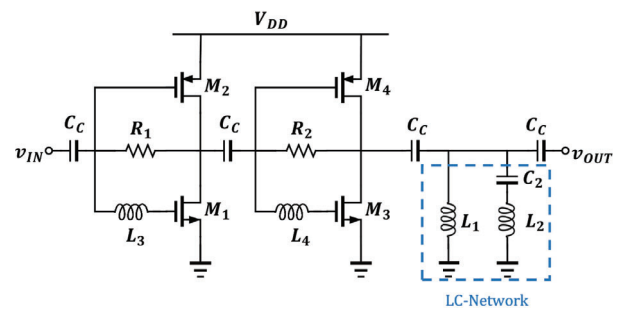


Figure 2: Schematic of the proposed DB-LNA.

In each stage, the current-reused technique is utilized to achieve low power dissipation and improve gain performance. Since the DC currents of transistors M_2 and M_4 are reused by M_1 and M_3 , respectively, there is no requirement for additional driving currents for M_1 and M_3 . The resistive feedbacks are utilized to achieve simultaneous proper input matching and flat gain. They also provide a self-biased structure for the proposed DB-LNA. The series peaking inductors of L_3 and L_4 are inserted in the gate of M_1 and M_3 to extend the bandwidth and provide proper input matching. The LC network of L_1 , L_2 , and C_2 is implemented at the LNA output to realize the dual-band frequency response within the LNA frequency response. The proposed circuit can provide high gain and good input matching at the two passbands with high attenuation in the stopband. The capacitance of CC is employed to provide the DC bias isolation of the circuit.

2.1 Bandwidth and gain analysis

A wideband amplifier operating over low frequency to 5.2-GHz is first designed to obtain the main structure of the proposed DB-LNA. Then, the frequency response of the DB-LNA is shaped by inserting an LC network. So far, several topologies are reported to achieve the wideband LNA, such as common-gate [22, 23] and

shunt resistive feedback [3, 24]. The common-gate (CG) configuration provides a wideband input impedance matching, high linearity, and good reverse isolation compared to the common-source (CS) configuration. Nevertheless, the CG configuration suffers from high NF, that is typically more than 3dB. Additionally, the feedback structure consumes more power. Using a modified inverter-based structure with shunt resistive feedback is an appropriate idea to improve the gain performance without additional power dissipation. Figure 3 shows a single modified inverter-based stage, which exhibits a relatively high flat gain over low frequency to 5.2-GHz.

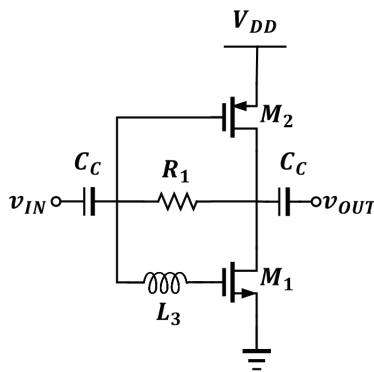


Figure 3: Schematic of the modified inverter-based LNA.

Higher gain is achieved by a second inverter-based LNA, which is connected in series with the first stage. However, the impedance mismatch between stages can result in ripples in the passbands, but using the stagger tuning technique results in flat gain over low frequency to 5.2-GHz. Figure 4 shows the proposed two-stage wideband LNA.

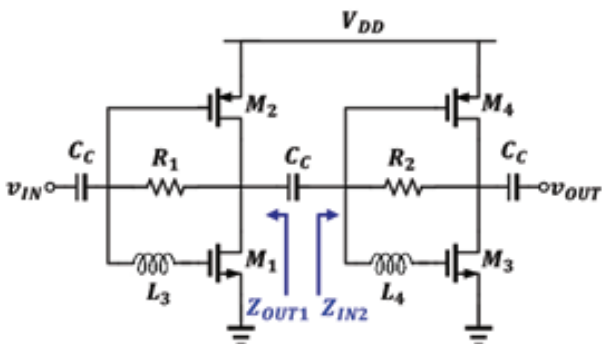


Figure 4: Schematic of the proposed wideband LNA.

The small-signal equivalent circuit of the proposed wideband LNA is shown in Figure 5. As can be seen, the feedback resistors of R_1 and R_2 are placed in parallel with the gate to drain capacitances (C_{gd}) to provide the wideband input matching. At the frequencies of interest, the impedances of the gate to drain capacitances

are almost always much higher than the feedback resistor impedances that they are in parallel with. Therefore, C_{gd} is neglected in the small-signal equivalent circuit of the proposed wideband LNA. In Figure 5, $Z_{L1} = r_{o1} || r_{o2}$ and $Z_{L2} = r_{o3} || r_{o4}$, where r_{oi} is the drain output resistance of M_i . It is assumed that $R_2 \gg Z_{L2}$ for alleviating the loading effect of the second stage. By neglecting the gate-to-drain capacitance (C_{gd}), the input impedance of the second stage (Z_{IN2}) in case of $\omega \ll \omega_T$ is obtained as follows:

$$Z_{IN2}(s) = \frac{L_4 C_{gs3} s^2 + 1}{(C_{gs3} + C_{gs4})s} \quad (1)$$

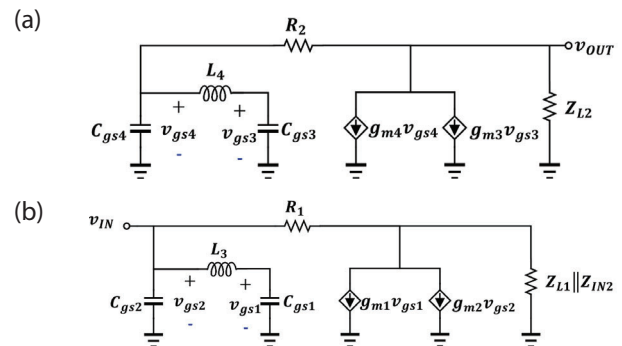


Figure 5: The small-signal equivalent circuit of the LNA (a) second stage and (b) first stage of the wideband LNA.

The overall voltage gain of the proposed wideband LNA is given by:

$$A_{v,T} = A_{v1} \times A_{v2} \quad (2)$$

where, A_{v1} and A_{v2} are the voltage gain of the first and the second stages, respectively. Based on the small-signal analysis, A_{v1} can be expressed as below:

$$A_{v1}(s) = -\frac{L_3 C_{gs1} g_{m2} s^2 + g_{mT1}}{L_3 C_{gs1} s^2 + 1} (R_1 Z_{L1} Z_{IN2}) \quad (3)$$

where gm represents the transconductance of the MOS transistor, and $g_{mT1} = g_{m1} + g_{m2}$ is the overall transconductance of the first stage. Similarly, A_{v2} is obtained as follows:

$$A_{v2}(s) = -\frac{L_4 C_{gs3} g_{m4} s^2 + g_{mT2}}{L_4 C_{gs3} s^2 + 1} (R_2 Z_{L2}) \quad (4)$$

where $g_{mT2} = g_{m3} + g_{m4}$ is the overall transconductance of the second stage. By assuming a small value for R_1 and high value for R_2 and regarding (2), $A_{v,T}$ is given as follows:

$$A_{v,T}(s) \cong g_{mT1} g_{mT2} R_1 Z_{L2} \frac{\left(L_3 C_{gs1} \frac{g_{m2}}{g_{mT1}} s^2 + 1 \right)}{\left(L_3 C_{gs1} s^2 + 1 \right)} \times \frac{\left(L_4 C_{gs3} \frac{g_{m4}}{g_{mT2}} s^2 + 1 \right)}{\left(L_4 C_{gs3} s^2 + R_1 (C_{gs3} + C_{gs4}) s + 1 \right)} \quad (5)$$

By assuming $R_1/L_4 > 5.2$ GHz, $A_{v,T}$ can be simplified as:

$$A_{v,T}(s) \cong g_{mT1} g_{mT2} R_1 Z_{L2} \frac{\left(1 + \frac{s^2}{\omega_{z1}^2} \right) \left(1 + \frac{s^2}{\omega_{z2}^2} \right)}{\left(1 + \frac{s^2}{\omega_{p1}^2} \right) \left(1 + \frac{s^2}{\omega_{p2}^2} \right)} \quad (6)$$

From (5) it can be seen that $A_{v,T}$ has four resonant frequencies $\omega_{p1,2}$ and $\omega_{z1,2}$, that expressed by:

$$\omega_{p1} = \frac{1}{\sqrt{L_3 C_{gs1}}} \quad (7)$$

$$\omega_{p2} = \frac{1}{\sqrt{L_4 C_{gs3}}} \quad (8)$$

$$\omega_{z1} = \frac{1}{\sqrt{L_3 C_{gs1} \frac{g_{m2}}{g_{mT1}}}} \quad (9)$$

$$\omega_{z2} = \frac{1}{\sqrt{L_4 C_{gs3} \frac{g_{m4}}{g_{mT2}}}} \quad (10)$$

From equation (6), it can be seen that the overall voltage gain is proportional to g_{mT1} and R_1 (Z_{L2} can be affected by load resistance). Since the input matching, power dissipation, and bandwidth limit the values of g_{mT1} and R_1 , the gain of the proposed wideband LNA can be adjusted by g_{mT2} . Moreover, the high band of the DB-LNA can be shaped by tuning ω_{p1} around 5.2-GHz. Figure 6 shows the overall frequency response of the proposed wideband LNA along with the frequency responses of the first and second stage. As can be seen, the proper roll-off in the upper-frequency response is achieved by setting ω_{z1} close to ω_{p1} .

2.2 Input impedance

Impedance matching over a wide band is one of the most challenging tasks in wideband LNA design. The input matching condition of the inverter-based LNA can be improved by applying the shunt-shunt resistive

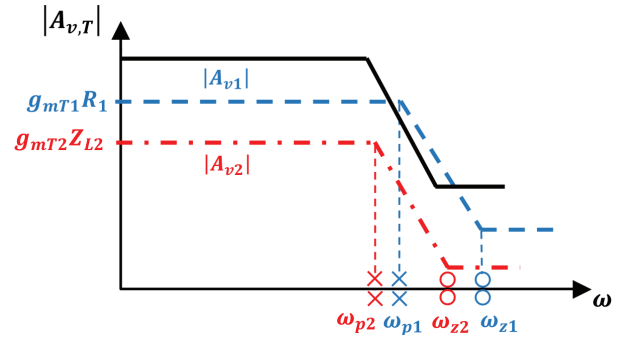


Figure 6: The frequency response ($|A_{v,T}|$) of the proposed wideband LNA.

feedback and inserting an inductor in series with the gate of the NMOS transistor. According to equation (1) and assuming $R_1/L_4 > 5.2$ -GHz, the input impedance of the proposed wideband LNA in case of $\omega \ll \omega_T$ is expressed by:

$$Z_{IN}(s) = \frac{(1 + R_1 (C_{gs3} + C_{gs4}) s) (1 + L_3 C_{gs1} s^2)}{g_{mT1} (1 + L_4 C_{gs3} s^2)} \quad (11)$$

As mentioned earlier, by assuming ω_{p1} around 5.2-GHz, $Z_{IN}(s)$ can be simplified as follows:

$$Z_{IN}(\omega) \approx \frac{1 + j\omega R_1 (C_{gs3} + C_{gs4})}{g_{mT1} (1 - L_4 C_{gs3} \omega^2)} \quad (12)$$

As can be seen, the input impedance is proportional to g_{mT1} , R_1 , and L_4 , thereby the trade-off between the gain and input matching can be reduced by only employing g_{mT1} for satisfying the input matching condition.

2.3 Noise figure

The noise performance of the wideband LNA is evaluated by assuming the thermal noise of the transistors and the resistors as the dominant noise sources, and the flicker noise is neglected. The loss of inductors is

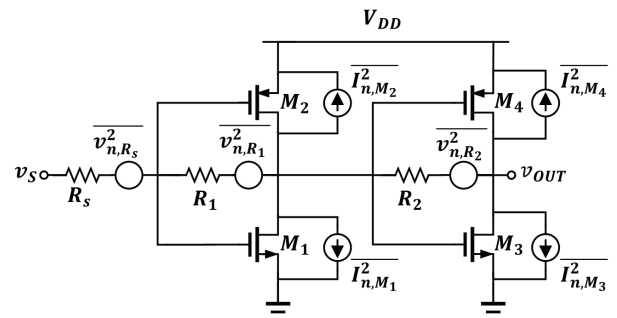


Figure 7: The simplified circuit of the wideband LNA for noise analysis.

neglected, and it is also assumed L_3 and L_4 resonate with the total capacitance at the input node of the first and the second stage, respectively. According to the mentioned conditions, the simplified circuit for noise calculation is derived, as shown in Figure 7.

The noise figure (NF) of the wideband LNA is given by:

$$NF = \frac{1}{A_{vs}^2} \frac{\overline{v_{n,out}^2}}{4KTR_s} \quad (13)$$

where A_{vs} is the voltage gain from v_s to v_{OUT} , and regarding $R_{IN} \approx R_1/2$, it can be expressed by:

$$A_{v1s}(s) = \frac{R_1}{R_1 + 2R_s} (g_{mT1}R_{o1}g_{mT2}R_{o2}) \quad (14)$$

where R_{o1} and R_{o2} represent the output resistance seen at the output nodes of the first and the second stage, respectively and they are given as:

$$R_{o1} \cong Z_{L1} \frac{R_s + R_1}{g_{mT1}R_s} \quad (15)$$

$$R_{o2} \cong Z_{L2} \frac{g_{mT1}R_2R_s + R_1}{g_{mT1}R_s + g_{mT2}(R_1 + R_2)} \quad (16)$$

According to Figure 7, the total output noise is expressed as:

$$\begin{aligned} \overline{v_{n,out}^2} = & 4KTR_2 + 4KT \frac{\gamma}{\alpha} g_{mT2}R_{o2}^2 + \\ & + \left(4KTR_1 + 4KT \frac{\gamma}{\alpha} g_{mT1}R_{o1}^2 \right) (g_{mT2}R_{o2})^2 + \\ & + 4KTR_s A_{vs}^2 \end{aligned} \quad (17)$$

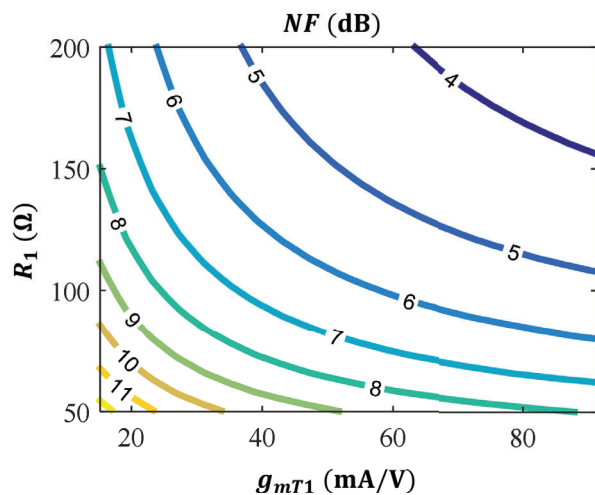


Figure 8: The contours of NF for $I_{D3}=2$ mA, $R_2=5$ k Ω , and $V_{eff1}=V_{eff3}=0.2$ V.

where α represents the ratio of g_m to the zero-bias drain conductance gd_0 , and γ is the MOS transistor thermal noise coefficient. Figure 8 shows the contours of $NF(g_{mT1}, R_1)$ in the case of $I_{D3}=2$ mA, $R_2=5$ k Ω and $V_{eff1}=V_{eff3}=0.2$ V. As shown in Figure 8, there is a trade-off between R_1 and g_{mT1} at a specific NF, and the proper NF can be achieved by choosing higher values for R_1 and g_{mT1} . Additionally, R_1 and g_{mT1} are limited by input matching, and thereby, a lower NF can be achieved regarding proper input matching and power dissipation.

2.4 LC network

As mentioned earlier, the circuit design starts with the design of a wideband LNA that exhibits a high flat gain over the low frequency to $f_2=5.2$ -GHz. It should be noted f_2 is defined by f_{p1} . It is assumed that the receiver receives two frequency bands concurrently without using switches. Therefore, concurrent DB-LNA is a development based on a multiband theory to achieve dual-band characteristics. For this purpose, an LC network is inserted in the LNA output to achieve the requirements with minimum effect on the gain, NF, and input matching. The proposed LC network determines the low band of the concurrent DB-LNA and enhances the spurious frequency rejection at the low frequency. Figure 9 shows the proposed LC network. As can be seen the low band of $f_1=2.4$ -GHz and the notch frequency of $f_3=3.5$ -GHz are realized by L_1 , L_2 , and C_2 as follows:

$$f_1 = \frac{1}{2\pi\sqrt{(L_1 + L_2)C_2}} \quad (18)$$

$$f_3 = \frac{1}{2\pi\sqrt{L_2C_2}} \quad (19)$$

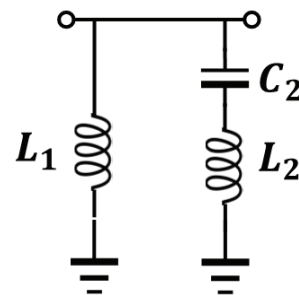


Figure 9: The proposed LC network used at the DB-LNA output.

Additionally, the frequency calibration method can be realized by using a varactor to tune the frequency shift due to the process variation. Figure 10 shows the frequency response of the proposed DB-LNA determined by the LC network.

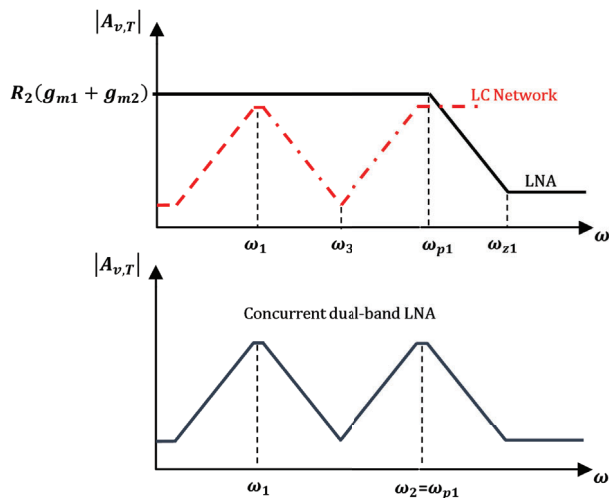


Figure 10: The frequency response ($|A_{v,T}|$) of the concurrent DB-LNA.

As shown, the proposed concurrent DB-LNA exhibits the operating frequencies of $f_1=2.4$ -GHz and $f_2=5.2$ -GHz.

3 Simulation results

The proposed concurrent DB-LNA is designed and simulated using Cadence Spectre-RF with 0.18 μm CMOS technology. The post-layout simulation results are reported in the paper, which take into account layout parasitic capacitances. The power supply of 1.5 V is used, and the minimum channel length is considered for all transistors. The first stage is designed to achieve moderate gain, low NF, and proper input matching over the lower frequencies to 5.2-GHz. Transistors M_1 and M_2 have the same width of 165 μm , while M_1 is biased at gate-source voltage (v_{gs1}) of 0.64 V, thereby $g_{m1} = 60$ mA/V and $g_{m2} = 25$ mA/V. A higher g_{mT1} value reduces the

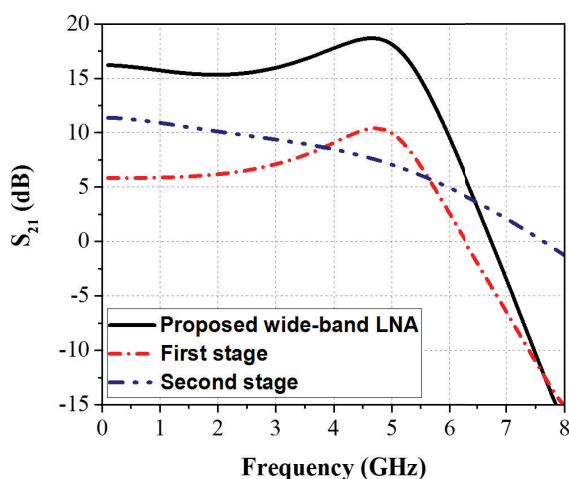


Figure 11: The simulated S_{21} of the proposed LNA.

NF, but increases the power dissipation and degrades the input matching. According to (7) and (9), the ω_{z1} is located at about $1.85\omega_{p1}$, thereby providing a proper roll-off at the upper-frequency band. The second stage enhances the gain and obtains a flat gain over a wide frequency band. For this purpose, the transistors M_3 and M_4 are designed to have $g_{m3}=90$ mA/V and $g_{m4}=10$ mA/V, while M_3 is biased at $v_{gs3}=0.54$ V with the total width of 310 μm , and M_4 has the width of 50 μm . The transistor dimensions chosen above and, according to (11) and (13), lead to $L_3=4.2$ nH, $L_4=2$ nH, $R_1=135$ Ω , and $R_2=1.5$ k Ω . Figure 11 shows the simulated power gains of the two separate stages and the proposed wideband LNA operating over the low frequencies to 5.2-GHz.

As shown in Figure 6, if the resonant frequencies of A_{v1} and A_{v2} are properly optimized, such as placing ω_{p2} at approximately 4-GHz and ω_{p1} at 5-GHz while keeping reasonable input-matching, a wideband flat power gain is expected. The dual-band gain response is achieved when the LC network is inserted at the output of the wideband LNA. Resonating at 3.8-GHz, L_2 and C_2 result in a very low output impedance. C_2 is chosen to be about 1.4 pF, while L_2 is adjusted about 1.5 nH. From (21), it can be seen that the low band operation of $f_1=2.4$ -GHz is achieved with $L_1=1.6$ nH. Table 1 lists the optimized component values of the concurrent DB-LNA and the bias current of transistors.

Table 1: Parameters and their values.

Component	Symbol	Value	Current (mA)
Transistor (Finger \times W(μm) \times L(μm))	M_1	(34 \times 4.8 \times 0.18)	5
	M_2	(50 \times 3.2 \times 0.18)	5
	M_3	(46 \times 6.8 \times 0.18)	2.2
	M_4	(25 \times 1.8 \times 0.18)	2.2
Inductance (nH)	L_1	1.6	
	L_2	1.5	
	L_3	4.2	
	L_4	2	
Capacitance (pF)	C_2	1.4	
	C_C	5	
Resistance(Ω)	R_1	135	
	R_2	1500	
Bias (V)	V_{DD}	1.5	

Figure 12 shows the layout of the proposed DB-LNA, occupying 0.55 mm \times 0.48 mm chip area, excluding the pads.

The post-layout simulated power gain (S_{21}) and input return loss (S_{11}) of the concurrent DB-LNA are shown in Figure 13 and Figure 14, respectively. As shown in Figure 13, the balanced amplitude of the gain at the oper-

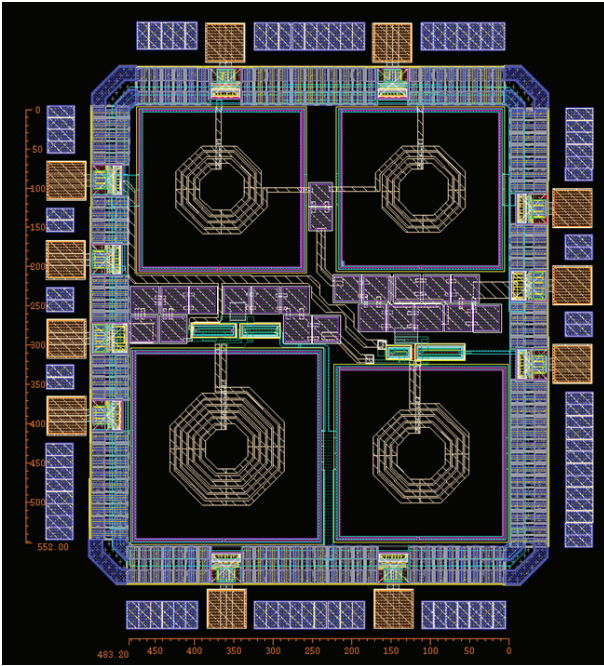


Figure 12: The layout of the proposed concurrent DB-LNA.

ating frequencies of 2.4-GHz and 5.2-GHz is achieved by choosing $L_1=1.6$ nH and $L_2=1.5$ nH. Figure 14 shows the value of g_{mT1} that determines the input matching range. As shown in Figure 14, the simultaneous dual-band input matching smaller than -10 dB is achieved by choosing the g_{mT1} smaller than 85 mA/V. However, the smaller values of g_{mT1} can potentially achieve a higher noise figure up to 2 dB and yield a substantially lower gain.

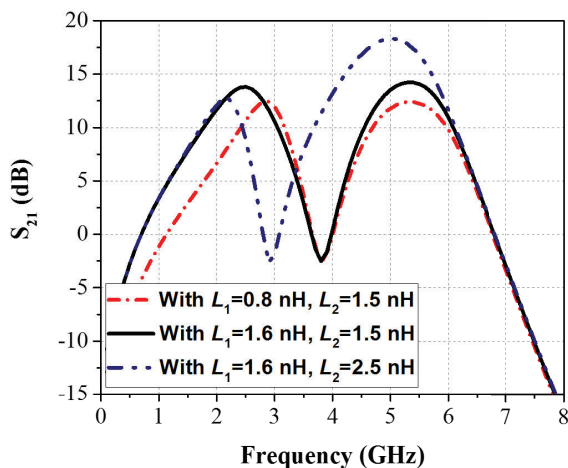


Figure 13: The simulated S_{21} of the concurrent DB-LNA.

Noise analysis for the concurrent DB-LNA is carried out for $R_1=135 \Omega$, as shown in Figure 15, in which the NF is 4.2 and 4.6 dB at the operating frequencies of 2.4-GHz and 5.2-GHz, respectively. The effect of R_1 on the noise performance of the proposed DB-LNA is also evaluated

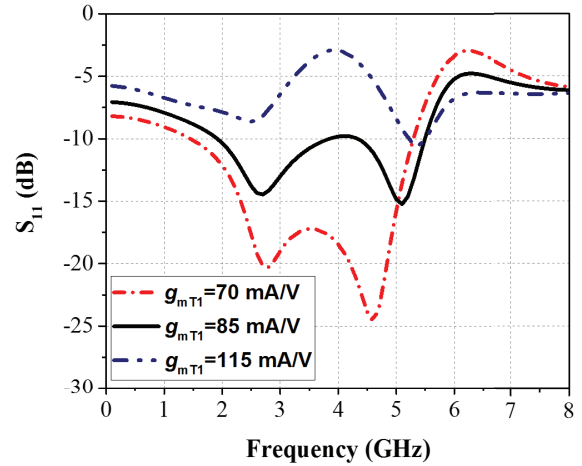


Figure 14: The simulated S_{11} of the concurrent DB-LNA

in Figure 15 by varying the value of R_1 . As shown in Figure 15, higher R_1 results in lower NF for both frequency bands. However, higher values of R_1 cause substantial peaking at the low band of the proposed DB-LNA.

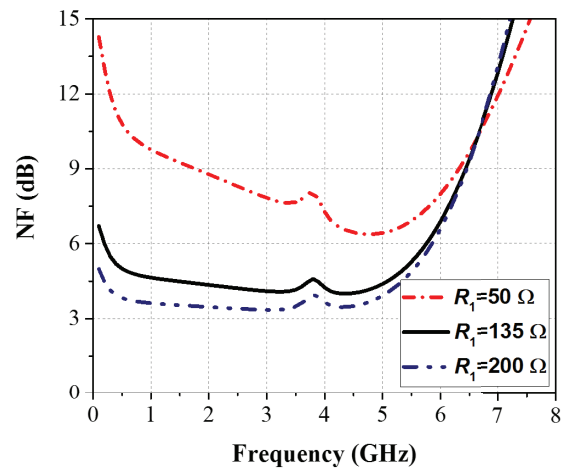


Figure 15: The simulated NF of the concurrent DB-LNA.

Figure 16 shows the third-order intermodulation intercept point (IIP3) simulations of the concurrent DB-LNA. The IIP3 is carried out by applying a two-tone test with 4-MHz frequency spacing. As shown in Figure 16, the post-simulated IIP3s are -6 dBm and -11 dBm at 2.4-GHz and 5.2-GHz, respectively.

Figure 17 shows the stability factors based on the S-parameters to consider the stability of the proposed DB-LNA. The necessary and sufficient conditions for unconditional stability are expressed as follows:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}||S_{21}|} > 1 \quad (20)$$

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (21)$$

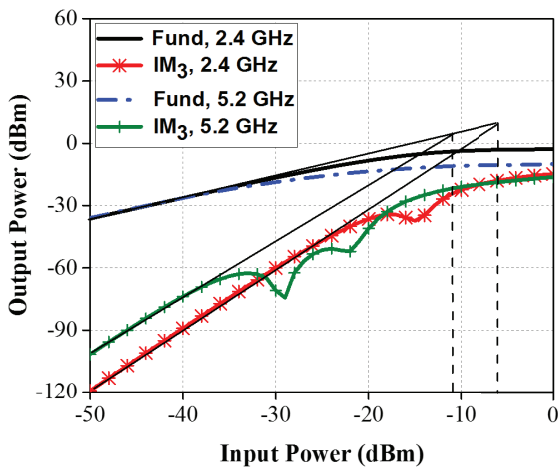


Figure 16: The simulated IIP3s with 4-MHz frequency spacing.

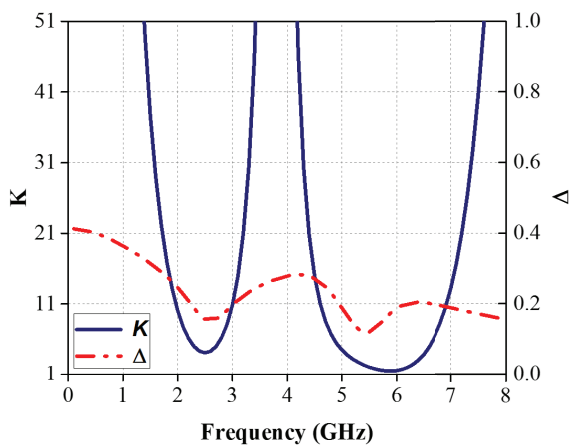


Figure 17: The simulated stability factors

As shown in Figure 17, the concurrent DB-LNA satisfies the conditions for unconditional stability at both frequency bands.

Monte Carlo analysis is carried out on the proposed DB-LNA to evaluate the effects of components mismatches on performance parameters such as S_{21} , NF, and S_{11} . In Monte Carlo simulation with 1000 iterations, a 2% mismatch with Gaussian distribution for all circuit components is considered. As shown in Figures 18 and 19, the mean S_{21} of 13.97/14.11 dB (nominally 13.73/14.11 dB) with a standard deviation of 0.21/0.45 are obtained at the operating frequencies of 2.4/5.2-GHz. The results show a mean NF of 4.18/4.72 dB (nominally 4.25/4.67 dB) with a standard deviation of 0.06/0.13 at the operating frequencies of 2.4/5.2-GHz. In addition, mean S_{11} of -12/-13.5 dB (nominally -12.95/-14.64 dB) with a standard deviation of 0.28/0.88 is obtained at the operating frequencies of 2.4/5.2-GHz.

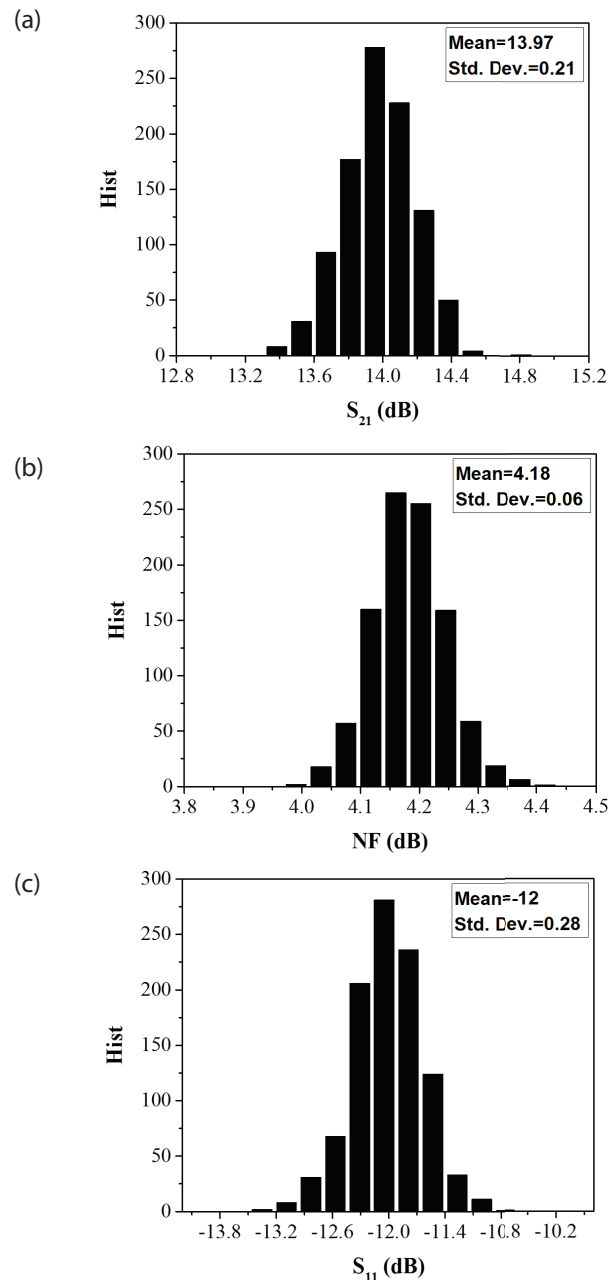


Figure 18: Monte Carlo simulation results at 2.4-GHz for (a) S_{21} (b) NF and (c) S_{11} .

As seen in Figures 18 and 19, the Monte Carlo simulation results confirm the low sensitivity of the proposed DB-LNA to process variations at both frequency bands. The process corner cases and temperature variation are simulated at the operating frequencies, and the results are listed in Table 2. The proposed DB-LNA is also simulated over the power supply variation, and the results are listed in Table 3.

Table 4 has compares the performance of the proposed DB-LNA with similar reported works. A figure of merit (FoM) in both bands, which allows comparison between the concurrent DB-LNAs, is defined as follows:

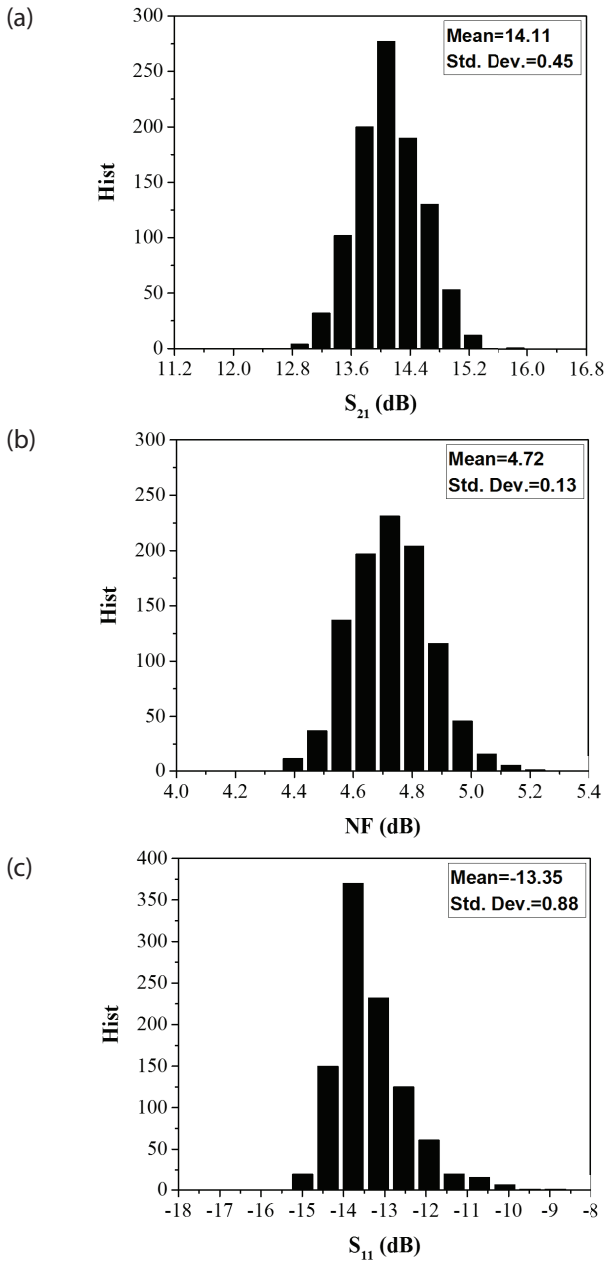


Figure 19: Monte Carlo simulation results at 5.2-GHz for (a) S_{21} (b) NF and (c) S_{11} .

$$FoM = 10 \log \left(\frac{10^{\frac{S_{21}(dB)}{20}} \times \sqrt{f_1 \times f_2}}{10^{\frac{NF(dB)}{10}} \times 10^{\frac{S_{11}(dB)}{20}} \times P(W) \times Size(mm^2)}} \right) \quad (22)$$

where f_1 and f_2 represent the centre frequencies of the low band and the high band of the concurrent DB-LNA, respectively. According to Table 4, the DB-LNA in (Roobert & Rani [25]) presents a high power gain and low NF at both bands. However, its operating frequencies are lower than those of the proposed DB-LNA. Moreover, (Neihart et al.,[26]) achieves a low power DB-LNA. However, it suffers from the unbalanced amplitude of the

gain at the operating frequencies. As seen in Table 4, the proposed circuit exhibits high and balanced amplitude of the gain and excellent input matching, moderate linearity, and power dissipation.

4 Conclusion

This paper proposed and analytically investigated an inverter-based concurrent dual-band LNA (DB-LNA) operating at 2.4/5.2-GHz. By inserting an LC network at the wideband LNA output, the dual-band operation is achieved. Analytical expressions for the gain, input matching, and noise figure are presented. In addition, the trade-off between the noise figure, and the input matching is detailed. The post-layout simulated circuit exhibits 13.7 dB/14.1 dB power gain and 4.2 dB/4.6 dB noise figure at 2.4 and 5.2 GHz, respectively. Moreover, it draws a current of 7.2-mA from 1.5 V supply. Compared to other DB-LNAs, the proposed LNA presents a high balanced gain, proper roll-off, and good input matching. The proposed concurrent DB-LNA could thus be a good choice for multiband receivers.

Table 2: The performance of the proposed DB-LNA for different process corners and temperature

Parameter	S_{21} (dB)	NF (dB)	S_{11} (dB)	P_c (mW)	IIP3 (dBm)
FF@-40 °C	19.3/22.9	2.9/3.4	-8.9/-17.1	16.6	-7/-8.5
TT@27 °C	13.7/14.1	4.2/4.6	-12.9/-14.6	10.8	-6/-11
SS@85 °C	7.9/6.4	5.9/6	-21.7/-12	7.4	-6.5/-8

Table 3: The performance of the proposed DB-LNA for power supply variation

VDD (V) ±10%	S_{21} (dB)	NF (dB)	S_{11} (dB)	P_c (mW)	IIP3 (dBm)
1.35	9.3/8.4	4.8/4.7	-17.8/-13.6	5.6	-10/-12.4
1.8	13.7/14.1	4.2/4.6	-12.9/-14.6	10.8	-6/-11
1.65	16.6/17.9	3.9/4.7	-11.2/-13.4	18.1	-2/-8.5

5 Conflict of interest

The authors have no affiliation with any organization with a direct or indirect financial interest in the subject matter discussed in the manuscript.

Table 4: The performance summary of the proposed concurrent DB-LNA and comparison with state-of-the-art concurrent DB-LNAs

Ref.	Tech. (nm)	f_0 (GHz)	S_{21} (dB)	NF (dB)	S_{11} (dB)	IIP3 (dBm)	V_{DD} (V)	Power (mW)	Size* (mm ²)	FoM
[20]	130	2.4	19.3	3.2	-16.8	-20.1	1.2	2.4	-	-
		5.2	17.5	3.3	-19.4	-18.1				-
[21]	130	2.05	14.9	4	-8.6	-2	1.2	12	0.44	5.8
		5.65	14.9	4.8	-32.4	-4.2				16.9
[25]	180	0.9	15	1.9	-10	-6	1.2	12	0.58	3.8
		2.4	16	2	-15	-2				6.7
[26]	180	2.4	14.2	4.4	-14	3.4	1.8	7.2	0.61	8.7
		5.2	14.6	3.7	-13.5	-2.7				9.4
[27]	180	2.4	10.8	3.25	-15	4.5	1.8	11.7	0.85	5
		5	8	4.1	-11	3				0.9
[28]	90	0.9	22	2	-21	-5.5	0.5	5.2	0.091	24.3
		2.3	24	2.7	-15	-6.65				21.6
[29]	SISL Avago ATF36163	2.45	28.4	0.7	-13	-6.6	1	36	-	-
		5.25	28.8	1.1	-20	-5.1				-
[30]	130	2.45	9.4	2.8	-12.6	-4.3	1.2	2.79	0.36	14
		6	18.9	3.8	-21	-5.6				21.9
[31]	180	1.217	13	1.58	-10.6	-	1.8	11.6	0.14	9.5
		1.568	11.5	3.1	-10.7	-				7.3
[32]	180	2.4	20	6.6	-7	-	1.8	15	0.225	7.1
		5.25	8	6.6	-12	-				3.6
[33]	150 PHEMT	2.4	20	2.2	-19	-8.5	3	37.8	1.15	6.3
		5	15	2	-13	-4				1
This work	180	2.4	13.7	4.2	-12.9	-6	1.5	10.8	0.265	10
		5.2	14.1	4.6	-14.6	-11				10.6

*Excluding Pads

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Arrived: 14. 08. 2020

Accepted: 28. 12. 2020