

Design of a Low Power and High-Efficiency Charge Pump Circuit for RFID Transponder EEPROM

Labonnah Farzana Rahman¹, Lubna Alam¹, Mohammad Marufuzzaman²

¹*Universiti Kebangsaan Malaysia, Institute for Environment and Development, Bangi, Malaysia*

²*Universiti Tenaga Nasional, Institute of Energy and Infrastructure, Kajang, Selangor, Malaysia*

Abstract: The charge pump (CP) circuit is an essential part of a radio frequency identification electrically-erasable-programmable-read-only memory (RFID-EEPROM). A CP circuit generates a boosted output voltage that is greater than the power supply voltage. However, the performance of the diode configured CP circuits is strongly affected by the extra power dissipation and the parasitic capacitance. The parasitic capacitors of the CP circuit are also responsible for increased power consumption. In this research, an improved CP circuit is designed for achieving higher output voltage gain by reducing the parasitic capacitances. Moreover, the proposed circuit consumes less power, which makes it more suitable for low power applications like RFID transponder. The proposed CP circuit is using the internal boosted voltage for backward control where active controls are applied to the charge transfer switch (CTS) to eradicate the reverse charge sharing trends. Simulated results showed that by using 1 pF pumping capacitor to drive the capacitive output load, the proposed circuit generates 9.56 V under 1.2 V power supply. In comparison with other research works, this CP circuit consumes less power (only 15.26 μ W), which is lower than previous research works. Moreover, the proposed CTS CP circuit can operate with the efficiency of 79.3%, which is found higher compared to other research works. Thus, the proposed design will be an essential module for low power applications like RFID transponder EEPROM.

Keywords: charge pump; charge transfer switch; non-volatile memory; transponder; RFID

Zasnova vezja črpalke naboja z majhno močjo in visoko učinkovitostjo za RFID transponder EEPROM

Izveček: Vezje črpalke naboja (CP) je bistveni del radijsko frekvenčne identifikacije električno izbrisljivega programabilnega pomnilnika samo za branje (RFID-EEPROM). CP vezje generira višjo izhodno napetost od napajalne. Kljub temu na delovanje CP vezij močno vpliva dodatna disipacija moči in parazitska kapacitivnost. Parazitski kondenzatorji vezja CP so prav tako odgovorni za povečano porabo energije. V tej raziskavi je predstavljeno izboljšano vezje CP, ki je zasnovano za doseganje višjega ojačenja izhodne napetosti z zmanjšanjem parazitskih kapacitivnosti. Poleg tega se predlagano vezje porabi manj moči, zaradi česar je bolj primerno za aplikacije z nizko porabo, kot je RFID transponder. Predlagano vezje CP uporablja notranjo ojačano napetost za povraten nadzor, kjer je uporabljena aktivna kontrola stikala za prenos naboja (CTS) za izkoreninjenje trendov delitve povratnega naboja. Simulirani rezultati so pokazali, da predlagano vezje z uporabo črpalnega kondenzatorja 1 pF generira napetost 9,56 V pri vhodni napajalni napetosti 1,2 V. V primerjavi z drugimi raziskavami to CP vezje porabi le 15,26 μ W moči. Poleg tega ima predlagano vezje CTS CP učinkovitost 79,3%. Predlagana zasnova bo tako bistveni modul za aplikacije z nizko porabo energije, kot je npr. RFID transponder EEPROM.

Ključne besede: črpalka naboja; stikalo za prenos naboja; trajni spomin; transponder; RFID

* Corresponding Author's e-mail: labonnah.deep@gmail.com, lubna@ukm.edu.my

1 Introduction

A typical RFID transponder is known as data carrying devices in RFID systems. RFID transponder can be embedded in objects like electronic devices, luggage, pets, or human being for identification. The RFID transponder is a chip or small circuit board coupled to an antenna [1]. A typical RFID chip contains mainly three blocks, such as analogue, logic, and memory blocks. To store information in the readerless RFID transponder, a small amount of NVM should be embedded [2] Transponder memory can contain read-only memory (ROM), Random Access Memory (RAM), non-volatile memory as EEPROM, flash memory, etc. and data buffers subjected to the device functionality [3]-[4].

Different types of memories exist in the market. Among them embedded NVM such as EEPROM is mostly used as tag memory in RFID, SoC, and FPGA systems. However, the prerequisites, additional masks, and fabrication steps made EEPROM and Flash memory highly expensive compared to a standard CMOS logic process. Many researchers wanted to develop EEPROM in a traditional CMOS logic process as it has the advantages of low cost and low power [5]-[8].

However, the maintenance and endurance features are inadequate due to the NMOS tunnelling junction or the single-ended memory cell architecture with a too-thin oxide [5]-[6]. It has a large area/bit and consumes much power as each bit cell contains its high voltage switch [7]-[8]. To generate the high voltages, an internal high-voltage generator circuit such as voltage doublers or CP circuit is required [9].

Currently, low-voltage and small size DC-DC converters are widely required for mixed-mode circuit schemes. To transform an input voltage from low to high with either a positive or reverse polarity, the CP circuit can be the vital element to encounter the demands [10]. In the CP circuit, capacitors are needed to store the energy of any devices instead of magnetic constituents. The capacitors required by the CP circuit can be small enough to be fabricated in IC. For low-power designs, CP circuits are needed to generate dc voltages higher than the power supply (VDD) or lower than the ground voltage (GND) of the memory chip. With the features of high-energy efficiency, small space, low power dissipation, and low current drivability, the CP circuit is chosen by the researcher as the compulsory module in EEPROM. Commonly, it is applied to the EEPROM in RFID transponder, DC-DC converters, and power supervision chips to write or to erase the floating-gate devices [11-13].

Dickson established the most widespread CP circuit in 1976, where the CP circuit used the diode-connected

NMOS arrangement as a charge transfer device instead of switches [14] (Dickson, 1976). However, power efficiency and voltage gain in each stage are very low in the diode-connected CP circuit due to the body effect. Several types of research have been made to enhance the performance of the CP circuit [15-16]. Yan et al. have considered a CP with additional devices, which suffered from more power consumption for a lower current load [15]. Liu et al. proposed a CP with charge transfer switches (CTS) and parasitic capacitors to solve the problem of body effect. Besides, the CP circuit used the next pumping voltages to switch each CTSs [16]. However, the enlarged parasitic capacitance at every pumping stage decreases the pumping efficiency or the voltage gain. In 2009, Wang et al. also designed a CP circuit with the backward. They forwarded the CTS controlling method to recover the efficiency, to eradicate the body effect, and to escalate the voltage gain [17]. Nevertheless, the pumping efficiency or voltage gain is still lower with the PMOS switch in the output stage.

In this research, an improved CP circuit using CTS with reduced parasitic capacitance is described. The designed CP circuit is capable of reducing power consumption and increased voltage efficiency, which is compatible with the RFID transponder EEPROM. Silterra 0.13 μm CMOS process is utilized to design and verify the enhanced CP circuit. The comparative study proves that the proposed design decreased the parasitic capacitance, increased the pumping efficiency, and cut down the power consumption compared Liu et al. and Wang et al.'s CP circuit.

2 Materials and methods

In this research, CTS is the most widely used CP design method, which has been used by many researchers in their study. In this scheme, the dynamic charge transfer scheme in each step is the key to enhancing the boosted charge from the lower supply voltage. Most of the previous researchers included both the NMOS and PMOS transistors to implement the diode configuration in CMOS, where PMOS transistors created a large substrate current in each step of the charge transfer process, which eventually increased the power dissipation of the overall design. Therefore, in this research, a novel CTS-based CP circuit is proposed, where all the PMOS transistors are excluded, and NMOS transistors are utilized in all stages. This reduces the substrate current or in another term, the power dissipation of the overall circuit. The schematic diagram of the proposed CTS CP circuit is shown in Figure 1. In this research, Silterra 0.13 μm CMOS process is used to design the

schematic of the proposed CP circuit. From Figure 1, it is shown that one diode-configured MOSFET MD1 is utilized in this design to initiate the voltage from the supply voltage VDD to start the charge transfer process from one stage to another, whereas, another MOSFET MD2 is connected with the output stage of the circuit. On the other hand, transistors (MS1–MS9) are required to control the CTS and to transmit the boosted charges from the first stage to last using the backward charge transfer scheme. As all the CTS switches from MS1–MS9 does not entirely turn “OFF” during this transfer process, additional controlling transistors MN1 to MN9 and MP1 to MP9 are added in this design.

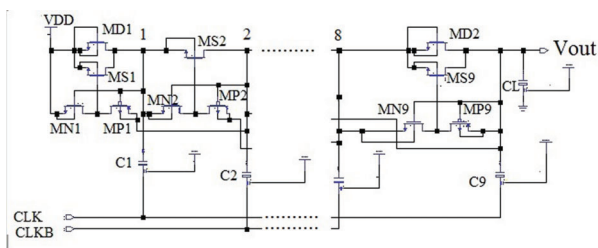


Figure 1: Schematic diagram of the proposed CTS based CP circuit.

In this research, when the clock signal CLK is in a high state, and the anti-phase clock signal CLKB is in a low condition, the gate of transistor MS2 is turned ON at the time of the charge pump process, which holds the amplitude of VDD as the pass transistor MN2 is switched OFF and MP2 is switched ON. Therefore, transistor MS2 has the value of VDD to node 2. On the other hand, when CLK is in a low state, and CLKB is in a high condition, the pass transistor MN2 is turned ON, and MP2 is turned OFF. Therefore, the gate voltage of MS2 becomes zero, which turns OFF the MS2 transistor entirely and the entire CP circuit feedbacks the charges from stage one to the next. In this design process, the total performance of the circuit closely depends on the sizing of the transistors. In this topology, zero V_{th} MOSFETs help to overcome the threshold voltage drop at each stage, which helps to boost the pumping process of this scheme. Usually, the amplitude of the V_{clk} is same as V_{DD} , in this scheme. Thus, the voltage variation and the voltage fluctuation of each pumping node can be expressed as,

$$\Delta V \approx V_{CLK} = V_{DD} \quad (1)$$

$$\Delta V = V_{CLK} \frac{C_{pump}}{C_{pump} + C_{par}} - \frac{I_o}{f \cdot (C_{pump} + C_{par})} \quad (2)$$

where V_{CLK} is the voltage amplitude of the clock signals, C_{pump} is the pumping capacitance, C_{par} is the parasitic capacitance of each pumping node, I_o is output current, and f is the clock frequency. If I_o is small enough,

and C_{pump} is large enough, I_o can be ignored from equation (2). Hence, the output voltage of the N-stage CP circuit can be expressed as

$$V_{out} = N \cdot (V_{DD} - V_D) \quad (3)$$

where V_D is the cut-in voltage of the pn-junction diode and N is the number of the stages taking part in pumping. The ripple voltage is defined as:

$$V_{ripple} = \frac{I_{out}}{f C_{out}} \quad (4)$$

where, C_{out} is the load capacitance, which is ignored to calculate the ripple voltage of the proposed CP circuit. The number of stages determines the power efficiency because of V_{out} and VDD, which are determined by the specific CMOS process [18].

Die layout of the proposed CP circuit with I/O padded structure is shown in Figure 2, where the CP circuit without I/O pad occupies only a small area of $224.2 \mu\text{m} \times 73.2 \mu\text{m}$. During the design process, all transistors and capacitors are placed in a manner that reduces the mismatch and parasitic capacitance. Figure 2 shows the chip layout of the proposed CP circuit with I/O pads.

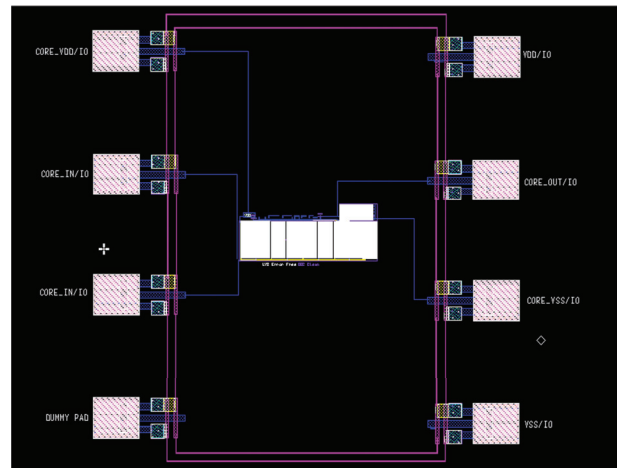


Figure 2: Die layout of the proposed CP circuit with I/O pads.

3 Results and discussions

The operating temperature was set to 27° C for the CTS CP circuit and the ELDOSPICE simulator (Mentor Graphics) was used within Silterra 0.13 μm CMOS process. VDD for simulating the outputs is set to 1.2 V. The simulated behaviour of the CTS CP circuit is illustrated in Figure 3. Figure 3 shows the simulated output voltage waveform of the proposed eight-stage CP circuit with

2pF pumping capacitors. Ideally, the output voltage of the designed eight-stage CP circuit with power supply voltage $V_{DD}=1.2\text{ V}$ should be as high as 9.6 V ($1.2 \times 8 = 9.6\text{ V}$). However, the output voltage of the proposed CP circuit is decreased due to some parasitic capacitances at every pumping node and the loading of the output current. Therefore, the simulated output voltage of the proposed CP circuit is achieved $V_{out} = 9.56\text{ V}$.

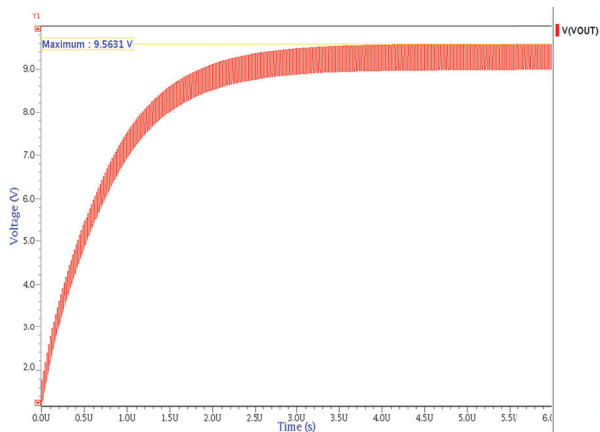


Figure 3: The simulated waveform of the proposed CTS CP circuit.

In this proposed design, both the clock signals (CLK and CLKB) amplitude is set to 1.2 V as same as the supply voltage. The circuit is simulated using 10.2 MHz clock frequency to observe the pumping performance of the proposed CP circuit. If the clock frequency is increased, the charge is transferred over a fixed time interval from one step to another in a faster way, which also increases the output voltage. At 50 MHz clock frequency, the proposed CP circuit exhibited the best performance. In this proposed design, increasing the clock frequency raises the output voltage gain, but incomplete charge transferring occurs if the circuit operates above 50 MHz clock frequency.

On the other hand, the proposed CP circuit is simulated for all 45 corners. In this research, $3 V_{cc}$ (1.1 V , 1.2 V , and

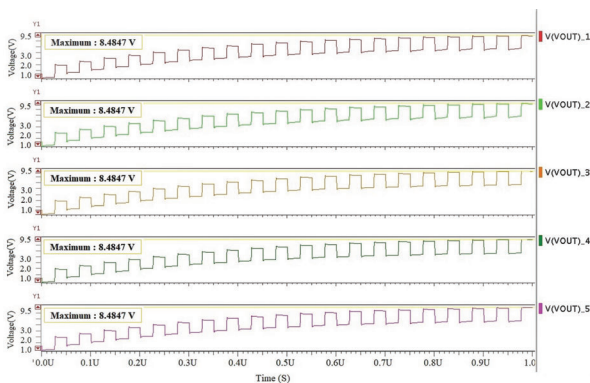


Figure 4: Post layout corner analysis of the proposed CP circuit.

1.3 V), three temperatures (-40°C , 27°C and 125°C), and five corners are examined, as shown in Figure 4. This corner analysis and process variation tests ensure the proposed CTS based CP circuit function correctly within manufacturing tolerances, which is compulsory in CMOS design. The corner test results revealed that the proposed CP circuit could function properly at different corners of V_{DD} and temperature.

The proposed design of the CP circuit achieved output voltage $V_{out} = 9.56\text{ V}$, which is higher than recently published research works, as shown in Figure 5. The simulated results discovered that [16] and [19] CP circuits achieved poor V_{out} due to threshold voltage loss and high parasitic capacitances in every node of the pumping stages. Conversely, to compare the simulated results with recently published research works, this proposed design is tested with different supply voltages, which is shown in Figure 5. From this comparison, it is evident that this novel CP circuit performed better than other research works for all the supply voltage values from 1.2 V to 2.4 V .

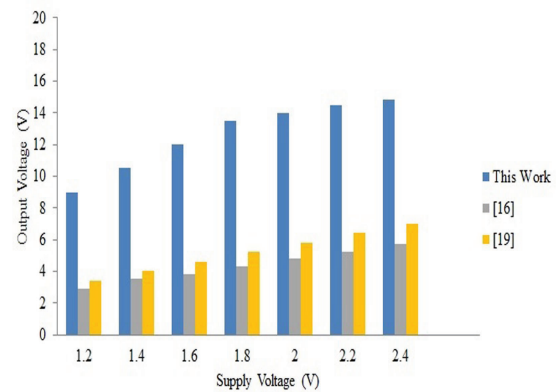


Figure 5: Comparison of output voltages against supply voltages among [16],[19] and this work under $1.2 \leq V_{DD} \leq 2.4$.

On the other hand, the comparison results of the load current against different V_{DD} among the proposed CP circuit, [16] and [19] are shown in Figure 6. From Figure 6, it is observed that the proposed CP circuit can operate successfully with a higher load current under different supply voltage ranges from 1.2 V to 2.4 V . The higher the load current a CP can drive the better its performance, so from Figure 6, it can be said that the proposed CP circuit's performance is better compared to [16] and [19] with higher load current.

Moreover, in this proposed design, a small number of pumping capacitors are utilized the parasitic capacitors (C_{par}) are removed as shown in [16], which helps to trim down the parasitic capacitance effect and leads to reduced load current against different supply volt-

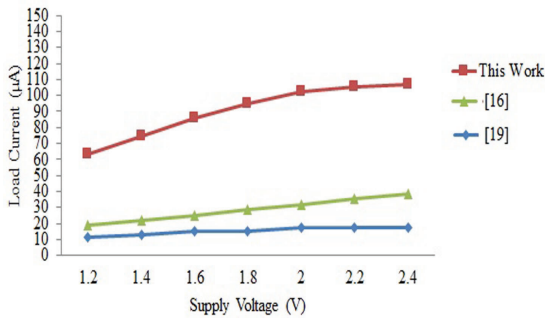


Figure 6: Comparison of load current against supply voltages among [16],[19] and this work under $1.2 \leq VDD \leq 2.4$.

age ranges $1.2 \leq VDD \leq 2.4$. The proposed CP circuit attained a higher output voltage V_{out} at a low power supply voltage as this proposed topology can reduce the parasitic capacitance effect. Moreover, by using the backward control process with the dynamic CTS scheme, the triple well MOSFETs are turned on/off successfully. This proposed design CP circuit achieved lower power dissipation compared to recently published research works within a supply voltage ranges from 1.2 V to 2.4 V. At $VDD = 1.2$ V the power consumption of CP circuit from [19] was $51.57 \mu W$. At the same voltage level, the CP circuit from [16] consumed $171.25 \mu W$.

On the other hand, the proposed CP circuit dissipates only $15.26 \mu W$, which is much lower than the recently published research works. The power efficiency at $VDD = 1.2$ V is calculated using equation (5) for [16], [19] and the proposed CP circuit with a different number of stages, which is shown in Figure 7. From Figure 7 it is found that for a different number of steps the proposed CP circuit can produce higher pumping efficiency up to 79.3% at 10.2 MHz using 2 pF pumping capacitances, which are much higher compared to [16] and [19].

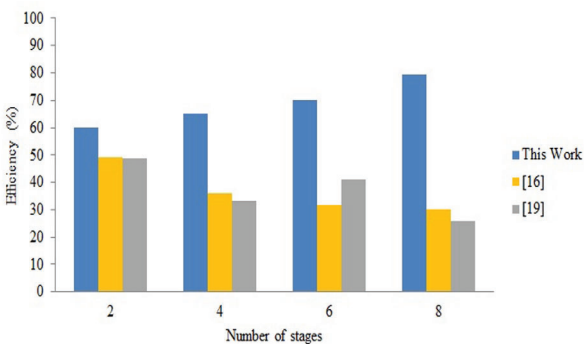


Figure 7: Graphical representation of the power efficiency of various CP circuits for different numbers of stages.

The size of each pumping capacitor of the CP circuit must be equal to get better comparison results. Conse-

quently, every pumping capacitors of the proposed CP circuit, [16] and [19] circuits was set to 2 pF, 1 pF, and 0.1 pF, respectively. For HVG compatible CP circuit, power efficiency can be expressed as,

$$\eta_{power} = \frac{V_{out} \cdot I_{out}}{(VDD - V_t) \cdot I_{in}} = \frac{V_{out}}{(N + 1)(VDD - V_t)} \quad (5)$$

The number of stages only determines the power efficiency of V_{out} and VDD is fixed by the application [18]. Compared to the initial Dickson CP circuit, when the diodes have zero V_t , the power efficiency is improved by $VDD / (VDD - V_t)$ using equation (5). Of course, the result is higher when VDD is low. The power efficiency at $VDD = 1.2$ V is measured for [16] and [19]. The proposed CP circuit with a different number of stages is, as shown in Figure 6. Table 1 summarizes the comparison studies among the proposed CP circuits along with the recently published research works.

Compared to all recently published research works, the proposed CP circuit has achieved the highest output voltage of 9.56 V under a supply voltage of 1.2 V, as shown in Table 1. In this design, the W/Ls of MD1 and MD2 were increased and the W/Ls of MS1-MS9 decreased, which helped to produce a higher output voltage, which is better than all the previous research outputs. However, [20] is made slightly higher output than this research work, which is achieved due to the higher supply voltage compared to this research work. Moreover, the proposed design achieved the highest pumping efficiency of 79.3%, which is better than [19, 21-22]. The result is achievable, as it has a smaller number of parasitic capacitances to turn out higher efficiency under low supply voltages. The pass transistors (MNs and MPs) were used in this design to prevent voltage loss and reverse the charge-sharing mechanism, which also improves the process of charge transfer and boosts the output voltage. In this research, the frequency was set to 10.2 MHz for the two anti-phase clock signals of the proposed CP circuit, which met the required specifications of the HVG.

Moreover, the designed CP circuit can perform up to 50 MHz, which makes the proposed design superior to [16, 20, 21-22]. In terms of accessibility. From the comparison table, it is also found that the proposed design has the lowest power dissipation of only $15.26 \mu W$ with eight stages of pumping capacitors, which is better than [16, 19, 21]. The proposed CP circuit used the triple well NMOS switch to control the CTSs dynamically instead of diode-configured switches in all stages. Hence, no substrate current is formed throughout the dynamic control process. Using PMOS transistors results in a substrate current at each step during

Table 1: Performance comparison of different cp circuits.

References	[16]	[17]	[19]	[20]	[21]	[22]	[23]	This Work
Technology (μm)	0.35	0.13	0.18	0.18	0.35	0.35	0.13	0.13
Supply Voltage (V)	3.3	1.5	1.8	2	3.3	3.3	1.2	1.2
Clock Frequency (MHz)	3	20	20	0.78	5	1.6~5.5	8	10.2
Number of Stages	4	5	4	8	6	4-8	3	8
Output Voltage (V)	3.18	6.32	5.95	9.8	14	4.8 ~ 8.5	3.08, -3	9.56
Power Consumption (μW)	304.76	-	205.56	-	150.48	-	-	15.26
Layout area(μm^2)	-	-	40x60	154x105	-	-	0.5mm ²	224.29 x 86
Efficiency (%)	-	-	25	-	31	75	60	79.3

the charge transfer process. As a result, the proposed CP circuit dissipated lower power with better reliability compared to recently published research works.

4 Conclusions

An enhanced CP circuit is illustrated in this research by using the four-stage CTS scheme to move the charges directly with improved pumping efficiency. Design and pre-fabrication simulation of the CP circuit was done with only 15.26 μW power dissipation, which was lower compared to recently published research works. 9.56 V of boosted internal supply voltage was obtained and 79.3 % pumping efficiency was achieved by decreasing the parasitic capacitance effects. Again, these were the highest value among compared research works. From these analyses, it is evident that the designed CP circuit can perform in low voltage devices with lower parasitic capacitances, which results in lower power consumption compared to previous designs.

5 Acknowledgements

The authors would like to express sincere gratitude to the research grant GUP-2017-069 from Universiti Kebangsaan Malaysia for financial support.

6 Conflict of interest

There is no conflict of interest among the authors.

7 References

- Rahman, L. F., Marufuzzaman, M., Alam, L., Sidek, L. M., & Reaz, M. B. I. "A low power and low ripple CMOS high voltage generator for RFID transponder EEPROM", P. one, vol. 15, no. 2, pp. e0225408, 2020, <https://doi.org/10.1371/journal.pone.0225408>.
- Javidan, J., Atarodi, S. M. & Luong, H. C. "Circuit and system design for an 860–960MHz RFID reader front-ends with Tx leakage suppression in 0.18 μm CMOS technology", Int. J. of Circ. Theory and App., vol. 40, no. 9, pp.957-974, 2012, <https://dl.acm.org/doi/10.1002/cta.765>.
- Rahman, L. F., Reaz, M. B. I., & Marufuzzaman, M. "Design of Low Power and Low Phase Noise Current Starved Oscillator for RFID Tag EEPROM", Inf. MIDEM, vol. 49, no. 1, pp. 19-24, 2019, <http://ojs.midem-drustvo.si/index.php/InfMIDEM/article/viewFile/646/248>.
- Kuo, K.C. & Chang, K.M. "Embedded Flash Memory: Non-volatile Memory Technologies with Emphasis on Flash", J. W. & S., Inc, 2007.
- Ohsaki, K., Asamoto, N. & Takagaki, S. "A single poly EEPROM cell structure for use in standard CMOS processes", IEEE J. of Sol. Sta. Circ., vol. 29, no. 3, pp. 311-316, 1994, <https://ieeexplore.ieee.org/document/278354>.
- Zhao, D., Yan, N., Xu, W., Yang, L.; Wang, J. & Min, H. "A Low-power, Single-poly, Non-volatile Memory for Passive RFID Tags", Chin. J. of Sem., vol. 29, no. 1, pp. 99-104, 2008, <http://www.jos.ac.cn/fileB-DTXB/journal/article/jos/2008/1/PDF/07070303.pdf>.
- Wang, B., Nguyen, H., Ma, Y. & Paulsen, R. "Highly Reliable 90-nm Logic Multi-time Programmable NVM Cells Using Novel Work-Function-Engineered Tunneling Devices", IEEE Trans. on Elec. Dev., vol. 54, no.9, pp.2526-2530, 2007, <https://ieeexplore.ieee.org/document/4294246>.
- Raszka, J., Advani, M., Tiwari, V., Varisco, L., Hacobian, N.D., Mittal, A., Han, M., Shirdel, A. & Shubat, A. "Embedded flash memory for security applications in a 0.13 μm CMOS logic process", Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC 2004), Pennsylvania, USA, 2004, pp. 46-512, <https://ieeexplore.ieee.org/document/1332586>.
- Mohammad, M.G., Ahmad, M.J. & Al-Bakheet, M.B. "Switched positive/negative charge pump design using standard CMOS transistors", IET Circ. Dev.

- Sys., vol.4, no.1, pp.57–66, 2010, <https://ieeexplore.ieee.org/abstract/document/5378439>.
10. Rahman, L. F., Ariffin, N. B., Reaz, M. B. I., & Marufuzzaman, M. "High-Performance CMOS Charge Pumps for Phase-locked Loop", *Trans. on Elec. and Elec. Mat.*, vol. 16, no. 5, pp. 241-249, 2015, <http://koreascience.or.kr/article/JAKO201536553130616.page>.
 11. Tanzawa, T.; Takano, Y.; Watanabe, K. & Atsumi, S. "High-voltage transistor scaling circuit techniques for high-density neither negative-gate-channel-erasing NOR flash memories", *IEEE J. of Sol. Sta. Circ.*, vol. 37, no. 10, pp. 1318-1325, 2002, <https://ieeexplore.ieee.org/document/1035946>.
 12. Tanzawa, T., Tanaka, T., Takeuchi, K. & Nakamura, H. "Circuit techniques for a 1.8-V-only NAND flash memory", *IEEE J. of Sol. Sta. Circ.*, vol. 37, no. 1, pp. 84-89, 2002, <https://ieeexplore.ieee.org/document/974549>.
 13. Kawahara, T., Kobayashi, T., Jyouno, Y., Saeki, S., Miyamoto, N., Adachi, T., Kato, M., Sato, A., Yugami, J., Kume, H. & Kimura, K. "Bit-line clamped sensing multiplex and accurate high voltage generator for quarter-micron flash memories", *IEEE J. of Sol. Sta. Circ.*, vol. 31, no. 11, pp. 1590-1600, 1996, <https://ieeexplore.ieee.org/document/542303>.
 14. Dickson, J.F. "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique", *IEEE J. of Sol. Sta. Circ.*, vol. 11, no. 3, pp. 374-378, 1976, <https://ieeexplore.ieee.org/abstract/document/1050739?section=abstract>.
 15. Yan, N. & Min, H. "A high efficiency all PMOS charge pump for low-voltage operations", *Proceedings of the IEEE Asian Solid-State Circuits Conference (ASSCC 2005)*, Hangzhou, China, 2005, pp.361-364, <https://ieeexplore.ieee.org/document/4017606>.
 16. Dong-Sheng, L., Xue-Cheng, Z., Fan, Z. & Min, D. "Embedded EEPROM Memory Achieving Lower Power - New design of EEPROM memory for RFID tag IC", *IEEE Circ. and Dev. Mag.*, vol. 22, no. 6, pp. 53-59, 2006, <https://ieeexplore.ieee.org/document/4099517>.
 17. Wang, X., Wu, D., Qiao, F.; Zhu, P., Li, K., Pan, L. & Zhou, R. "A High-Efficiency CMOS Charge Pump for Low Voltage Operation", *Proceedings of the IEEE 8th International Conference on ASIC (ASICON '09)*, Changsha, Huan Chen, China, 2009, pp.320-323, <https://ieeexplore.ieee.org/document/5351437>.
 18. Wu, J.-T., Chang, Y.-H. & Chang, K. L. "1.2 V CMOS switched-capacitor circuits", *IEEE 42nd International Conference on Solid-State Circuits*, 1996, pp. 388-389, <https://ieeexplore.ieee.org/document/488729>.
 19. Wei, K. C., Amin, M. S. & REAZ, B. I. "Low voltage charge pump circuit using 0.18 μm CMOS technology", *Rev. Roum. Sci. Techn. – Électrotechn. et Énerg.*, vol. 58, no. 1, pp. 83–92, 2013, http://revue.elth.pub.ro/upload/128885Art09_KWei83-92.pdf.
 20. Peng, F., Yunlong, L. & Nanjian, W. "A high-efficiency charge pump circuit for low power applications", *J. of Sem.*, vol. 31, no. 1, pp. 015009, 2010, <https://iopscience.iop.org/article/10.1088/1674-4926/31/1/015009>.
 21. Yan, L., Shilin, Z. & Yiqiang, Z. "High voltage generator circuit with low power and high efficiency applied in EEPROM". *J. of Sem.*, vol. 33, no. 6, pp. 065006, 2012, <https://iopscience.iop.org/article/10.1088/1674-4926/33/6/065006/meta>.
 22. Jeong, H.-I., Park, J.-W., Choi, H.-Y. & Kim, N.-S. "High-Performance Charge Pump Converter with Integrated CMOS Feedback Circuit". *Tran. on Elec. and Elec. Mat.*, vol. 15, no. 3, pp. 139-143, 2014, <https://doi.org/10.4313/TEEM.2014.15.3.139>.
 23. Maghami, M. H., Sodagar, A. M., Sawan, M., "Versatile stimulation, back-end with programmable exponential current pulse shapes for a retinal visual prosthesis", *IEEE Trans. on Neu. Sys. and Rehab. Eng.*, vol. 24, no. 11, pp. 1243-1253, 2016, <https://ieeexplore.ieee.org/document/7444183/>.



Copyright © 2020 by the Authors. This is an open access article distributed under the Creative Commons Attribution (CC BY) License (<https://creativecommons.org/licenses/by/4.0/>), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Arrived: 02. 10. 2020

Accepted: 01. 12. 2020