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High-Gain Super Class-AB Bulk-driven Sub-threshold Low-Power CMOS Transconductance Amplifier for Biomedical Applications

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Abstract: This article describes a high-gain sub-threshold region-operated bulk-driven (BD) super class-AB power-efficient single-stage operational transconductance amplifier (OTA) with enhanced unity gain frequency (UGF). The proposed amplifier has a BD adaptively biased flipped voltage follower (FVF) differential input pair functioning in class-AB mode to raise the dynamic current and subsequently raise the UGF, and slew rate. Additionally, the core circuit of the proposed OTA employs partial positive feedback (PPF) to magnify the circuit's effective input transconductance and gain. Moreover, the circuit's overall gain is moved up by using three additional low-power current mirror loads, two of which are FVF current mirrors and one of which is a self-cascode current mirror, placed at the output. The proposed OTA circuit and its traditional counterpart are developed and simulated on the Cadence Spectre tool by exploiting UMC 0.18µm CMOS process technology, both circuits are biased with a minimal supply of 0.5V. The simulation results exhibit that the proposed circuit delivers 72.35dB open loop DC gain, 61.33º phase margin, and 18.706 kHz UGF with a consumption of only 62.82nW power. The performance outcomes ensured the suitability of the proposed OTA circuit for biomedical applications.

Keywords: Adaptive biasing, Bulk-driven OTA, FVF, Partial Positive Feedback, Self-cascode

Ojačevalnik prevodnosti CMOS z nizko močjo in velikim ojačenjem Super Class-AB za biomedicinske aplikacije

Izvleček: V članku je opisan enostopenjski operacijski transkonduktančni ojačevalnik (OTA) z visokim ojačenjem, ki deluje v podpražnem območju in je voden preko substrata (BD), ki je energetsko učinkovit in ima povečano frekvenco enotnega ojačenja (UGF). Predlagani ojačevalnik ima BD adaptivno pristranski diferencialni vhodni par z obrnjenim napetostnim sledilnikom (FVF), ki deluje v načinu razreda AB za povečanje dinamičnega toka in posledično povečanje UGF in hitrosti premikanja. Poleg tega jedro vezja predlaganega ojačevalnika OTA uporablja delno pozitivno povratno zvezo (PPF) za povečanje učinkovite vhodne transkonduktivnosti in ojačitve vezja. Poleg tega se celotno ojačenje vezja poveča z uporabo treh dodatnih tokovnih zrcal z nizko porabo, od katerih sta dve tokovni zrcali FVF, eno pa je tokovno zrcalo s samokaskodo, ki je nameščeno na izhodu. Predlagano vezje OTA in njegovo tradicionalno analogno vezje sta razvita in simulirana v orodju Cadence Spectre z uporabo 0,18µm CMOS procesne tehnologije UMC, obe vezji sta obremenjeni z minimalnim napajanjem 0,5 V. Rezultati simulacije kažejo, da predlagano vezje zagotavlja 72,35 dB DC ojačitve v odprti zanki, 61,33º fazno razliko in 18,706 kHz UGF s porabo samo 62,82 nW energije. Rezultati delovanja so zagotovili primernost predlaganega vezja OTA za biomedicinske aplikacije.

Ključne besede: prilagodljiva pred napetost, množično voden OTA, FVF, delna pozitivna povratna zanka, samo-kaskoda

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1 Introduction

Over the last few years, due to the advancement of CMOS technology, there is a continuous requirement for portable handset electronic devices like laptops, notepads, wireless sensor networks, mobile phones, biomedical implantable devices, etc in our everyday lives. The medical field is also drastically changing towards portability to continuously monitor patient health [1-5], this makes the attraction in the evaluation of ultra-low-voltage, low-power circuit designs for portable applications. Analog circuit designers are still rigorously working in this field and illustrating different design techniques for low voltage in the literature [6-8].

As the most fundamental block in an analog circuit, the OTA plays a pivotal role in analog front-end circuits used in biomedical data acquisition systems. Electromyograms (EMG), Electroencephalograms (EECG), Electrocardiograms (ECG), and other bio-potential signals are low voltage (amplitude in mV), and low-frequency signals with only a few kHz range. Rail-to-rail input/output swing, high DC gain, low noise, high linearity, and minimal power consumption are the basic requirements of the OTA used in biomedical applications [3]. Achieving these characteristics using a low power supply in deep submicron technologies is really a challenge. The conventional gate-driven technique is unsuitable for application under a 1V environment because of the threshold voltage constraint; OTA's restricted linear range and high power consumption are two of its biggest flaws. The weak-inversion design technique is well-suited to reduce power consumption, as the necessary drain-to-source voltage (V_{DS}) for strong inversion is 250 mV, which is decreased to about 78 mV [5, 9-11]. An alternate approach for operating rail-to-rail is to use the bulk-driven (BD) technique, which can prevail over the aforementioned linearity and threshold voltage restrictions. The bulk-driven technique in combination with the sub-threshold technique is preferable for biomedical applications, as the combined effect of both techniques increases linearity and reduces power consumption. Although the bulk-driven technique increases input common-mode range (ICMR), it reduces open-loop DC gain, and UGF and raises input-referred noise, since the gate transconductance (g_m) is (2.5–5) times higher than the bulk transconductance (g_{mb}) [12-16]. A number of bulk-driven OTA designs are described to improve the above-mentioned disadvantages of reduced bulk-transconductance under sub-1V environments in the literature [10-19], and also discussed in the references [20-22] in extremely low voltage conditions with very little power loss. Despite being the most power-efficient, single-stage amplifiers cannot deliver enough gain, in order to provide high gain, cascode techniques are used earlier. This approach is no longer used since it lowers output voltage swings. A self-cascode (SC), as described in references [5, 11, 14, 16], is an excellent approach to carry a strong DC gain and great output swing. It consists of two transistors but is handled as a single composite transistor. When SC loads are used, the output impedance roughly increases by a factor of 10, which is comparable to a gain improvement of about 20 dB. The composite SC loads don't require any extra bias sources to drive the cascode transistors and hence maximize the voltage gain. Some authors utilize partial positive feedback (PPF) techniques mentioned in [5, 12, 16, 17, 23-29] to improve the input core bulk- transconductance and hence improve the small-signal performances of bulk-driven OTAs, but the enhancement of the large-signal performances is not mentioned in these techniques.

This paper presents an improved bulk-driven low-power single-stage super class-AB OTA [12, 26, 30-32], operated in a sub-threshold region, which has been termed as super class-AB bulk-driven sub-threshold (SBDST) OTA in the whole paper. The proposed amplifier utilizes an adaptive bias technique in the input differential pair based on a BD-FVF [26, 31] functioning in the class-AB mode to improve the dynamic current and unity gain frequency. The partial positive feedback (PPF) technique has been exploited in the core circuit to improve the overall effective input transconductance and hence gain of the circuit. In addition to the improvement of input transconductance, output impedance also increases by using low power and high performance three current mirrors at the output, hence, the overall gain of the circuit further raises. The proposed SBDST OTA offers significant open loop DC gain, UGF, and slew-rate while exploiting minimal power, by utilizing the aforementioned techniques.

This paper is structured as follows: The study of conventional OTA is covered in Section 2, along with a thorough circuit description of both the proposed and conventional OTA. Section 3 discusses the proposed OTA's intricate circuit analysis. In Section 4, the simulation outcomes of conventional and proposed OTA including Monte Carlo, process corner analysis, and layout are covered. Section 5 compares the proposed OTA's performance to those of the other previously reported designs, and Section 6 finally brings to a conclusion of the paper.

2 Circuit Descriptions

2.1 Conventional Bulk-driven Sub-threshold (BDST) OTA

The conventional BDST OTA, in which the input core circuit is designed using bulk-input PMOS transistors PI_{1a}-

PI_{1b}, is depicted in Fig. 1. The differential input transistor pair working in the sub-threshold region is biased by using transistor P_B; the drain current (I_{DS}) of a transistor operating in sub-threshold is expressed as [11]:

$$I_{DS} = I_s \left(\frac{W}{L}\right) e^{\left(q\frac{V_{GS}-V_{Tn}}{nKT}\right)} \left[1 - e^{\left(q\frac{-V_{DS}}{KT}\right)}\right] \quad (1)$$

where I_S and K are the characteristic current of the sub-threshold and Boltzmann constant, n is the slope of the curve in the sub-threshold region, T is the absolute temperature and q is the charge of electron respectively.

The transistors are in saturation in the sub-threshold region if $V_{DS} \geq 3V_T$, where ($V_T = KT/q$) is the thermal equivalent voltage and its value at 27° is 26 mV.

Applying the condition $V_{DS} \geq 3V_T$ in (1), then the term $e^{\left(q\frac{-V_{DS}}{KT}\right)} \ll 1$, hence the equation (1) simplifies to

$$I_{DS} = I_s \left(\frac{W}{L}\right) e^{\left(q\frac{V_{GS}-V_{Tn}}{nKT}\right)} \quad (2)$$

The output of differential input pair consists of NMOS transistor pair ($N_{1a\text{-}3a} - N_{1b\text{-}3b}$), form the non-linear current mirrors with a current transfer ratio $K_1 = 2$. These current mirrors known as the adaptive loads [26], are loads of the input transistor pair. The output of the adaptive loads is routed to the summing stage, which is at the circuit's output, to raise the output impedance. The summing stage of the conventional OTA uses PMOS transistors ($P_{2a\text{-}2b} - P_{3a\text{-}3b}$) as a current mirror to boost the largely dc gain of the circuit. The conventional BDST OTA's effective transconductance is provided by:

$$G_{m,BDST} = K_1 . g_{mb1,a/b} \quad (3)$$

where g_{mb1} represents the bulk-transconductance of input transistors.

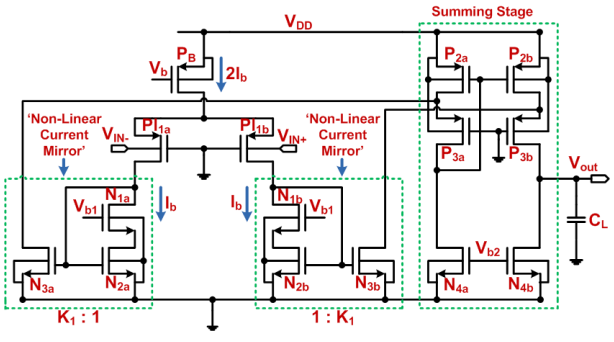

Figure 1: Conventional Bulk-driven sub-threshold (BDST) OTA

The output impedance R_{out} of the BDST OTA is provided as:

$$R_{out} = [r_{o4,bN} || (r_{o3,bP} + (r_{o3,bN} || r_{o2,bP}))] \quad (4)$$

since, $r_{o3,bP} >> (r_{o3,bN} || r_{o2,bP})$

therefore, equation (4) is simplified as:

$$R_{out} = (r_{o4,bN} || r_{o3,bP}) \quad (5)$$

Effective transconductance and the circuit's output impedance combine to provide the open loop dc gain (A_v), which is expressed as:

$$A_{V,BDST} = G_{m,BDST} . R_{out}$$
$$A_{V,BDST} = K_1 . g_{mb1,a/b} . (r_{o4,bN} || r_{o3,bP}) \quad (6)$$

The main problem of conventional BDST OTA is a very low open-loop gain, it is only about 32 dB. A non-linear current mirror is employed here to increase the amplifier's slew rate and unity gain frequency (UGF), which can be evaluated with capacitive load C_L by the following equations:

$$UGF_{BDST} = \frac{K_1 . g_{mb1,a/b}}{2\pi C_L} \quad (7)$$

$$SR_{BDST} = \frac{2.K_1 . I_B}{C_L} \quad (8)$$

The values of UGF and slew rate of the conventional amplifier are 1.637 kHz, and 0.92V/ms respectively, which are quite low. Therefore, some structural change is required in the amplifier to get better the whole performance of the conventional BDST OTA concerning open-loop gain, slew rate, UGF, etc.

2.2 Proposed SBDST OTA

We proposed the super class-AB bulk-driven sub-threshold (SBDST) OTA, which is depicted in Fig. 2, to enhance the performance of conventional BDST OTA. Its input core makes use of two identical adaptively biased BD-FVF pair, eliminating the bias current source of the conventional circuit, which is supplied by P_B in Fig. 1.

The best possible dimensions of transistors are selected to function the proposed SBDST in a sub-threshold region so that the circuit can obtain low power operation i,e., below 100nW. To extend the input common-mode range (0 to V_{DD}) of the circuit bulk-driven differential pair is used in the input stage, however, gate transconductance (g_m) is (2.5–5) times more than the bulk transconductance (g_{mb}) [12]. Consequently, the

circuit's effective transconductance decreases, and hence, the gain and UGF of the circuit are also considerably low. To overcome these limitations an adaptive biased super class-AB [26, 31, 32] is incorporated into the input core. The BD-FVF pair at the input consists of bulk-driven transistors PI_{1a}-PI_{1b}, diode-connected transistors PI_{3a}-PI_{3b} connected in negative feedback [31, 32], and the current source made by transistors NI_{5a}-NI_{5b}. The input core of the SBDST is made up of adaptively biased input differential pair PI_{2a}-PI_{2b} and adaptive loads. Non-linear current mirrors ($N_{1a\text{-}3a}$ - $N_{1b\text{-}3b}$) with a current ratio of $1{:}K_1$ are called adaptive loads. The source terminal of FVF pair is the output node that has very low impedance, given by $\frac{1}{g_{m3a}\, g_{m1a} r_{o1a}}$. The FVF is capable to source a significant amount of current even greater than the bias current I_b on the variation of differential input voltage because of the low impedance at the output node. Hence, the FVF pair in combination with the adaptive biased differential pair makes the proposed OTA function in class-AB. This combination eliminates the limitations of traditional BDST OTA.

Differential input signals V_{in-} and V_{in+} are applied across the bulk terminal of transistors PI_{1a}-PI_{1b} as well as to the bulk terminal of adaptive biased differential pair PI_{2a}-PI_{2b}. Due to the voltage follower action of FVF, the transistor PI_{1a} source terminal is also V_{in-}. This terminal is named C as shown in Fig.2 and is also connected to the source terminal of the transistor PI_{2a}, hence, the total signal voltage that appears across the transistor PI_{2a} is $V_{BS} = [V_{in+} - V_{in-}] = [V_{in+} - (-V_{in+})] = 2\,V_{in+}$. Similarly, the V_{BS} of the transistor PI_{2b} is $2V_{in-}$. Therefore, the proposed SBDST OTA's effective transconductance is twice as much as that of the traditional OTA and is equal to $2g_{mb1,a/b}$.

Since the transconductance of the SBDST increases, so the gain and UGF are also increase. To further enhance the transconductance, and gain, the PPF technique has been introduced using transistors N_{4a} and N_{4b} at adaptive load ends of the input core, shown in Fig. 2 inside the box colored green. The PPF loop increases the overall input transconductance but with a little loss of phase margin (PM), as it generates a non-dominate pole at node *E* of the SBDST OTA. Therefore, a small compensation capacitor C_C is used between the drain of NI_{5b} and the output node.

In addition to the improvement of transconductance, output impedance is also enhanced using three current mirrors at the output of the circuit. Among these mirrors, two are highly-effective FVF current mirrors [5] with a current gain factor of 1.25, and one is a self-cascode current mirror. In composite SC structure, the aspect ratio of the cascode transistor and the transistor connected to the supply is set to 20, to operate in saturation in the sub-threshold region [11, 16]. Hence, by raising the input stage's transconductance and the output stage's output impedance, the proposed SBDST OTA's overall performance is enhanced.

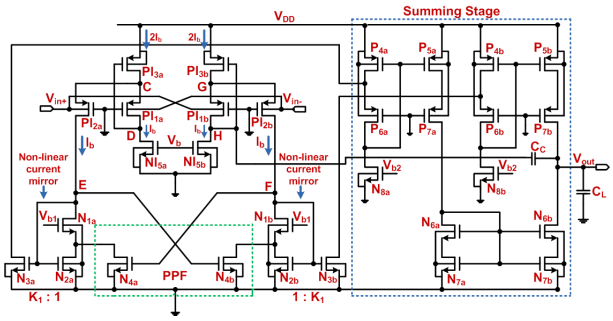

Figure 2: Proposed SBDST OTA

3 Explanation of the proposed SBDST OTA

This section describes the SBDST OTA's overall transconductance, voltage gain, UGF, and stability.

3.1 Effective transconductance and UGF

The half sub-circuit of the input core of SBDST and its small signal AC equivalent circuit are depicted in Fig. 3a and b.

The input signals V_{in-} and V_{in+} are applied to the bulk terminal of the transistors PI_{1a} and PI_{2a} respectively, assuming the voltage at their source terminals is V_C, and

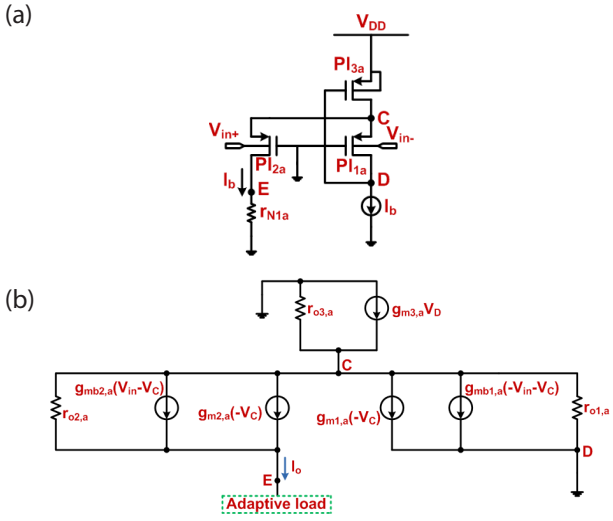

Figure 3: (a) Input core's half circuit of SBDST OTA, (b) half circuit small signal equivalent model

the transistor PI_{3a} gate voltage is V_D. The drain terminal of PI_{1a} is also connected to point D, so its drain voltage is also V_D. A constant DC source I_b made by transistors NI_{5a}-NI_{5b} biases the transistor PI_{1a}. As a result, zero AC small signal current passes through the input transistor PI_{1a} [31].

And all the AC signal current of PI_{3a} is the output AC small signal current I_o which flows through the transistor PI_{2a} [12, 26,31,32]. The effective overall transconductance of the proposed OTA is calculated from the following equations,

The small signal current through transistor PI_{1a} at node *D* is given by:

$$g_{m1,a}\left(-V_C\right)+g_{mb1,a}\left(-V_{in}-V_C\right)+\frac{\left(V_C-V_D\right)}{r_{o1,a}}=0 \quad (9)$$

and the output current I_o contributed by PI_{2a} is expressed as:

$$I_o=g_{m2,a}\left(-V_C\right)+g_{mb2,a}\left(V_{in}-V_C\right)+\frac{\left(V_C-V_E\right)}{r_{o2,a}} \quad (10)$$

Neglecting the output resistance term from both equations since its value is very high.

So, Eq. (9) can be approximated as:

$$g_{m1,a}\left(V_C\right)+g_{mb1,a}\left(V_{in}+V_C\right)=0 \quad (11)$$

$$\Rightarrow \left(g_{m1,a}+g_{mb1,a}\right)V_C=-g_{mb1,a}V_{in} \quad (12)$$

$$\Rightarrow \quad V_C=\frac{-g_{mb1,a}V_{in}}{\left(g_{m1,a}+g_{mb1,a}\right)} \quad (13)$$

Eq. (10) can be written as:

$$I_o=g_{mb2,a}V_{in}-V_C\left(g_{m2,a}+g_{mb2,a}\right) \quad (14)$$

Putting the value of V_C from Eq. (13) to Eq. (14) and solving it in terms of V_{in}, then the equation becomes:

$$I_o=g_{mb2,a}V_{in}+\frac{g_{mb1,a}V_{in}}{\left(g_{m1,a}+g_{mb1,a}\right)}\left(g_{m2,a}+g_{mb2,a}\right) \quad (15)$$

Since the transistors PI_{1a} and PI_{2a} are identical, therefore

$$g_{m1,a}=g_{m2,a} \text{ and } g_{mb1,a}=g_{mb2,a} \quad (16)$$

Putting the above relations into Eq. (15), then the value of I_o can be simplified as:

$$I_o=2g_{mb1,a}V_{in} \quad (17)$$

As the circuit is symmetry, therefore the input core transconductance is given as:

$$\mathrm{G_{m,\,input\ core}}=\frac{\mathrm{I_o}}{\mathrm{V_{in}}}=2\mathrm{g_{mb1}} \quad (18)$$

Considering the current gain $K_1 = 2$ of the non-linear current mirror together with the partial positive feedback technique employing the transistors N_{4a}, and N_{4b} in the input core, the effective overall transconductance of the proposed SBDST OTA is provided by:

$$\mathrm{G_{m,\,effective}}\big|_{\mathrm{SBDST}}=\mathrm{K_1}\frac{2\mathrm{g_{mb1}}}{(1-\alpha)} \quad (19)$$

where K1 and α are the aspect ratios of the transistors given by $\mathrm{K_1}=\frac{\mathrm{g_{m3,\,N}}}{\mathrm{g_{m2,\,N}}}$ and $\alpha=\frac{\mathrm{g_{m4,\,N}}}{\mathrm{g_{m2,\,N}}}$.

The UGF of the SBDST OTA is given by:

$$\mathrm{UGF}=\frac{\mathrm{G_{m,\,effective}}\big|_{\mathrm{SBDST}}}{2\pi\mathrm{C_L}}=\frac{\mathrm{K_1}}{(1-\alpha)}\frac{2\mathrm{g_{mb1}}}{2\pi\mathrm{C_L}} \quad (20)$$

Due to its enhanced effective transconductance value, the proposed OTA provides a significantly higher UGF than the traditional BDST OTA, as shown by expression (20).

3.2 Voltage gain

The SBDST OTA's open loop voltage gain is obtained by multiplying the circuit's output impedance and effective transconductance. The entire circuit's output impedance at the output node is provided by:

$$R_{out}=(g_{m7,bP}r_{o7,bP}r_{o5,bP})\|(g_{m6,bN}r_{o6,bN}r_{o7,bN}) \quad (21)$$

Hence, the proposed SBDST OTA's overall voltage gain is given by:

$$A_V\big|_{SBDST}=G_{m,effective}\big|_{SBDST}R_{out}$$

$$\Rightarrow A_V\big|_{SBDST}=\mathrm{K_1}\frac{2\mathrm{g_{mb1}}}{(1-\alpha)}[(g_{m7,bP}r_{o7,bP}r_{o5,bP})\|(g_{m6,bN}r_{o6,bN}r_{o7,bN})] \quad (22)$$

3.3 Stability analysis

The proposed SBDST OTA introduces a dominant pole (p_1) at the output node owing to its capacitive load and output impedance hence, its frequency is not influenced by the PPF loop and is given as:

$$\mathrm{p_1}=\frac{1}{\mathrm{R_{out}}\left(\mathrm{C_C}+\mathrm{C_L}\right)} \quad (23)$$

where C_C is the small compensation capacitor and C_L is the load capacitance.

The PPF technique employed in the input core causes the non-dominant pole (P_2) at the drain terminal of $N_{2,a/b}$ to shifts towards a lower value, and its value given in [12], is expressed as:

$$p_2 = \frac{\left(g_{m2,N} - g_{m4,N}\right)}{C_P} \quad (24)$$

where C_p indicates the parasitic capacitance at the above-mentioned drain terminal node. This node has a higher impedance due to PPF action. The lower secondary pole value in (24) limits the maximum possible UGF. To ensure a stable phase margin a small compensation capacitor C_C is placed between the drain of NI_{5b} and the high-impedance output node.

4 Simulation results

Using 180nm CMOS process technology, the traditional BDST and proposed SBDST OTAs are driven by only 0.5V supply for a load capacitor of 15pF and are simulated in the Cadence Virtuoso simulator. The bias current I_b of the BD-FVF pair in SBDST OTA is fixed to 10nA and the total stand-by-current under the sub-threshold region of operation is 124nA while that of conventional OTA is 100nA, and the reference temperature for both is 27°C. The bias current used for biasing the high-performance FVF current mirror is 1.2nA. In the design, all the MOSFETs have an optimum value of aspect ratio to lower the influence of channel length modulation and input referred noise of the circuit. Additionally, the bias voltage V_{b1} has been chosen properly to bias the transistor $N_{2,a/b}$ in the triode region, so that the combination of transistors ($N_{1a\text{-}3a} - N_{1b\text{-}3b}$) works as a non-linear mirror.

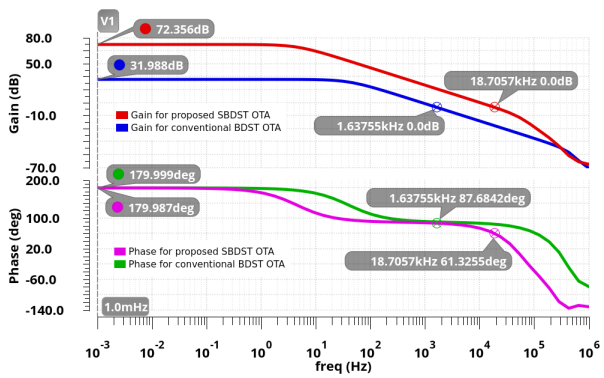

Figure 4: Simulated AC plot of BDST OTA and SBDST OTA

Figure 4 shows the AC responses of conventional BDST OTA and proposed SBDST OTA, the simulation outcomes demonstrate that the open loop DC gain, UGF, and phase margin of the proposed SBDST OTA are 72.356 dB, 18.7057 kHz, and 61.3255° respectively. This result of the proposed OTA exposes that the improvement in DC gain is 2.26 times and in UGF is 11.42 times than the conventional circuit, with a little loss of phase margin. A compensation capacitor of value, C_C = 0.4pF is used in the SBDST OTA, to increase its phase margin above 60°.

The overall effective input core transconductance is exposed in Fig. 5, the proposed SBDST OTA accomplishes a significantly greater effective input core transconductance of 1.76μS compared to 158.5nS of conventional bulk-driven OTA.

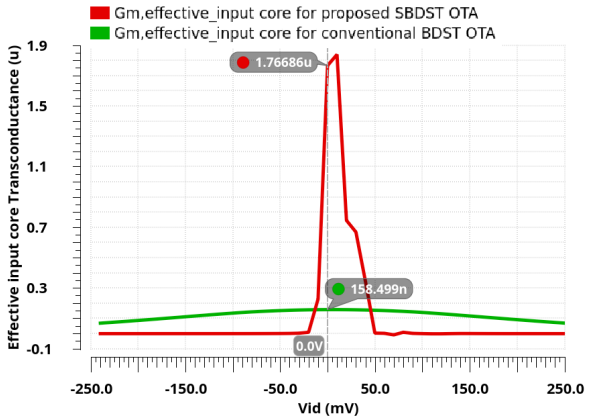

Figure 5: Effective input core transconductance of BDST OTA and SBDST OTA

One of the most crucial factors of an OTA is noise, it is an undesired signal that frequently combines with the desired signal as a result of fluctuations in the power supply or component mismatches, producing unwanted output. In addition to this, the thermal, as well as flicker noise of MOS transistors itself, adds to the overall noise density. Since the range of biosignals is 10mHz ≤ f_{bio} ≤ 1kHz, hence the flicker noise predominates more in bi-

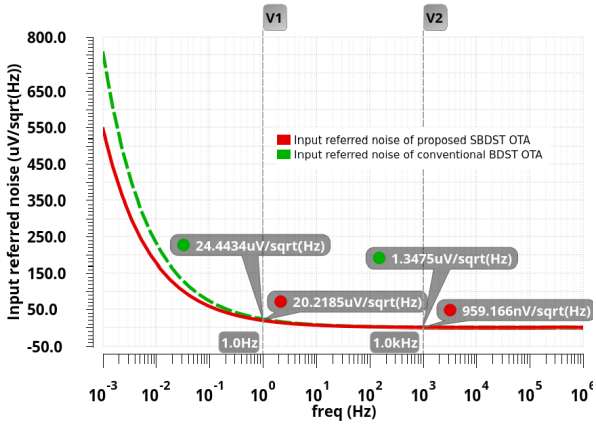

Figure 6: Plot of input referred noise voltage of BDST OTA and SBDST OTA

omedical applications. So, the design of the OTA circuit must assure minimum input-referred output noise for biomedical applications. Figure 6 highlights the input-referred noise produced at the input pair terminals of the proposed and conventional OTA, the SBDST OTA and BDST OTA are found to have input-referred noise (IRN) values of 0.959 μV/√Hz and 1.347 μV/√Hz, respectively, at 1 kHz. Its value is less in the proposed SBDST OTA due to the enhancement in the overall effective transconductance of the input pair.

The PSRR ± and CMRR values must be very large to reject unwanted signals which are generated by variations in the power supply, these unwanted signals are common to both inputs. Figure 7 shows the result of CMRR and PSRR ± of the SBDST OTA, it is found that the proposed SBDST OTA at 1 mHz provides a high CMRR, PSRR+, and PSRR– of values 161.48 dB, 86.17 dB, and 69.22 dB respectively.

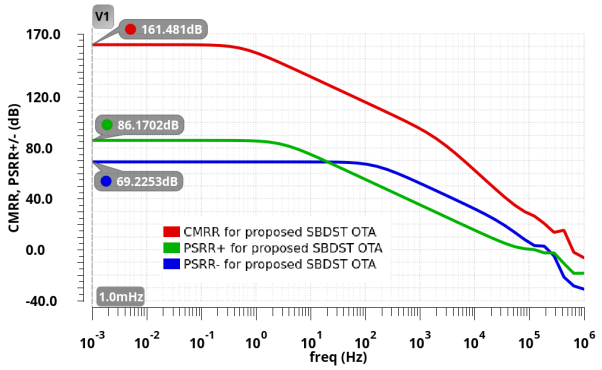

Figure 7: CMRR, PSRR (+/–) of proposed SBDST OTA

Figure 8 shows a unity gain closed loop structure of the suggested SBDST OTAs by shorting its inverting input to output to achieve the transient response of large-signals. The output response is highlighted in Fig. 9 for a 15pF capacitive load when a step input signal of 0.5V peak-to-peak voltage (V_{pp}) at 250Hz frequency is applied at the non-inverting input of OTA. It is found that the value of an average slew rate of the SBDST OTA is 2.07 V/ms.

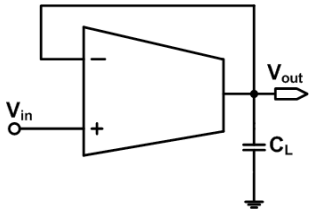

Figure 8: Unity gain configuration of the SBDST OTA

Sinusoidal transient response is evaluated by applying two sinusoidal input signals of $0.5V_{pp}$ and $0.4V_{pp}$ with common-mode voltages (V_{cm}) of 0.25V and 0.2V, respectively on the non-inverting input terminal in Fig. 8 at 250 Hz frequency. The simulation's outputs are revealed in Fig. 10(a) and (b), the result displays that the proposed OTA provides (12.55 mV–491.3 mV) and (12.56 mV–399.37 mV) of output signal swing respectively. The output voltage swing in response to a sinusoidal transient is nearly rail-to-rail.

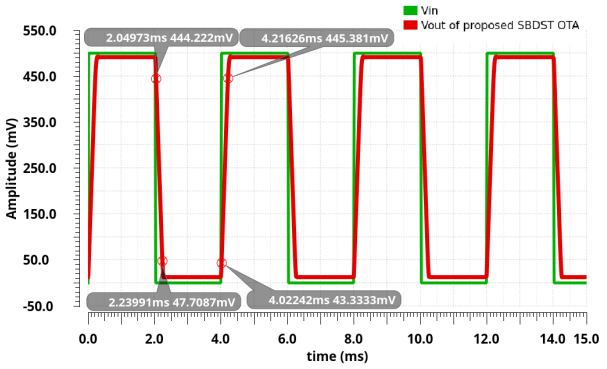

Figure 9: Large-signal pulse response to 0.5Vpp at 250 Hz square wave for proposed SBDST OTA

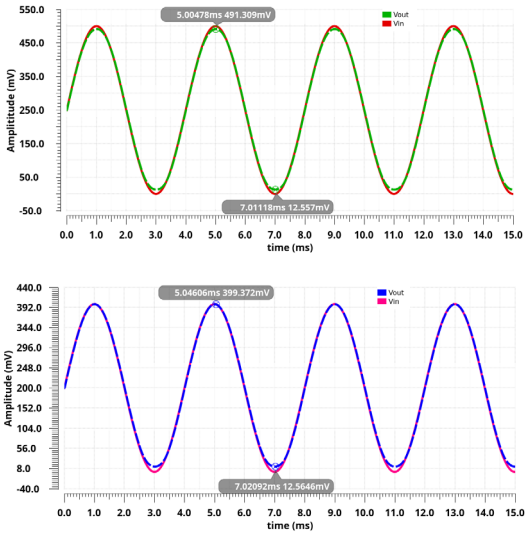

Figure 10: Sinusoidal transient response of the proposed SBDST OTA for (a) $V_{in,pp}$ = 0.5V with V_{cm} = 0.25V, (b) $V_{in,pp}$ = 0.4V with V_{cm} = 0.2V

The proposed OTA's input common-mode range (ICMR) is evaluated by performing its DC sweep analysis in a non-inverting voltage buffer configuration with a 15pF capacitive load, and the simulation's output is exposed in Fig. 11(a), and the variation of error voltage (V_{out}–V_{in}) over the whole input (0 to V_{DD}) voltage range is displayed in Fig. 11(b). It has been found that the error voltage generated at 0V input is 12.63 mV, while at 0.5V input is 8.8 mV only. Thus, it is ensured from the DC sweep results revealed in Fig. 11(a) and (b), that the proposed SBDST OTA is linear over a wide range of ICMR.

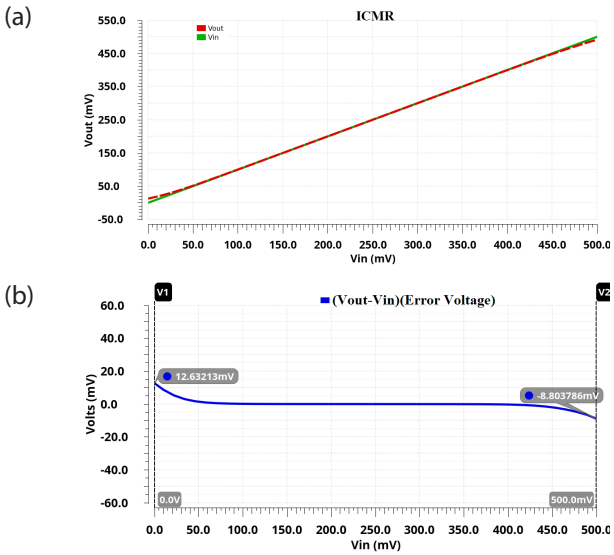

Figure 11: (a) DC sweep for ICMR of the SBDST OTA, (b) Error voltage (V_{out} - V_{in}) in DC sweep

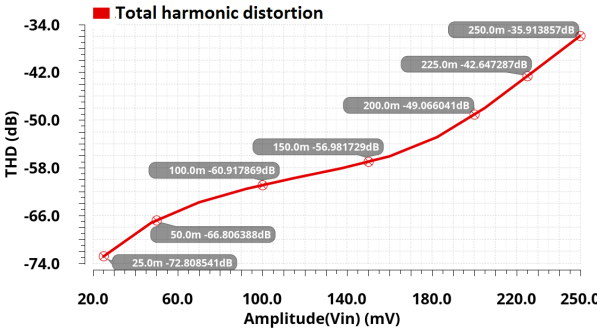

Figure 12: Plot of THD against amplitude for SBDST OTA

A 250 Hz sine wave input signal with varying peak-to-peak amplitudes from 50mV to 500mV has been used to assess the nonlinearity of the SBDST OTA in a unit gain configuration. The simulation result is highlighted in figure 12. At 200 mV (pp), the total harmonic distortion is -60.91dB, and up to 466 mV(pp) amplitude of the input sine wave, the SBDST OTA ensures that the THD value is less than -40dB.

The robustness of the OTA is determined by the deviation of its performance parameters from process and mismatch. For 300 samples, Monte Carlo simulations are utilized to assess the proposed SBDST OTA's robustness. The statistical data of such analysis is shown in Fig. 13 in the form of a histogram.

In addition to this, Monte Carlo simulations of the whole parameters of the SBDST OTA have been tabularized in Table 1. Table 1's outcomes demonstrate that the proposed OTA delivers low standard deviation (SD) for all the performance parameters and hence is insensitive to process variations.

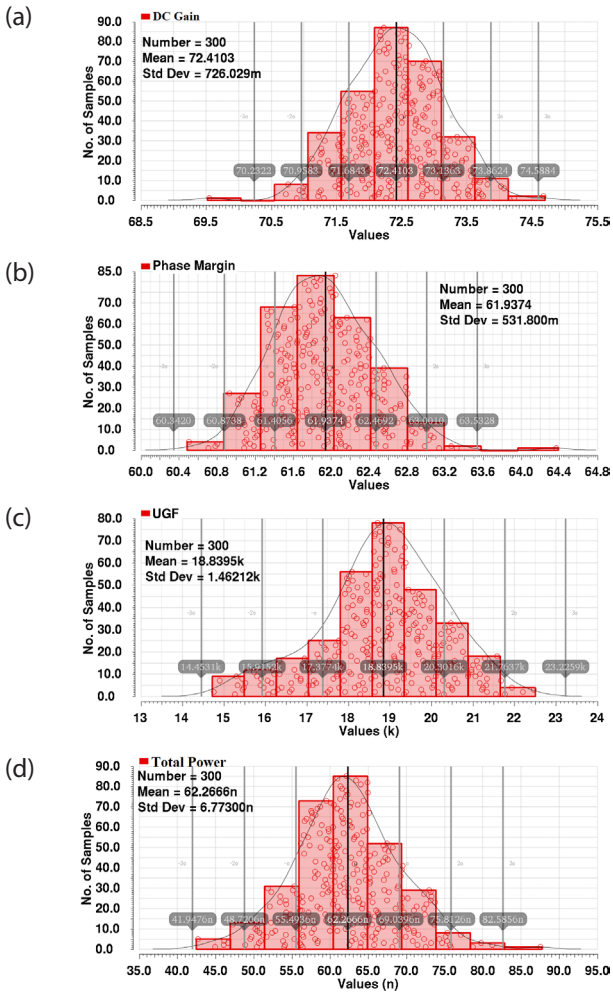

Figure 13: Simulation results of Monte Carlo iteration of (a) DC gain, (b) PM, (c) UGF, (d) total power consumption for 300 samples

Table 1: Performance result of proposed SBDST OTA under Monte Carlo simulation using 300 samples

Parameters	Mean (μ)	SD (σ)
Open loop DC gain (dB)	72.41	726m
Phase margin (degree)	61.94	531.8m
UGF (kHz)	18.84	1.462k
CMRR (dB) @ 1mHz	151.7	10.66
PSRR+ (dB) @ 1mHz	86.31	1.399
PSRR– (dB) @ 1mHz	69.28	883.6m
SR(av) (V/ms)	2.078	140.1m
IRN (μV/Hz$^{0.5}$) at 1kHz	0.96	6.999n
Total current (nA)	124.5	13.55n
Total Power (nW)	62.27	6.773n

Integrated circuits (ICs) must be so designed by manufacturers that after fabrication, PVT (process, voltage, and temperature) fluctuations have no effect on ICs. Deviations in manufacturing conditions like dopant concentrations, temperature, pressure, and variations in the semiconductor fabrication process cause "process

variation". The other key factors for process variation are variations in metal thickness, oxide thickness, UV light wavelength, faults in the manufacturing process, and variations in transistors characteristics [12]. There may be a chance of voltage fluctuation also in some circumstances, so the proposed OTA's simulation results should also be verified by varying the supply voltage.

Figure 14 shows the five process corners (TT, FF, SS, FNSP, and SNFP) effects at 27 ºC on the gain and phase margin of the proposed SBDST circuit. The SS corner has the largest DC gain, measuring 76 dB, and the FNSP corner has the lowest DC gain, measuring 65.59 dB. To check the sensitivity of the proposed OTA against the variations of PVT, corner analysis for five different corners at temperatures (–14 ºC, 27 ºC, and 60 ºC) has been done, and the performance of OTA has been also verified by varying ±10% supply voltage. The simulation results of all the performance parameters against fluctuations of PVT are tabulated in Table 2 and Table 3.

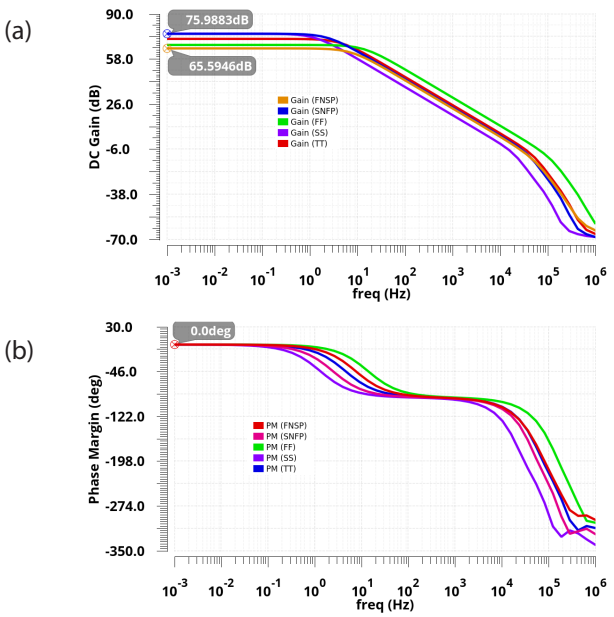

Figure 14: Process corners effect on DC gain and phase margin at room temperature

Table 2: Simulation results on the variation of supply voltage

Parameters	VDD – 10%	VDD + 10%
Open loop DC gain (dB)	63.33	77.64
Phase margin (degree)	68.43	56.83
UGF (kHz)	7.4	27.46
CMRR (dB) @ 1mHz	126.88	115.1
PSRR+ (dB) @ 1mHz	71.13	94.4
PSRR– (dB) @ 1mHz	61.66	73.28
IRN (μV/Hz$^{0.5}$) at 1kHz	0.96	0.94
Total current (nA)	102.9	144
Total Power (nW)	46.3	79.2

Figure 15 depicts the layout of the single-stage SBDST OTA. The proposed OTA takes up (76 x 81) μm2 area, including the area of the compensation capacitor, and the post-layout outcome of the AC response of the SBDST OTA is exposed in Fig. 16. The simulation outcomes of post-layout express that the open loop DC gain, UGF, and phase margin are 72.281 dB, 18.329 kHz, and 61.635º respectively. The results of pre-layout and post-layout AC responses expose that there is a high degree of proximity. This proximity supports the usability and design of this SBDST OTA.

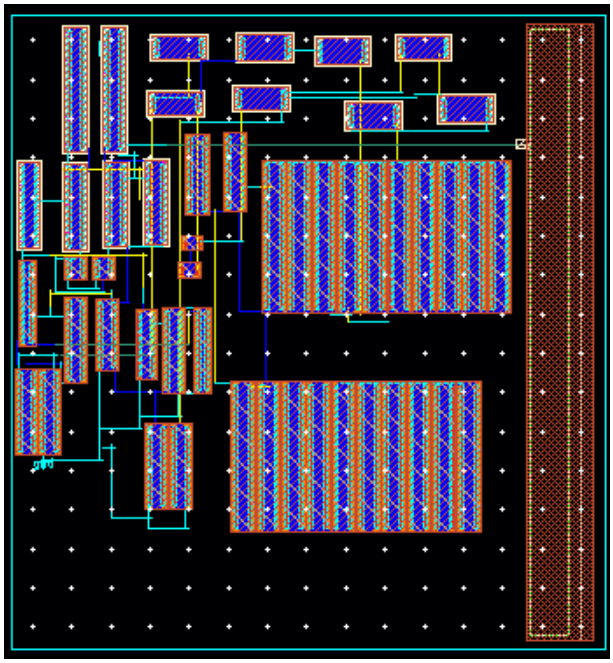

Figure 15: Proposed SBDST OTA's layout

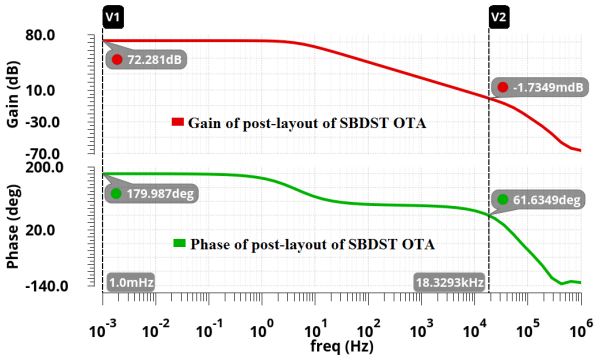

Figure 16: Post-layout AC plot of BDST OTA

Table 3: Simulation results of the performance of SBDST OTA on variations of process and temperature

Parameters	Different corners at temperature –14 °C				
	TT	FF	SS	SNFP	FNSP
Open loop DC gain (dB)	79.41	76.17	80.68	79.08	73.63
Phase margin (degree)	53.37	54.04	53.29	58.79	54.1
UGF (kHz)	9.08	23.57	2.68	5.21	10.16
CMRR (dB) @ 1mHz	135.18	131.26	149.96	109.27	133.98
PSRR+ (dB) @ 1mHz	98.44	91.51	102.45	91.49	85.1
PSRR– (dB) @ 1mHz	73.09	70.34	74.68	72.24	68.85
SR(av) (V/ms)	1.22	2.5	0.58	1.58	0.84
IRN (μV/Hz$^{0.5}$) at 1kHz	0.93	0.81	1.31	1.03	0.88
Total Power (nW)	18.14	58.99	4.83	10.85	29.58
Parameters	Different corners at temperature 27 °C				
	TT	FF	SS	SNFP	FNSP
Open loop DC gain (dB)	72.36	68.06	76	75.99	65.59
Phase margin (degree)	61.96	65.42	59.69	61.28	68.07
UGF (kHz)	19.11	34.77	8.47	15.41	14.39
CMRR (dB) @ 1mHz	161.49	142.19	131.91	107.02	136.82
PSRR+ (dB) @ 1mHz	86.17	79.86	93.27	89.12	74.44
PSRR– (dB) @ 1mHz	69.21	65.56	72.41	71.72	63.69
SR(av) (V/ms)	2.06	3.66	1.12	2.91	1.41
IRN (μV/Hz$^{0.5}$) at 1kHz	0.95	0.92	1.08	0.94	0.96
Total Power (nW)	62.81	162.98	21.79	42.62	88.66
Parameters	Different corners at temperature 60 °C				
	TT	FF	SS	SNFP	FNSP
Open loop DC gain (dB)	65.35	60.48	69.72	70.18	14.08
Phase margin (degree)	69.83	73.96	65.86	65.74	102.17
UGF (kHz)	23.15	33.87	13.87	25.77	0.093
CMRR (dB) @ 1mHz	133.58	139.19	124.83	102.66	137.38
PSRR+ (dB) @ 1mHz	76.11	70.17	82.49	81.76	19.35
PSRR– (dB) @ 1mHz	63.69	59.27	67.59	67.47	14.08
SR(av) (V/ms)	2.74	4.32	1.66	3.9	1.8
IRN (μV/Hz$^{0.5}$) at 1kHz	1.03	1	1.09	0.96	1.21
Total Power (nW)	137.94	316.13	55.62	102.48	175.65

5 Performance comparison and discussions

Table 4 lists the performance parameters of proposed OTAs. To verify the overall performance of OTA in terms of the responses to small- and large-signals, two popular figures of Merit (FOM_{Sm}, FOM_{La}) are specified in [22, 27, 28], and are given in equations (25) and (26) respectively.

$$FOM_{Sm} = \frac{UGF\left(MHz\right)\times C_L\left(pF\right)}{I_T\left(\mu A\right)} \tag{25}$$

$$FOM_{La} = \frac{SR_{av}\left(V/\mu s\right)\times C_L\left(pF\right)}{I_T\left(\mu A\right)} \tag{26}$$

The proposed SBDST OTA performance parameters are compared with some of the other recent BD OTAs and reported in Table 5. According to Table 5, the proposed SBDST OTA has offered the largest DC gain, PSRR+/– among others and also has maximum CMRR except that of [19] only. The proposed SBDST OTA's large-signal response (FOM_{La}) is comparable to only [14] in comparison to the other remaining OTAs given in Table 5, but it has provided the highest small-signal response (FOM_{Sm}) as compared to other reported OTAs, with the exception of [20].

Table 4: Proposed SBDST OTA performance parameters

Parameters	SBDST OTA
Power supply (V)	0.5
Load capacitance (pF)	15
Technology	0.18µm
DC gain	72.35
Phase margin (°)	61.33
UGF (kHz)	18.7
CMRR (dB) @ 1mHz	161.48
PSRR+ (dB) @ 1mHz	86.17
PSRR– (dB) @ 1mHz	69.22
IRN @ 1kHz(µV/Hz$^{0.5}$)	0.95
SR average (V/ms)	2.07
Total current (nA)	125.64
Total power (nW)	62.82
FOM_{Sm}	2.23
FOM_{La}	0.247

6 Conclusions

This article's work presents an enhanced bulk-driven single-stage architecture of an OTA functioning in the weak-inversion region, powered by 0.5V of power supply. The proposed architecture of the amplifier employs a BD-FVF that is based on an adaptively biased differential input pair operating in the class-AB mode to improve dynamic current and unity gain frequency. Additionally, it employs a partial positive feedback technique in the differential pair's core to increase the gain of the circuit. Further, the gain of the circuit is increased by using a low-power, high-performance current mirror load based on FVF at the amplifier's output. The suggested OTA's simulation results show that the amplifier uses just 62.82nW of power and has a DC gain of 72.35 dB, a phase margin of 61.32°, and a UGF of 18.7 kHz. For a 250 Hz input sine wave of 200 mV (pp), the SBDST OTA in its unity gain configuration offers -60.91 dB total harmonic distortion. The obtained outcomes of the amplifier ensured that the proposed SBDST OTA is appropriate for biomedical signal processing, audio signal processing, and low-frequency sensors.

7 Conflict of Interest

The authors declare that they have no conflicts of interest.

Table 5: Proposed SBDST OTA and previously reported BD OTAs performance differences at 0.18µm technology

Parameters	[14] 2015	[11] 2017	[15] 2017	[16] OTA_1 2018	[16] OTA_2 2018	[17] 2018	[19] 2019	[29] 2021	[20] 2022	This-Work 2023
C_L(pF)	15	15	12	15	15	50	15	50	30	15
Power supply (V)	0.5	0.5	0.6	0.6	0.6	0.8	0.6	0.7	0.4	0.5
Phase margin (°)	68.9	54	62.45	93	78.41	87	74	89.07	60	61.33
(DC gain)[a] (dB)	67.8	70.4	61.5	61.9	60.76	44.3	71@ 0.1Hz	71.35	60	72.35
UGF (MHz)	0.003	0.009	0.03015	0.0024	0.00773	1.45	0.0182	0.00107	0.007	0.0187
CMRR[a] (dB)	–	106 @ 1Hz	–	122 @ 1Hz	119@ 1Hz	–	201.8@ 10Hz	138.5	85	161.48
PSRR[a]+ (dB)	–	70@ 1Hz	67.9	62.8@ 1Hz	61.8 @ 1Hz	–	77.4@ 10Hz	77.08	76	86.17
PSRR[a]– (dB)	–	–	–	–	–	–	–	60.23	–	69.22
IRN[b] @ (µV/HZ0.5)	0.56	2.53	6.25 @ 0.1Hz	2.454	2.97	–	0.25@ 0.1Hz	0.779	–	0.95
SR average (V/µs)	0.84/ 0.59[c]	0.967	0.0553	1.15	1.404	3.5	0.0066	0.00157	0.079	0.00207
Total current (nA)	52	125.5	275	50.63	115	62,000	240	200	60	125.64
Total power(nW)	26	64	165	30.38	69	49,600	144	140	24	62.82
FOM_{Sm}	0.94	1.11	1.31	0.711	1.008	1.17	1.13	0.27	3.5	2.23
FOM_{La}	0.24	116	3.01	340.7	183.13	2.82	0.412	0.39	39.5	0.247
Area (µm^2)	52000	–	–	6620	7406	–	16,000	–	7900	6,156

a: at 1mHz, b: at 1kHz, c: V/ms

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